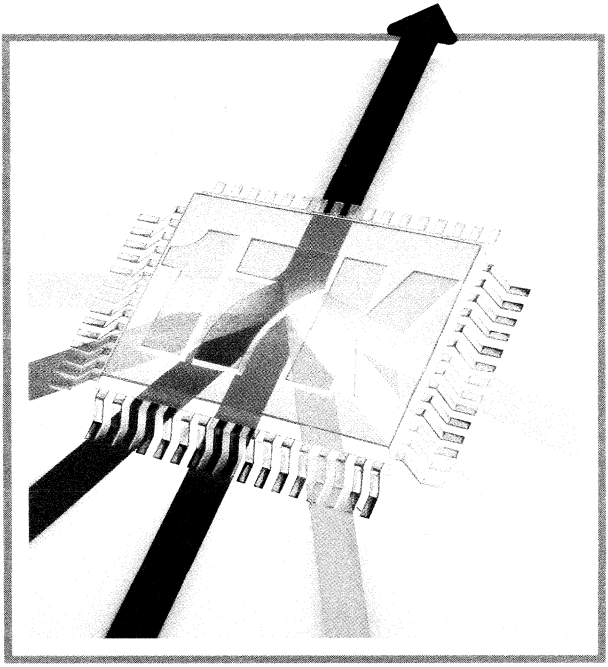
μPD17K Family
4-Bit CMOS
Microcomputers



Data Book

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μPD17K Family
4-Bit CMOS
Microcomputers

Data Book

Table of contents

General information

Section 1 - General information

μPD170XX series-digital tuning systems (DTS) family

Device	Main applications	Features	ROM	RAM	Pins/Package
	Car radios, tuners	Common features: Serial interface, prescaler, PLL, interface counter, 6-bit A/D converter, 8-bit D/A converter OTP versions available			
μPD17001GH			4K x 16	224 x 4	48/Flat
μPD17003AGF		LCD controller/driver	4K x 16	320 x 4	80/Flat
μPD17005GF		LCD controller/driver	8K x 16	432 x 4	80/Flat
μPD17010GF		LCD controller/driver Enhanced timer for remote control receiver	8K x 16	432 x 4	80/Flat
μPD17006GF		Enhanced timers for RDS decoding SRAM interface, RDS firmware	12K x 16	896 x 4	80/Flat
	TV, LCD-TV, VCR, all with PLL	Common features: Image display controller, external prescaler requiring PLL, serial interface 4-bit A/D and 6-bit D/A converter OTP versions available for most devices			
μPD17002CU			4K x 16	336 x 4	48/SDIP
μPD17008CW*		2 Kbit EEPROM	16K x 16	672 x 4	64/SDIP
	Portable TV, CTV, all voltage synthesizer types	Common features: Image display controller, pulse width modulation for voltage synthesis, serial interface 4-bit A/D and 6-bit D/A converter OTP versions not available			
μPD17051CU			8K x 16	448 x 4	48/SDIP
μPD17052CW			8K x 16	448 x 4	64/SDIP
μPD17053CW			12K x 16	672 x 4	64/SDIP
OTP (one-time programmable) versions for evaluation and prototyping					
μPD17P001GH		OTP for μPD17001GH			
μPD17P005GF		OTP for μPD17003GH and μPD17005GF			
μPD17P010GF		OTP for μPD17010GF			
μPD17P006GF		OTP for μPD17006GF			
μPD17P008CW*		OTP for μPD17008CW			

** under development*

μPD171XX series-general-purpose controller family

Device	Main applications	Features	ROM	RAM	Pins/Package
μPD17102G	Rice cooker,french fryer	LCD controller/driver (48 segments), serial interface, 2 x 8-bit timers, 2 op amps,4 comparator inputs, 6-bit D/A converter OTP versions not available	2K x 16	222 x 4	52/Flat
μPD17106GC	Front panel	High voltage LCD controller/driver for up to 176 segments, serial interface OTP versions available	4K x 16	178 x 4	64/Flat
	Electric cooker, iron, toaster, battery charger	Simplest μCOM in small package OTP versions available Low voltage versions available			
μPD17103(L)CX μPD17103(L)GS μPD17104(L)CS μPD17104(L)GS		Ceramic resonator	0,5K x 16	16 x 4	16/DIP 16/SOP 22/SDIP 24/SOP
μPD17107(L)CX μPD17107(L)GS μPD17108(L)CS μPD17108(L)GS		RC oscillator			16/DIP 16/SOP 22/SDIP 24/SOP
	Electric drills, heating control, central locking, door opener	Small μCOM with serial interface, 8-bit timer, power-on/down reset			
μPD17120CS μPD17120GS		RC oscillator	768 x 16	64 x 4	24/SDIP 24/SOP
μPD17121CS μPD17121GS		Ceramic resonator	768 x 16	64 x 4	24/SDIP 24/SOP
μPD17132CS μPD17132GS		RC oscillator	1K x 16	111 x 4	24/SDIP 24/SOP
μPD17133CS μPD17133GS		Ceramic resonator	1K x 16	111 x 4	24/SDIP 24/SOP
	Washing machine, coffee machine, shaver	Compact μCOM with 8-bit A/D converter, zero cross detection, 8-bit timers, serial interface OTP versions available			
μPD17134ACT μPD17134AGT		RC oscillator	1K x 16	112 x 4	28/SDIP 28/SOP
μPD17135ACT μPD17135AGT		Ceramic resonator			28/SDIP 28/SOP
μPD17136ACT μPD17136AGT		RC oscillator	2K x 16	112 x 4	28/SDIP 28/SOP
μPD17137ACT μPD17137AGT		Ceramic resonator			28/SDIP 28/SOP
μPD17156CU		Ceramic resonator	3K x 16	336 x 4	48/SDIP
OTP (one-time programmable) versions for evaluation and prototyping					
μPD17P103CX		OTP for μPD17103CX			16/DIP
μPD17P103GS		OTP for μPD17103GS			16/SOP
μPD17P104CS		OTP for μPD17104CS			22/SDIP
μPD17P104GS		OTP for μPD17104GS			24/SOP
μPD17P106GC		OTP for μPD17106GC			64/QFP
μPD17P107CX		OTP for μPD17107CX			16/DIP
μPD17P107GS		OTP for μPD17107GS			16/SOP
μPD17P108CS		OTP for μPD17108CS			22/SDIP
μPD17P108GS		OTP for μPD17108GS			24/SOP
μPD17P132CS		OTP for μPD17132 and μPD17120			24/SDIP
μPD17P132GS		OTP for μPD17132 and μPD17120			24/SOP
μPD17P133CS		OTP for μPD17133 and μPD17121			24/SDIP
μPD17P133GS		OTP for μPD17133 and μPD17121			24/SOP
μPD17P136ACT		OTP for μPD17134ACT and μPD17136ACT			28/SDIP
μPD17P136AGT		OTP for μPD17134AGT and μPD17136AGT			28/SOP
μPD17P137ACT		OTP for μPD17135ACT and μPD17137ACT			28/SDIP
μPD17P137AGT		OTP for μPD17135AGT and μPD17137AGT			28/SOP
μPD17P156CU		OTP for μPD17156CU			48/SDIP

μPD172XX series-remote controller family

Device	Main applications	Features	ROM	RAM	Pins/Package
	Remote control	Low voltage operation (2V), signal carrier on chip, serial interface, 8-bit timer, low voltage detection circuit on chip OTP versions available			
μPD17201AGF	High-end general purpose	4-channel 8-bit A/D converter, LCD controller driver (136 segments)	3K x 16	336 x 4	80/Flat
μPD17207GF			4K x 16	336 x 4	
μPD17202AGF	VCR, TV, home electronics	LCD controller/driver (96 segments)	2K x 16	112 x 4	64/Flat
μPD17203AGC	Learning remote	16 Kbit static RAM, receiver and transmitter circuit on chip, serial interface, watchdog timer	4K x 16	336 x 4	52/Flat
μPD17204GC		8 Kbit static RAM, otherwise like μPD17203AGC	8K x 16		
μPD17211GT	General purpose	Programmable carrier generator	2K x 16	111 x 4	28/SOP
OTP (one-time programmable) versions for evaluation and prototyping					
μPD17P207AGF		OTP for μPD17201AGF and μPD17207GF			80/Flat
μPD17P202AGF		OTP for μPD17202AGF			64/Flat
μPD17P203AGC		OTP for μPD17203AGC			52/Flat
μPD17P204GC		OTP for μPD17204GC			52/Flat
μPD17P214GT		OTP for μPD17211GT			28/SOP

OTPs are designed to cover the full operating range

Device	SE board	Probe	Adapter	Assembler package
μPD17001GH	SE-17001	EP-17001GH	EV-9200GH-48	
μPD17002CU	SE-17002	EP-17002CU		
μPD17003AG	SE-17010	EP-17003GF	EV-9200G-80	
μPD17005GF	SE-17010	EP-17003GF	EV-9200G-80	
μPD17006GF	SE-17006	EP-17201GF	EV-9200G-80	
μPD17008CW	SE-17008	EP-17008CW		AAMSD-I5DD-170XX
μPD17010GF	SE-17010	EP-17003GF	EV-9200G-80	
μPD17051CU	SE-17051	EP-17051CU		
μPD17052CW	SE-17052	EP-17052CW		
μPD17053CW	SE-17053	EP-17052CW		
μPD17102G	SE-17102	EP-17102G	EV-9200G-52	
μPD17103(L)CW	SE-17103L	EP-17103CX		
μPD17103(L)GS	SE-17103L	No SOP probe		
μPD17104(L)CS	SE-17104L	EP-17104CS		
μPD17104(L)GS	SE-17104L	No SOP probe		
μPD17106GC	SE-17106	EP-17106GC	EV-9200G-64	
μPD17107(L)CX	SE-17107	EP-17103CX		
μPD17107(L)GS	SE-17107	No SOP probe		
μPD17108(L)CS	SE-17108	EP-17104CS		
μPD17108(L)GS	SE-17108	No SOP probe		
μPD17120CS	SE-17120	EP-17120CS		
μPD17120GS	SE-17120	No SOP probe		
μPD17121CS	SE-17120	EP-17120CS		AAMSD-I5DD-171XX
μPD17121GS	SE-17120	No SOP probe		
μPD17132CS	SE-17120	EP-17120CS		
μPD17132GS	SE-17120	No SOP probe		
μPD17133CS	SE-17120	EP17120CS		
μPD17133GS	SE-17120	No SOP probe		
μPD17134ACT	SE-17134	EP-17K28CT		
μPD17134AGT	SE-17134	EP-17K28GT		
μPD17135ACT	SE-17134	EP-17K28CT		
μPD17135AGT	SE-17134	EP-17K28GT		
μPD17136ACT	SE-17134	EP-17K28CT		
μPD17136AGT	SE-17134	EP-17K28GT		
μPD17137ACT	SE-17134	EP-17K28CT		
μPD17137AGT	SE-17134	EP-17K28GT		
μPD17156CU	SE-17156	EP-17156CU		
μPD17201AGF	SE-17207	EP-17201GF	EV-9200GH-80	
μPD17202AGF	SE-17202	EP-17202GF	EV-9200GH-64	
μPD17203AGC	SE-17203	EP-17203GC	EV-9200GH-52	
μPD17204GC	SE-17204	EP-17203GC	EV-9200GH-52	AAMSD-I5DD-172XX
μPD17207GF	SE-17207	EP-17201GF	EV-9200GH-48	
μPD17211CT	SE-17211	EP-17K28CT		
μPD17211GT	SE-17211	EP-17K28GT		

μPD17K-Family

Section 2 - μPD 17K-Family

μPD170xx Series (Digital tuning systems)

μPD171xx Series (General purpose microcomputers)

μPD172xx Series (Remote controllers)

A new addition to NEC's wellestablished microcomputer families is the μPD 17K. Most devices in this 17K family are tailor-made for very specific, high-volume applications and offer an extremely attractive cost-performance ratio. The family contains four groups of devices all with the same CPU core, but with different on-chip peripheral function blocks for specific tasks, depending on the target application. The devices 4-bit microcomputer has a maximum ROM address space of 64K words (organized in 16-bit words). The architecture of the μPD 17K family is based on an earlier family of digital tuning systems, the μPD 1700, which proved their worth in many audio and car radio applications. This forerunner was limited to DTS functions, in contrast to today's μPD 17K family which has a very much broader application base. The diagram shows how the 17K family consists of four different device groups each for a different application area - digital tuning systems, remote control, general purpose and home automation.

Digital tuning system

A digital tuning system (DTS) is a special microcomputer for digitally tuning the receiver of TV, VCR and audio equipment. This microcomputer usually has a PLL (phase-locked loop) circuit integrated on chip plus various other peripheral functions, depending on the required features.

General-purpose devices

One product line within the 17K family is not tailored for a specific application area - the μPD 171XX devices are designed as more general-purpose ICs. General-purpose ICs either replace dedicated hardware logic in more complex systems, or serve as single-chip controllers in mini applications like timers, electric irons, shavers, toys and LCD front panels.

Remote control

Nowadays infrared light is a preferred medium for remote control. The demand, on the one hand, for more system comfort and higher system flexibility, and on the other, for convenience and low cost, necessitates a wireless method - either infrared or radio frequency. Remote control ICs are used in the transmitters of infrared remote control systems like those used for operating TV or radio sets, video recorders and hi-fi equipment. Other applications include electronic locks, security systems and burglar alarms.

17K-Family

- One machine-cycle instruction execution
- General Register Machine not just Accu based CPU
- 16 bit instruction length

170xx

- Digital tuning systems
- Serial interface
- A/D-D/A-converters
- IF-counter
- LCD-driver
- Image display controller
- PLL

171xx

- White goods controllers
- Low power consumption
- General purpose
- Serial interface
- A/D-converter
- Timer
- Low voltage operation

172xx

- Remote controller
- Low voltage operation
- Carrier frequency generation
- Low voltage detection circuit
- Constant LCD voltage circuit
- Learning remote controller
- Built-in preamplifier
- Large static RAM

170xx – Overview

		DTS (TUNERS)					LCD-TV/VCR		Portable TV; Voltage synthesizer		
		17001	17003A	17005	17010	17006	17002	17008	17051	17052	17053
ROM (16 bits)		3836	3836	7932		12288	3968	16256	8192		12288
RAM (4 bits)		224	320	432		896	336	672	448		672
Stack levels		7			9	7	6	7	6		7
Minimum instruction execution time		4.44µs/4.5MHz				1.78µs/ 4.5MHz	2µs/8MHz				
ADCs		6 x 6 bit				6 x 8 bit	6 x 4 bit	8 x 4 bit			
DACs (PWM)		3 x 8 bit				3 x 9 bit	4 x 6 bit	9 x 8 bit 6 x 6 bit	3 x 6 bit	4 x 6 bit	
Amplifiers		1			–		–				
Int./ext. interrupts		3/1	3/2		4/2		–/1				
Serial interface		1 channel 3 wires 1 channel 2 wires	2 channels 3 wires 1 channels 2 wires				1 channel 3 wires 1 channel 2 wires				
I/O-Ports		12	16			48	15	16	15	20	
Input-Ports		8					4				
Output-Ports		12	9			11	8	25	12	20	
LCD Driver		–	30 segments/2 common			–	–				
IDC	charact. on screen						99	200	97	99	199
	different types						120	248	128	128	256
Counter		16 bit IF counter					Vsync-; Hsync- counter				
PLL/voltage synthesizer		150MHz PLL	250MHz PLL	150 MHz PLL			15 MHz PLL (ext. preecaler required)		14 bit D/A (PWM) Voltage synthesizer		
Pins Package		48 QFP	80 QFP				48 SDIP/ QFP	64 SDIP	48 SDIP	64 SDIP	
OTP		17P001	17P005		17P010	17P006	No OTP version	17P008	No OTP version		

171xx – Overview

	17102	17106	17103 (L)*	17104 (L)*	17107 (L)*	17108 (L)*	17120	17121	17132	17133
ROM (16 bits)	2048	4096	512				768		1024	
RAM (4 bits)	222	178	16				64		104	
Stack levels	3	7	1							
Minimum instruction execution time	2 µs/8 MHz		STD: V_{DD} 4.5 - 6V 2 µs/8 MHz L: V_{DD} 1.8 - 3.6V 8 µs/2 MHz		STD: V_{DD} 4.5 - 6V 8 µs/1 MHz L: V_{DD} 1.5 - 3.6V 40 µs/200 kHz		8 µs/ 2 MHz	2 µs/ 8 MHz	8 µS/ 2 MHz	2 µs/ 8 MHz
ADCs	6 bits 4 channels	–					–			
DACs (PWM)	1 x 6 bit	–								
Timers	8 bits 2 channels	–					8 bit 1 channel			
Zero-Cross Detectors	1	–					–			
Int./ext. interrupts	2/3	2/1	–				2/1			
Serial interface	1 channel 3 wires	2 channels 2 and 3 wires	–				1 channel 3 wires			
LCD-Driver	48 segments	176 segments	–							
I/O-Ports	16	5	11	16	11	16	18			
Input-Ports	8	4	–							
Output-Ports	14	–								
Amplifiers	2	–								
Clock Generator	Ceramic resonator				RC oscillator			Ceramic resonator	RC oscillator	Ceramic resonator
Pins Package	52 QFP	64 QFP	16 DIP 16 SOP	22 SDIP 24 QFP	16 DIP 16 SOP	22 SDIP 24 SOP				
OTP	No OTP version	17P106	17P103	17P104	17P107	17P108	17P132	17P133	17P132	17P133

*L: Low voltage version

171xx – Overview

	17134A	17136A	17135A	17137A	17156
ROM (16 bits)	1024	2048	1024	2048	6144
RAM (4 bits)	112				336
Stack levels	5				7
Minimum instruction execution time	8 µs / 1 MHz		2 µs / 8 MHz		2 µs / 8 MHz
ADCs	1 x 8 bit / 4 channels				8 bit / 8 channels
DACs (PWM)	–				
Timers	8 bit / 2 channels + watchdog				8 bit / 3 channels + watchdog
Zero-Cross Detectors	1				–
Int./ext. interrupts	4/1				6/1
Serial interface	1 channel 3 wires				1 channel 3 wires
LCD-Driver	–				–
I/O-Ports	21				32
Input-Ports	9				
Output-Ports	–				–
Amplifiers	–				–
Clock Generator	RC resonator		Ceramic resonator		Ceramic resonator
Pins Package	28 SDIP 28 SOP				48 SDIP
OTP	17P136A		17P137A		17P158

172xx – Overview

	17201A	17207	17202A	17203A	17204	17211
ROM (16 bits)	3072	4096	2048	4096	7936	7936
RAM (4 bits)	336		112	336 + 4096 SRAM	336 + 2048 SRAM	111
Stack levels	5				7	5
Instr. exec. time	4 µs / 4 MHz					
ADCs	4 x 8 bit		–			–
Timers	8 bit + watchdog			8 bit / 10 bit / 16 bit + watchdog		8 bit
Ext. interrupt	1					1
Serial interface	1		–	1		–
I/O-Ports	19		16	28		21
LCD-Drivers	34 segments + 4 common		24 segments + 4 common	–		–
Pins Package	80 QFP		64 QFP	52 QFP		28 SOP
OTP	17P207		17P202A	17P203A	17P204	17P214

BUILT-IN PRESCALER

μPD17001 is a 4 bits CMOS microcomputer for Digital Tuning System implemented prescaler (operational frequency up to 150 MHz), PLL frequency synthesizer and IF counter on chip.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

As PLL frequency synthesizer can apply pulse swallow method, high performance tuner is easily constructed by selecting high reference frequency like 50 kHz or 100 kHz.

In addition, station detect is realized by counting intermediate frequency of tuner using built-in 16 bits IF counter.

As system development support tools of μPD17001, IE-17K (In Circuit Emulator) and AS17K (assembler) are prepared.

FEATURES

- 4 bits microcomputer for Digital Tuning System
- program memory (ROM)
  : 8 K bytes (16 bits x 3836 steps)
- data memory (RAM)
  : 224 words (4 bits x 224 words)
- stack level: 7
- 35 types of simple instruction
- decimal operation
- instruction execution time: 4.44 μs
  (with 4.5 MHz crystal oscillator)
- built-in PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequencies can be selected by software.
  1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
- built-in amplifier for LPF (Low pass filter)
- built-in IF counter (AMIFC, FMIFC)
- built-in 8 bits serial interface
  1 system 2 channels: 3 wire or 2 wire system
- built-in D/A converter: 8 bits x 3 (PWM output)
- built-in A/D converter: 6 bits x 6
- built-in discharge detection circuit and power on reset circuit
- interrupt
  external interrupt: 2 channels
  internal interrupt: 3 channels
- various I/O ports
  input/output ports: 12 lines
  input ports : 8 lines
  output ports : 12 lines
- built-in CGP (Clock Generator Port)
- single power supply (5 V±10 %)
- CMOS low power consumption
- 48-pin plastic QFP

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

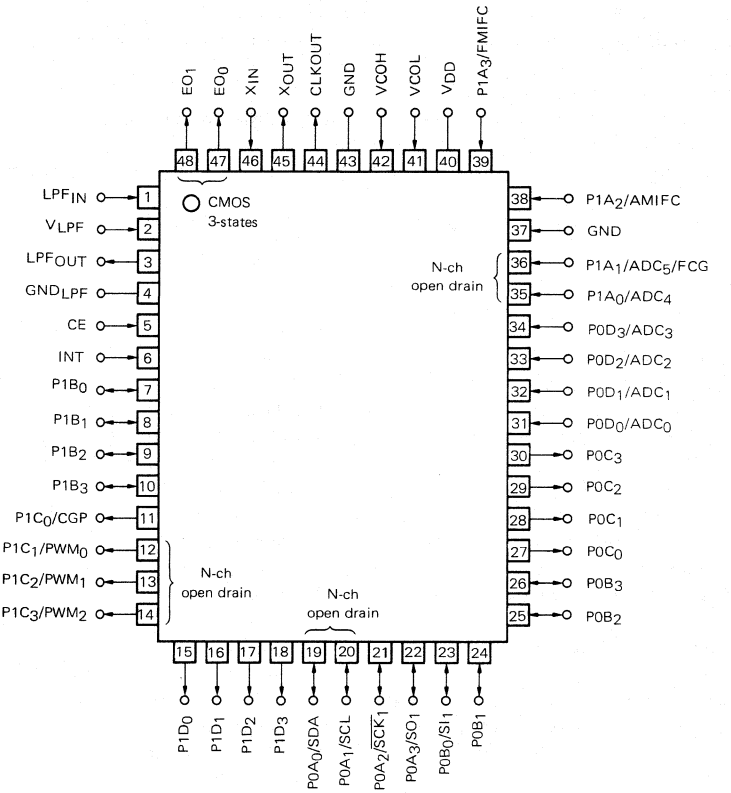
In case of using this interface mode note the following:

Duties when using I2C bus system

Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)

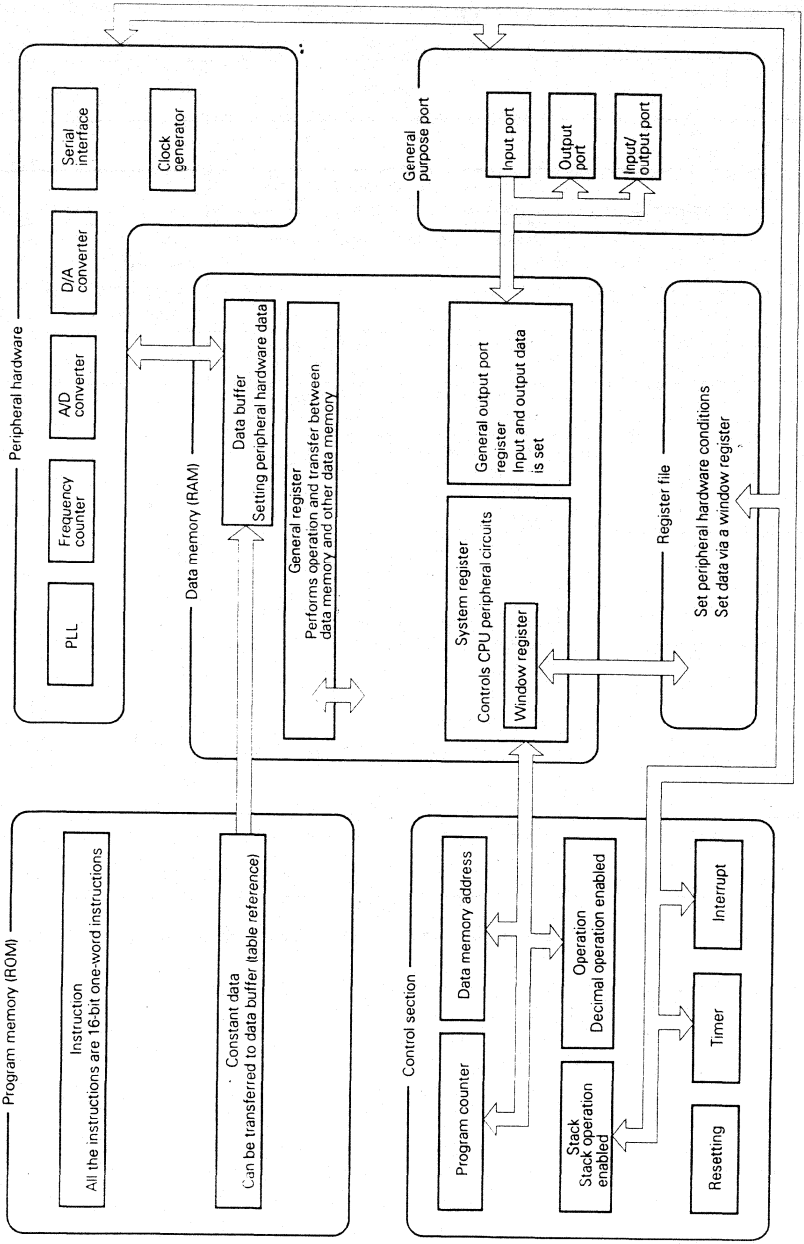


μPD17001 FUNCTION OUTLINE

Item	Function
Program memory (ROM)	• 3836 steps × 16 bits The internal ROM areas can be table-referenced.
General data memory (RAM)	• 224 × 4 bits Data buffer: 4 × 4 bits General register: 16 × 4 bits
System register	• 12 × 4 bits
Register file	• 27 × 4 bits (control register)
General port register	• 8 × 4 bits
Instruction execution time	• 4.44 μs (using 4.5 MHz quartz oscillator)
Stack level	• 7 levels (stack operation enabled)
General purpose port	• Input/output port : 12 • Input ports : 8 • Output ports : 12
Clock generator port (CGP)	• 1 VDP (Variable Duty Pulse) and SG (Signal Generator) functions
Serial interface	• One type (2 channels) 8-bit 3-wire system: 1 channel 8-bit 2-wire system: 1 channel
D/A converter	• 8 bits x 3 (PWM output and output resisting pressure 14 V Max.)
A/D converter	• 6 bits x 6 (consecutive comparison method by software)
Interrupt	• 4 channels (maskable interrupt) External interrupt: 1 channel (INT pin) Internal interrupt : 3 channels (timer, serial interface, and frequency counter)
Timer	• Two types Timer carry FF (1, 5, 100, 250 ms) Timer interrupt (0.11, 1, 5, 100 ms)
Reset	• Power On Reset (at power supply connection) • Resetting by CE pin (CE pin Low - High) • Blackout detection function

Item		Function
PLL frequency synthesizer	Division method	• 2 types Direct division method (VCOL pin 20 MHz Max.) Pulse swallow method (VCOL pin 40 MHz Max.) (VCOH pin 130 MHz Max.)
	Reference frequency	• 12 types are selected by the program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	• Two independent error output
	Phase comparator	• Unlocking can be detected by a program Unlocking FF delay time can be selected
	LPF amplifier	• CMOS operation amplifier output resisting pressure 14 V Max.
Frequency counter		• Frequency test $P1A_3$/FMIFC pin 5-15 MHz $P1A_2$/AMIFC pin 0.1-1 MHz • External gate width test $P1A_1$/ADC_5/FCG pin
Power supply voltage		5 V ± 10 %
Package		48-pin plastic QFP

CONCEPT OF μPD17001



PIN FUNCTIONS

EXPLANATION ON EACH PIN FUNCTION

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON/ RESETTING
1	LPF_{IN} **Notes 1, 2**	Ussed as low pass filter amplifier input port	–	Input. Internal Pull-up.
2	V_{LPF} **Notes 1, 2**	Used as low pass filter amplifier power supply port.	–	–
3	LPF_{OUT} **Notes 1, 2**	Used as low pass filter amplifier output port.	N-ch open drain, withstanding voltage 14 V	High impedance
4	GND_{LPF} **Notes 1, 2**	Uesd as low pass filter amplifier ground.	–	–
5	CE	Used as μPD17001 operation selecting and resetting signal input port.	–	Input
6	INT	Used as edge detecting vector interrupt input port. Both rising and falling edges can be selected.	–	Input
7 | 10	$P1B_0$ | $P1B_3$	Used as 4-bit CMOS input/output port.	CMOS push/pull	Input
11 12 | 14	$P1C_0$ $P1C_1/PWM_0$ | $P1C_3/PWM_2$	Used as port 1C, D/A converter and clock generator port output pin. • $P1C_0$-$P1C_3$ · 4-bit output port • PWM_0-PWM_2 · 8-bit resolution D/A converter output • CGP · Clock generator port output	CMOS push/pull ($P1C_0$/ CGP) N-ch open drain, withstanding voltage 14 V $P1C_1/PWM_0$ to $P1C_3/PWM_2$	Undefind data is output. ($P1C_0$-$P1C_3$)
15 | 18	$P1D_0$ | $P1D_3$	Used as 4-bit CMOS output port.	CMOS push/pull	Undefined data is output.

Notes 1. Refer to **Fig. 16-6 Configuration Example of Operational Amplifier and Low Pass Filter.**

2. Using an external operational amplifier will result in better performance than using the built-in operational amplifier.

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON/ RESETTING
19 20 21 22 23 24 | 26	P0A0/SDA P0A1/SCL P0A2/$\overline{SCK}$ P0A3/SO P0B0/SI P0B1 | P0B3	Used as port 0A, port 0B and input/output port of serial interface. • P0A0-P0A3 · 4-bit input/output port · Permits setting of input/output in units of one bit • P0B0-P0B3 · 4-bit CMOS input/output port · Permits setting of input/output in units of one bit • SDA, SCL · SDA: Serial data input/output · SCL: Serial clock input/output • $\overline{SCK}$, SO, SI · $\overline{SCK}$: Serial clock input/output · SO: Serial data output · SI: Serial data input (SDA and SCL pins cannot be used together with $\overline{SCK}$, SO and SI pins.)	N-ch open drain, voltage 5 V (P0A0/SDA, P0A1/SCL) CMOS push/pull (P0A2/$\overline{SCK}$, P0A3/SO, P0B0, P0B1, P0B2, P0B3)	Input (P0A3-P0A0, P0B3-P0B0)
27 | 30	P0C0 | P0C3	Used as 4-bit CMOS output port.	CMOS push/pull	Undefined data is output.
31 | 34 35 36	P0D0/ADC0 | P0D3/ADC3 P1A0/ADC4 P1A1/ADC5/FCG	Used as port 0D, port 0A, A/D converter analog input and external gate counter input port. • P0D0-P0D3, P0A0, P0A1 · 4-bit input port · Built-in pull-down resistance • ADC0-ADC5 · 6-bit resolution A/D converter analog input port • FCG · External gate counter input port	– N-ch open drain, withstanding voltage 5 V (P1A0/ADC4, P1A1/ADC5/FCG)	Input port with pull-down resistance (P0D0-P0D3)
37, 43	GND	Used as ground pin.	–	–
38 39	P1A2/AMIFC Note P1A3/FMIFC Note	Used as port 1A and frequency counter input port. • P1A2, P1A3 · 4-bit input port • AMIFC, FMIFC · Frequency counter input port Measurable frequencies	–	Input (P1A2-P1A3)

Input Pin	Input frequency	Input amplitude
PIA3/FMIFC	5-15 MHz	0.3 VP-P
PIA2/AMIFC	0.1-1 MHz	0.3 VP-P

Note These pins are used as an AC amplifier input port. The DC compoment should be cut off from the signal to be entered by a series-connected condenser.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>FUNCTION</th><th>OUTPUT TYPE</th><th>POWER ON/ RESETTING</th></tr>
<tr><td>40</td><td>VDD</td><td>Positive power supply.
5 V ±10 % voltage is supplied when CPU and peripheral functions are operating.
Data can be retained at 2.2 V when clock stops. When VDD is applied, the μPD17001 is reset by the built-in power-ON/resetting circuit.</td><td>–</td><td>–</td></tr>
<tr><td>41

42</td><td>VCOL Note 1

VCOH Note 1</td><td>Used as PLL local oscillation frequency input port.
<table>
<tr><th>Dividing system</th><th>Input pin</th><th>Input frequency (MHz)</th><th>Input voltage (Vp-p)</th></tr>
<tr><td>Direct dividing (MF)</td><td>VCOL</td><td>0.5-30</td><td>0.3</td></tr>
<tr><td>Pulse swallow (HF)</td><td>VCOL</td><td>5-40</td><td>0.3</td></tr>
<tr><td>Pulse swallow (VHF)</td><td>VCOH</td><td>9-130</td><td>0.3</td></tr>
</table></td><td>–</td><td>Input</td></tr>
<tr><td>44</td><td>CLKOUT</td><td>Clock output for external micro computer.
Outputs the same frequency as Xout.</td><td>CMOS push/pull</td><td>Low level output</td></tr>
<tr><td>45

46</td><td>XOUT Note 2

XIN Note 2</td><td>Connect quartz oscillator for system clock generation.</td><td>CMOS push/pull

–</td><td>–</td></tr>
<tr><td>47
48</td><td>EO0
EO1</td><td>Output from PLL frequency synthesizer charge pump. The phase of the local oscillation frequency is compared, and the result is output.</td><td>CMOS 3-state</td><td>High impedance</td></tr>
</table>

Notes 1. These pins are used as an AC amplifier input pote. The DC component should be cut off from the signal to be entered by a series-connected condenser.

2. Refer to **APPENDIX A: PRECAUTIONS IN CONNECTING QUARTZ OSCILLATOR.**

NOTES ON USING A GENERAL PURPOSE PORT

Port Register Data Set

The port registers (registers P0A to P1D) on data memory are used for reading input data or setting output data of each of the ports, Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, and Port 1D.

In this case, the POA_3 pin of Port 0A corresponds to the highest bit of port register P0A and the $P0A_0$ pin corresponds to the lowest bit.

These apply also to Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, and Port 1D.

Input/output Ports (Port 0A, Port 0B, and Port 1B)

(1) When each port is specified as an input port

By executing an instruction (the address of the port register is specified for m of SKT m, #i, or ADD r, m) for reading the contents of each port register in the data memory, the status of each port pin is used as the value of the port register.

When an instruction (specified for r of MOV m, #i or ADD r, m) for writing data to each port register is executed, the value is written to the output data latch circuit.

(2) When each port is specified as an output port

When an instruction for writing data to each port register is executed, the value is written to the output data latch circuit and is output from each pin.

When an instruction for reading the contents of each port register is executed, the content of output data latch are used as the value of the port register. However, for pins $P0A_0$/SDA and $P0A_1$/SCL, the pin status is read as it is when the contents of the port register are read and the status may be different from the output data.

At Power On Reset, CE Reset, or execution of a Clock Stop instruction, all of these pins are set for input ports. Since the contents of the output data latch circuit are undefined at Power On Reset, a Write instruction must be executed for the port register before setting data to the output port. Otherwise, undefined data is output. At CE Reset or execution of a Clock Stop instruction, the contents of the output data latch circuit do not change.

Output Ports (Port 0C, Port 1C, and Port 1D)

An output port is used for writing the value of the port register to the output data latch circuit by executing an instruction for writing data in a port register and outputting data from each pin.

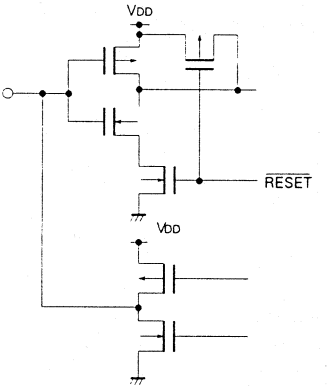
When a Read instruction is executed for a port register value, the port register value is set as the status of the output data latch circuit.

At Power On Reset, undefined data is output.

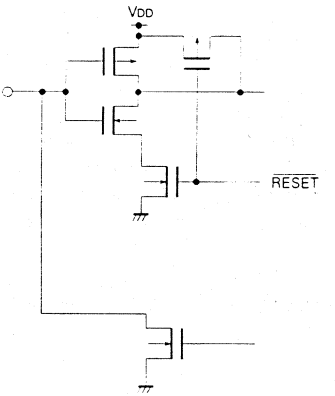
At CE Reset, the previous output data is kept at execution of a Clock Stop instruction.

PIN EQUIVALENT CIRCUITS

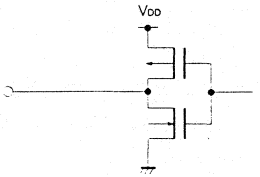
P0A ($P0A_2/\overline{SCK}$, $P0A_3$/SO)
P0B ($P0B_0$/SI, $P0B_1$, $P0B_2$, $P0B_3$)
P1B ($P1B_0$, $P1B_1$, $P1B_2$, $P1B_3$)
} (Input/output)



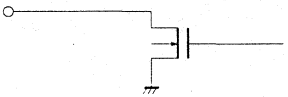
P0A ($P0A_0$/SDA and $P0A_1$/SCL) (Input/output)



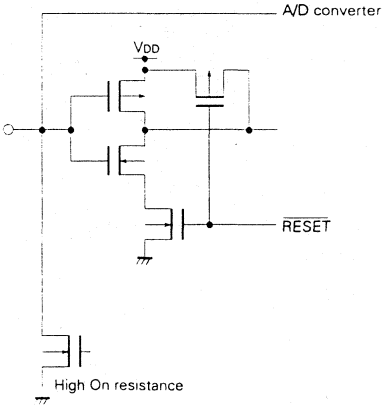
P0C ($P0C_0$, $P0C_1$, $P0C_2$, $P0C_3$)
P1C ($P1C_0$/CGP)
P1D ($P1D_0$, $P1D_1$, $P1D_2$, $P1D_3$) } (Output)



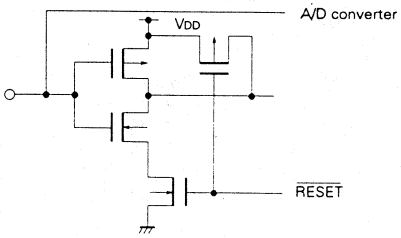
P1C ($P1C_1$/PWM_0, $P1C_2$/PWM_1, $P1C_3$/PWM_2) (Output)



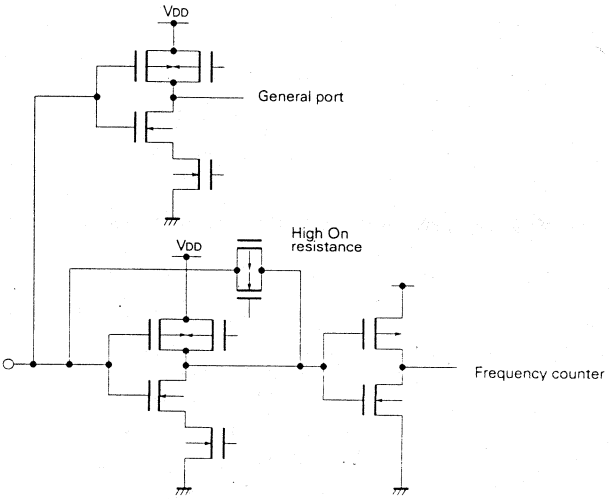
P0D ($P0D_0$/ADC_0, $P0D_1$/ADC_1, $P0D_2$/ADC_2, $P0D_3$/ADC_3) (Input)



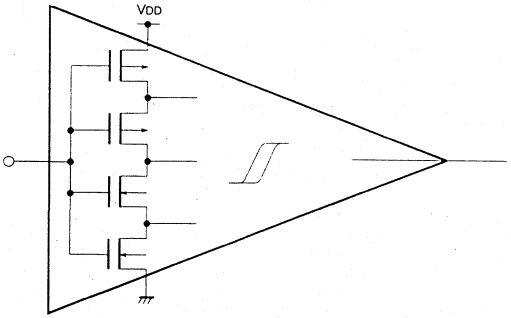
P1A (P1A0/ADC4, P1A1/ADC5) (Input)



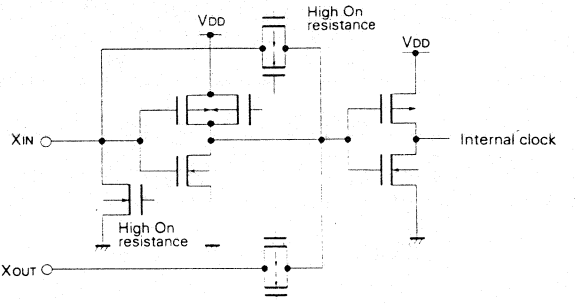
P1A (P1A2/AMIFC, P1A3/FMIFC) (Input)



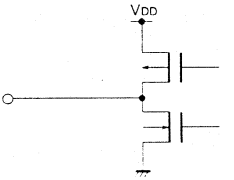
CE
INT } **(Hysteresis input)**



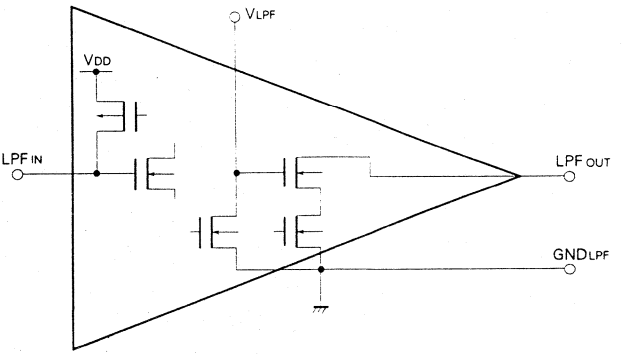
X_{OUT} (output), X_{IN} (input)



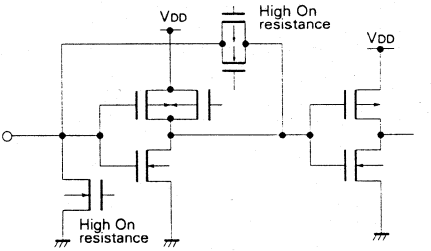
EO_1
EO_0 **(Output)**



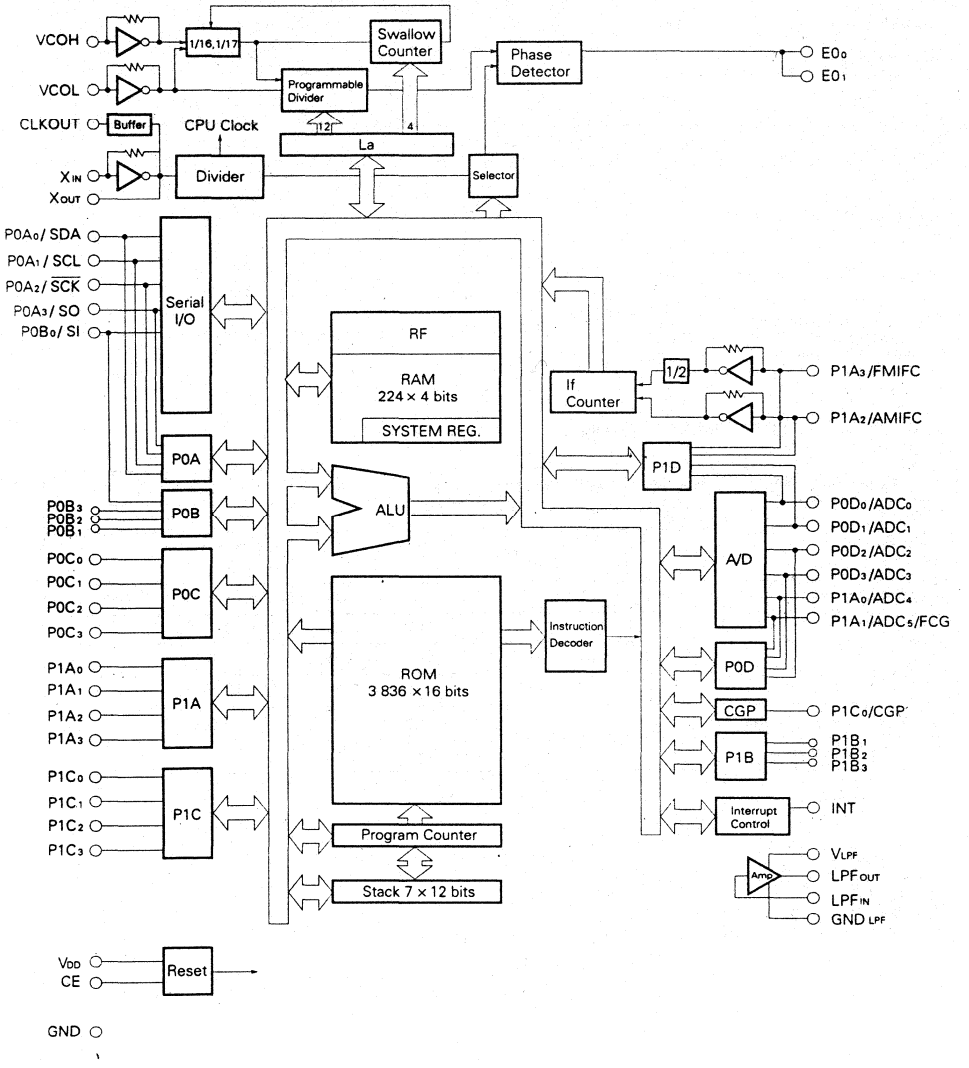
LPF_{IN} (input), LPF_{OUT} (output), V_{LPF}



VCOH
VCOL **(Output)**



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Unless Otherwise Specified, T_a = 25 ±2 °C)

Source Voltage	V_{DD}		−0.3 - + 6.0	V
Input Voltage	V_I		−0.3 - V_{DD} + 0.3	V
Output Voltage	V_O	Excluding $P1C_1$ - $P1C_3$, $P0A_0$, $P0A_1$ and LPF_{OUT}	−0.3 - V_{DD} + 0.3	V
Output Withstand Voltage	V_{BDS1}	$P1C_1$ - $P1C_3$, LPF_{OUT}	16.0	V
	V_{BDS2}	$P0A_0$, $P0A_1$	V_{DD} + 0.3	V
High Level Output Current	I_{OH}	1 pin	−12	mA
		All pins	−20	mA
Low Level Output Current	I_{OL}	1 pin	12	mA
		All pins	20	mA
Operating Temperature	T_{opt}		−40 - + 85	°C
Storage Temperature	T_{stg}		−55 - + 125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Source Voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU are operating
	V_{DD2}	3.5	5.0	5.5	V	PLL is OFF and CPU is operating
Data Holding Voltage	V_{DDR}	2.2		5.5	V	Quartz oscillator is OFF
Source Voltage Rise Time	t_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Amplitude	V_{in1}	0.5		V_{DD}	V_{P-P}	VCOL, VCOH
	V_{in2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output Withstand Voltage	V_{BDS}			14.0	V	$P1C_1$ - $P1C_3$, LPF_{OUT}
Operating Temperature	T_{opt}	−40		+85	°C	

DC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL are operating
	V_{DD2}	3.5	5.0	5.5	V	CPU is operating and PLL is OFF
Source Current	I_{DD1}		1.2	2.4	mA	CPU is operating and PLL is OFF. X_{IN} pin Sine wave input (f_{in} = 4.5 MHz, V_{in} = V_{DD}), T_a = 25 °C
	I_{DD2}		0.45	0.90	mA	CPU is operating, PLL is OFF, and HALT instruction is used (20 instructions executed per 1 ms). X_{IN} pin Sine wave input (f_{in} = 4.5 MHz, V_{in} = V_{DD}), T_a = 25 °C
Data Holding Voltage	V_{DDR1}	3.5		5.5	V	Power failure detection by timer FF. Quartz oscillator ON
	V_{DDR2}	2.2		5.5	V	Power failure detection by timer FF. Quartz oscillator OFF
	V_{DDR3}	2.0		5.5	V	Data memory (RAM) holding
Data Holding Current	I_{DDR1}		2	15	μA	Quartz oscillator OFF. T_a = 25 °C
	I_{DDR2}		2	10	μA	Quartz oscillator OFF. V_{DD} = 5.0 V, T_a = 25 °C
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$, $P1A_0$ - $P1A_3$, $P1B_0$ - $P1B_3$, CE, INT
	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$ - $P0D_3$
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD}	V	$P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$, $P0D_0$ - $P0D_3$, $P1A_0$ - $P1A_3$, $P1B_0$ - $P1B_3$, CE, INT
High Level Output Current	I_{OH1}	−1.0	−5.0		mA	$P0A_2$, $P0A_3$, $P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P1B_0$ - $P1B_3$, $P1C_0$, $P1D_0$ - $P1D_3$ V_{OH} = V_{DD} −1 V
	I_{OH2}	−1.0	−4.0		mA	EO_0, EO_1 V_{OH} = V_{DD} − 1 V
Low Level Output Current	I_{OL1}	1.0	7.0		mA	$P0A_2$, $P0A_3$, $P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P1B_0$ - $P1B_3$, $P1C_0$, $P1D_0$ - $P1D_3$ V_{OL} = 1 V
	I_{OL2}	1.0	3.5		mA	EO_0, EO_1 V_{OL} = 1 V
	I_{OL3}	1.0	2.0		mA	$P1C_1$ - $P1C_3$ V_{OL} = 1 V
	I_{OL4}	1.0	10.0		mA	$P0A_0$, $P0A_1$ V_{OL} = 1 V

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
High Level Input Current	I_{IH1}	0.1	0.8		mA	VCOH pull-dow $V_{IH} = V_{DD}$
	I_{IH2}	0.1	0.8		mA	VCOL pull-down $V_{IH} = V_{DD}$
	I_{IH3}	0.1	1.3		mA	X_{IN} pull-down $V_{IH} = V_{DD}$
	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ - $P0D_3$ pull-down $V_{IH} = V_{DD}$
Output Off Leak Current	I_{L1}			500	nA	$P0A_0$, $P0A_1$ $V_{OH} = V_{DD}$
	I_{L2}			500	nA	$P1C_1$ - $P1C_3$ $V_{OH} = 14$ V
	I_{L3}			±100	nA	EO_0, EO_1 $V_{OH} = V_{DD}$ $V_{OL} = 0$ V

AC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

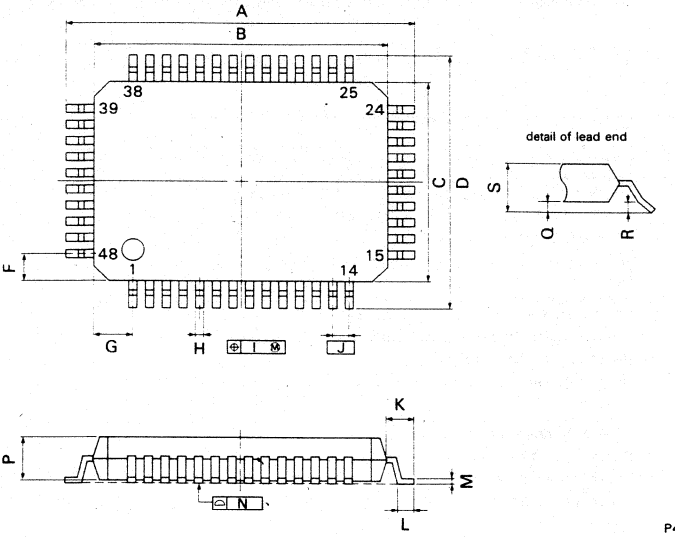
CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{in1}	0.5		30	MHz	VCOL MF mode. Sine wave input. V_{in} = 0.3 V_{P-P}
	f_{in2}	5		40	MHz	VCOL HF mode. Sine wave input. V_{in} = 0.3 V_{P-P}
	f_{in3}	9		130	MHz	VCOH Sine wave input V_{in} = 0.3 V_{P-P}
	f_{in4}	0.1		1	MHz	AMIFC Sine wave input V_{in} = 0.3 V_{P-P}
	f_{in5}	5		15	MHz	FMIFC Sine wave input V_{in} = 0.3 V_{P-P}
AD Converting Resolution				6	bit	
AD Converting Overall Error			±1	±1.5	LSB	T_a = −10 - +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source Current	I_{DD3}		15		mA	CPU and PLL are operating. VCOH Sine wave input f_{in} = 130 MHz, V_{in} = 0.5 V_{P-P}, V_{DD} = 5 V, T_a = 25 °C

PACKAGE DIMENSION

48PIN PLASTIC QFP (10×14)



P48GH-80-2A5-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$16.8^{\pm 0.4}$	$0.661^{+0.017}_{-0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{\pm 0.008}$
C	$10.0^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
D	$12.8^{\pm 0.4}$	$0.504^{\pm 0.016}$
F	1.4	0.055
G	1.8	0.071
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.4^{\pm 0.2}$	$0.055^{\pm 0.008}$
L	$0.6^{\pm 0.2}$	$0.024^{+0.008}_{-0.009}$
M	$0.20^{+0.10}_{-0.05}$	$0.079^{+0.068}_{-0.073}$
N	0.15	0.006
P	$2.2^{\pm 0.1}$	$0.087^{+0.004}_{-0.005}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	2.5 MAX.	0.099 MAX.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17001GH

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	IR30-162
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	VP15-162
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	WS60-162
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

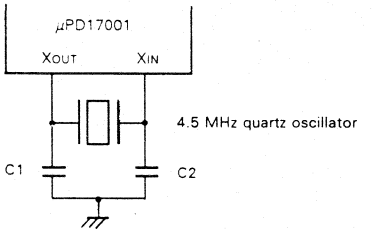
*: Exposure limit before soldering after dry-pack package is opened. Storage conditions: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

APPENDIX A PRECAUTIONS IN CONNECTION OF QUARTZ OSCILLATOR

When using a system clock oscillation circuit, observe the following precautions of the shaded portion shown below to avoid averse effects of wiring capacitance, etc.

- Use as short wiring as possible.
- Do not use unnecessarily large capacitances for C1 and C2.
  This may result in deterioration of the oscillation start characteristics or increase in power dissipation.
- The oscillation frequency adjusting trimmer condenser is generally connected to the X_{IN} pin. Note, however, that the oscillation stability may differ depending on the quartz used. This should therefore be evaluated based on the quartz oscillator actually used.
- If an emulation probe is connected to the X_{OUT} or X_{IN} pin, accurate adjustment of oscillation frequency may be disabled due to the capacitance of the probe. In such a case, adjust while measuring the LCD drive waveform (125 Hz) or VCO oscillation frequency.



BUILT-IN EPROM, PRESCALER

μPD17P001 is a 4 bits CMOS microcomputer for Digital Tuning System implemented EPROM, prescaler (operational frequency up to 150 MHz), PLL frequency synthesizer and IF counter on chip.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

As PLL frequency synthesizer can apply pulse swallow method high performance tuner is easily constructed by selecting high reference frequency like 50 kHz or 100 kHz.

In addition, station detect is realized by counting intermediate frequency of tuner using built-in 16 bits IF counter.

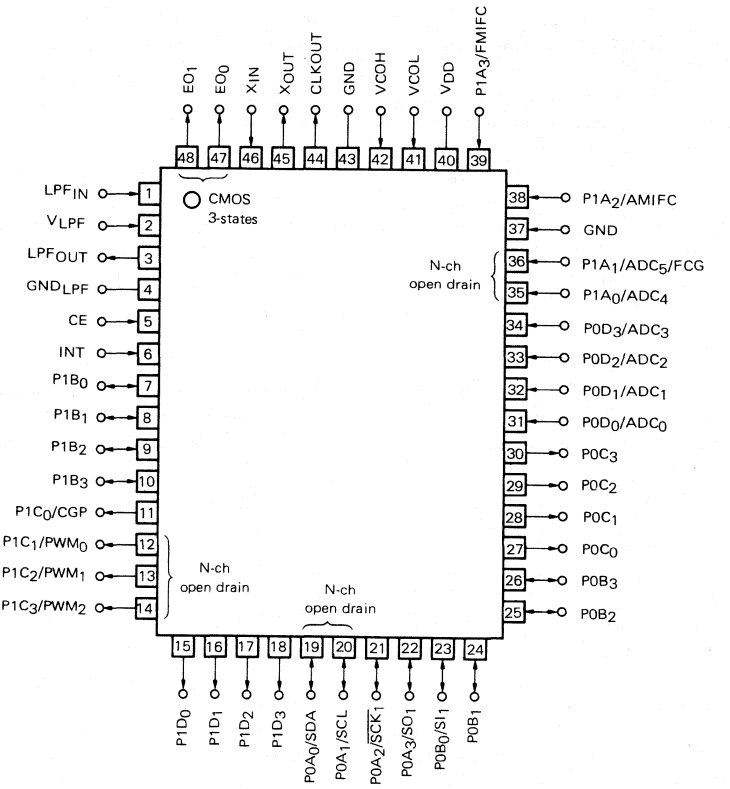
μPD17P001 is the most suitable for evaluating the program of μPD17001 or for producing a few products because μPD17P001 is built-in EPROM.

As system development support tools of μPD17P001, IE-17K (In Circuit Emulator) and AS17K (assembler) are prepared.

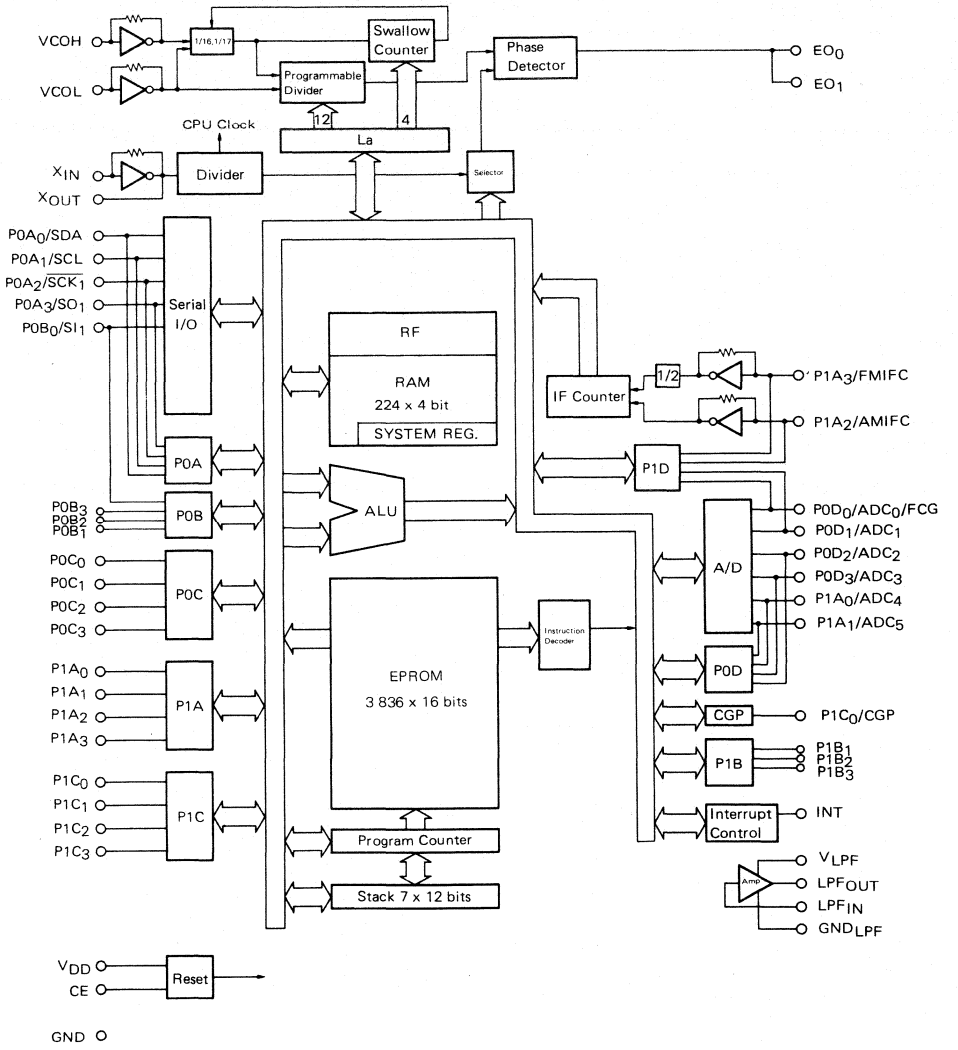
FEATURES

- 4 bits microcomputer for Digital Tuning System
- program memory (EPROM)
  : 8 K bytes (16 bits x 3836 steps)
- data memory (RAM)
  : 224 words (4 bits x 224 words)
- stack level: 7
- 35 types of simple instruction sets
- decimal operation
- instruction execution time: 4.44 μs
  (with 4.5 MHz crystal oscillator)
- built-in PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequencies can be selected by software.
  1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
- built-in amplifier for LPF (Low pass filter)
- built-in IF counter (AMIFC, FMIFC)
- built-in 8 bits serial interface
  1 system 2 channels: 3 wire or 2 wire system
- built-in D/A converter: 8 bits x 3 (PWM output)
- built-in A/D converter: 6 bits x 6
- built-in discharge detection circuit and power on reset circuit
- interrupt
  external interrupt: 2 channels
  internal interrupt: 3 channels
- various I/O ports
  input/output ports: 12 lines
  input ports : 8 lines
  output ports : 12 lines
- built-in CGP (Clock Generator Port)
- single power supply (5 V±10 %)
- CMOS low power consumption
- Product of mask ROM version: μPD17001
- 48-pin plastic QFP

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



DIGITAL TUNING SYSTEM HARDWARE BUILT-IN 4-BIT SINGLE CHIP MICRO CONTROLLER

μPD17003A is a 4-bit single chip CMOS micro controller which contains digital tuning system hardware.

17K architecture is used for CPU, data and memory manipulations and various types of operations, and peripheral hardware control can be performed directly by one instruction.

Peripheral hardware devices include a prescaler which operates up to 250 MHz, PLL frequency synthesizer, LPF (Low Pass Filter) amplifier, and frequency counter for digital tuning in addition to various types of input/output ports, LCD controller/driver, A/D converter, D/A converter (PWM output), and clock generator ports.

Consequently, a high performance digital tuning system with a variety of functions can be constructed using only one chip. μPD17005 (note) is available as the product which is pin-compatible with μPD17003A and whose memory size (ROM) is extended. One-time PROM version μPD17P005 (note) is available as μPD17005, and μPD17P005 can be used for program evaluation of μPD17003A at small volume production.

FEATURES

- Using 17K architecture
- Program memory (ROM)
  8K bytes (3836 steps x 16 bits)
- General purpose data memory (RAM)
  320 nibble (320 words x 4 bits)
- Instruction execution time
  4.44 μs (using 4.5 MHz quarts oscillator)
- Decimal operation enabled
- Table reference enabled
- Built-in PLL frequency synthesizer hardware
- Dual modules prescaler (250 MHz Max.), programmable divider, phase comparator, charge pump, and LPF amplifier
- Various types of peripheral hardware
  General purpose input/output ports, LCD controller/driver, serial interface, A/D converter, D/A converter (PWM output), clock generator, ports, and frequency counter
- Various types of interrupt
  External interrupt : 2 channels
  Internal interrupt : 3 channels
- Power On Reset, resetting by a CE pin, and built-in blackout detection circuit
- CMOS low power consumption
- Power supply voltage 5 V ±10%

ORDERING INFORMATION

Order Code	Package
μPD17003AGF-XXX-3B9	80-pin plastic QFP (14 x 20)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

In case of using this interface mode note the following:

Duties when using I2C bus system

Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

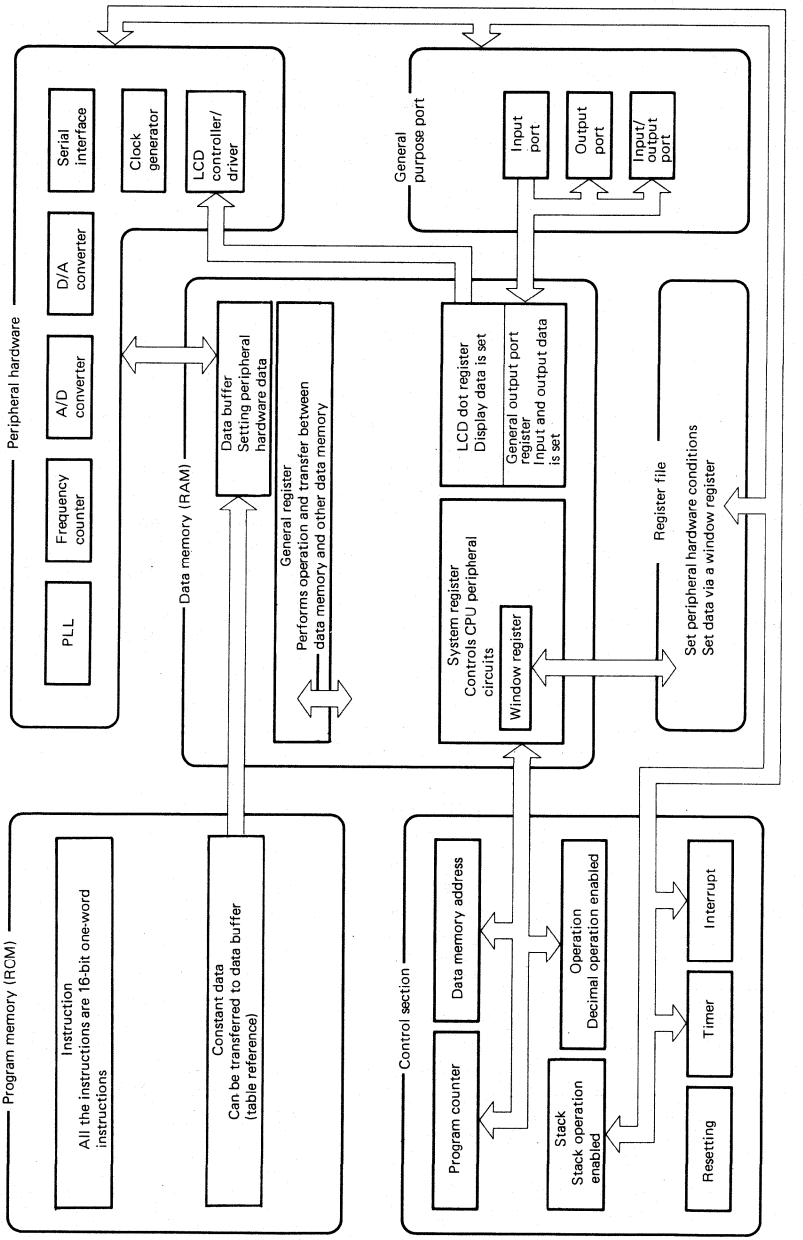
Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

μPD17003A FUNCTION OUTLINE

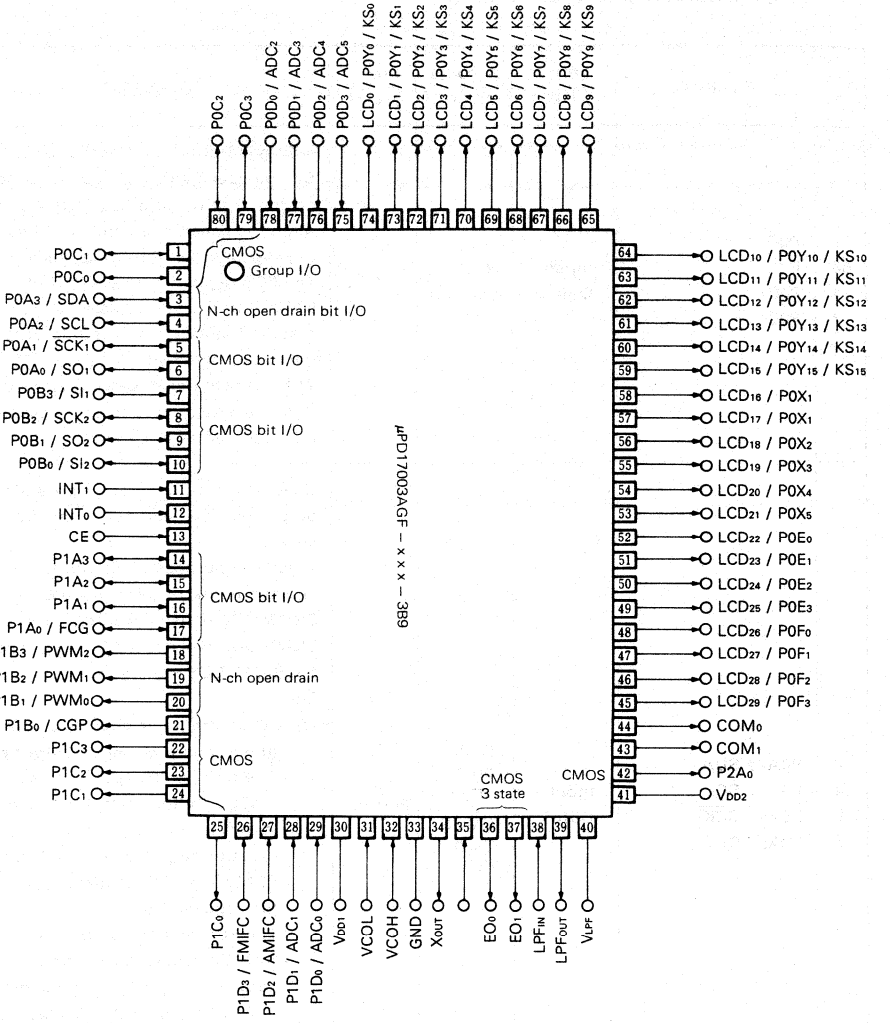
Item	Function
Program memory (ROM)	• 8K bytes (3836 steps x 16 bits) Table reference area: up to 256 steps x 16 bits
General data memory (RAM)	• 320 nibble (320 words x 4 bits) Data buffer: 4 nibbles General register: 16 nibbles
System register	• 12 nibbles
Register file	• 33 nibbles (control register)
General port register (including LCD dot data register)	• 24 nibbles
Instruction execution time	• 4.44 μs (using 4.5 MHz quarts oscillator)
Stack level	• 7 levels (stack operation enabled)
General purpose port	• Input/output port: 16 • Input ports: 8 • Output ports: 9 (+30: LCD segment pin)
Clock generator port (CGP)	• 1 VDP (Variable Duty Pulse) and SG (Signal Generator) functions
LCD controller/driver	• 30 segments, 2 common 1/2 duty, 1/2 bias, frame frequency 250 Hz, driving voltage V_{DD}, segment pin used also for key source: 16 ports All of the 30 ports can be used as output ports (4 ports, 4 ports, 6 ports, and 16 ports can be set independently)
Serial interface	• Two types (3 channels) 8-bit 3-wire system: 2 channels 8-bit 2-wire system: 1 channel
D/A converter	• 8 bits x 3 (PWM output and output resisting pressure 16 V Max.)

Item		Function
A/D converter		• 6 bits x 6 (consecutive comparison method by software)
Interrupt		• 5 channels (maskable interrupt) External interrupt: 2 channels (INT_0 pin and INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, and frequency counter)
Timer		• Two types Timer carry FF (1, 5, 100, 250 ms) Timer interrupt (1, 5, 10, 250 ms)
Reset		• Power On Reset (at power supply connection) • Resetting by CE pin (CE pin Low – High) • Blackout detection function
PLL frequency synthesizer	Division method	• 2 types Direct division method (VCOL pin 20 MHz Max.) Pulse swallow method (VCOL pin 40 MHz Max.) (VCOH pin 250 MHz Max.)
	Reference frequency	• 12 types are selected by the program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	• Two independent error output
	Phase comparator	• Unlocking can be detected by a program Unlocking FF delay time can selected
	LPF amplifier	• CMOS operation amplifier output resisting pressure 16 V Max.
Frequency counter		• Frequency test $P1D_3$ / FMIFC pin 5 to 15 MHz $P1D_2$ / AMIFC pin 0.1 to 1 MHz • External gate width test $P0A_1$ / FCG pin
Power supply voltage		5 V ±10%
Package		80-pin plastic QFP

CONCEPT OF μPD17003A



PIN CONFIGURATION (Top View)



1. PIN FUNCTIONS

1.1 EXPLANATION ON EACH PIN FUNCTION

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
79 80 1 2	$P0C_3$ $P0C_2$ $P0C_1$ $P0C_0$	Input/ Output	CMOS Push-Pull	Port 0C	4-bit general purpose output port. Can be specified as an input or output port in 4-bit units (group I/O). Input/ output is specified by the P0CGPIO register (address 27H) of a register file. The P0C register (address 27H of BANK0) of the port register is used for reading input data and setting output data. At Power On Reset, Clock Stop instruction execution, or CE Reset, these pins are specified as input ports.
3 4 5 6	$P0A_3$ / SDA $P0A_2$ / SCL $P0A_1$ / $\overline{SCK_1}$ $P0A_0$ / SO_1	Input/ Output	N-ch open drain CMOS Push-Pull	Port 0A	Used as a 4-bit general purpose input/ output port and also for serial interface. A general purpose input/output port and serial interface is switched by the SIO1MODE register (address 08H) and SIO2MODE register (address 02H) of the SIO1MODE register of the register file. **(1) When the pin is used as a 4-bit general purpose input/output port** The port can be specified as an input or output port in bit units (bit I/O). Input or output is specified by the P0ABIO register (address 35H) of the register file. The P0A register (address 70H of BANK0) is used for reading input data and output data and setting the port register. Since $P0A_3$ / SDA, and $P0A_2$ / SCL pins are N-ch open drain output, pull-up resistance is required in the external section.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
3 4 5 6	$P0A_3$ / SDA $P0A_2$ / SCL $P0A_1$ / $\overline{SCK_1}$ $P0A_0$ / SO_1	Input/ Output	N-ch open drain CMOS Push-Pull	Port 0A	(2) **When the pins are used for serial interface** Two types of serial interfaces are available, serial interface 1 and serial interface 2 including Port 0B (pin numbers 7 to 10). Serial interface 1 and serial interface 2 can be used concurrently. Two channels of a 2-wire system and 3-wire system can be used for serial interface 1 and one channel of a 3-wire system can be used for serial interface 2. When using serial interface 1, specify pins from the SIO1MODE register of the register file and when using serial interface 2, specify pins using SIO2MODE register. The function of each pin is listed below.

Pin name	Function	Operating mode	
$P0A_3$ / SDA	Data input/ output	2-wire	Serial interface 1
$P0A_2$ / SCL	Clock input/ output		
$P0A_1$ / $\overline{SCK_1}$	Clock input/ output	3-wire	
$P0A_0$ / SO_1	Data output		
$P0B_3$ / SI_1	Data input		

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>3
4
5
6</td><td>P0A3 / SDA
P0A2 / SCL
P0A1 / $\overline{SCK_1}$
P0A0 / SO1</td><td>Input/ Output</td><td>N-ch open drain
CMOS Push-Pull</td><td>Port 0A</td><td>
<table>
<tr><th>Pin name</th><th>Function</th><th colspan="2">Operating mode</th></tr>
<tr><td>P0B2 / $\overline{SCK_2}$</td><td>Clock input/ output</td><td rowspan="3">3-wire</td><td rowspan="3">Serial interface 2</td></tr>
<tr><td>P0B1 / SO2</td><td>Data output</td></tr>
<tr><td>P0B0 / SI2</td><td>Data input</td></tr>
</table>
Since pins P0A3 / SDA and P0A2 / SCL are N-ch open drain, Pull-Up resistance is required externally.
At Power On Reset, Clock Stop instruction execution, and CE Reset, all of these pins are specified as input ports of general purpose input/output ports.
</td></tr>
<tr><td>7
8
9
10</td><td>P0B3 / SI1
P0B2 / $\overline{SCK_2}$
P0B1 / SO2
P0B0 / SI2</td><td>Input/ Output</td><td>CMOS Push-Pull</td><td>Port 0B</td><td>Used for 4-bit general purpose input/ output ports and also for serial interface
The SIO1MODE register (address 08H) or SIO2MODE register (address 02H) of the register file are used for switching the function as general purpose input/ output port to serial interface or vice versa.
(1) When using the pins as 4-bit general purpose input/output ports
The pins can be specified as input or output ports in bit units (bit I/O).
Input or output is specified by the P0BBIO register (address 35H) of the register file.
The P0B register (address 71H of BANK0) of the port register is used for reading input data and setting output data.</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
7 8 9 10	$P0B_3$ / SI_1 $P0B_2$ / $\overline{SCK_2}$ $P0B_1$ / SO_2 $P0B_0$ / SI_2	Input/ Output	CMOS Push-Pull	Port 0B	(2) **When the pins are used for serial interface** Two types of serial interface can be used including Port 0A (addresses 3 to 6), serial interface 1 and serial interface 2. See the explanation on Port 0A for the function of each pin. At Power On Reset, Clock Stop instruction execution, and CE Reset, all of these pins are specified as input ports of general purpose input/output ports.
11 12	INT_1 INT_0	Input	–	Interrupt	External interrupt request input pin. An interrupt request is issued from the input signal rising edge or falling edge of the input signal added to the pin. A rising edge and a falling edge can be specified by the INTEDGE register (address 1FH) of the register file using INT_0 pin and INT_1 pin independently. Even if an interrupt request is issued, interrupt cannot be accepted unless it is permitted (maskable interrupt). Types of interrupt permission include permission of all the interrupts by the EI instruction and permission of the interrupt of each INT_0 pin and INT_1 pin. Permission of interrupt for each pin is specified by the INTPM2 register (address 2FH) of the register file. When interrupt is permitted and when an interrupt request is issued, the interrupt is accepted. When interrupt is accepted, control of the program is passed to address 0005H in the case of interrupt by the INT_0 pin and address 0004H in the case of interrupt by the INT_1 pin. When interrupts for both INT_0 pin and INT_1 pin are allowed and when interrupts for both pins are issued, priority is given to the interrupt by INT_0 pin.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
11 12	INT_1 INT_0	Input	–	Interrupt	Even if an interrupt is not permitted, the issuing of an interrupt request can be checked using the INTREQ2 register (address 3FH) of the register file. When an interrupt function is not used, the input level of each pin can be detected by the INTJDG register (address 0FH) of the register file, and the pin can be used as a general purpose input port. At Power On Reset, Clock Stop Instruction execution, or CE Reset, the interrupt permission and interrupt request are reset.
13	CE	Input	–	Chip Enable	Input pins for device operation selection signal and reset signal. Device operation selection is to select the operation of the PLL frequency synthesizer and standby status as described below. (1) **Device operation selection** When the CE pin is at a High level, the PLL frequency synthesizer section can be operated. When the CE pin is at a Low level, the PLL frequency synthesizer section sets to a Disable state (operation prohibited) automatically in the device internal section. When the CE pin is at a Low level, the operation of quartz oscillation circuits in the internal section and CPU can be stopped by executing a Clock Stop instruction and data memory can be kept under a low consumption current (15 μA or less) (at CE pin = High level, the Clock Stop instruction operates as the NOP instruction). At execution of a Clock Stop instruction, the LCD controller/driver is set to a Display Off mode (LCD_0 to LCD_{29}, COM_0, COM_1 pin are Low level

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
13	CE	Input	–	Chip Enable	output) and general purpose input-output ports (Port 0A, Port 0B, Port 0C, and Port 1A) are used as input ports. (2) **Reset signal input** When the CE pin is changed from a Low level to High level, the device is reset by synchronizing with the Timer Carry FF of the internal section (CE Reset). When the device is reset, the program starts from address 0. In this case, the general purpose input/output ports are used as input ports. Since four types of internal Timer Carry FF, 1, 5, 100, and 250 ms can be selected, the time elapsing from when the pin is changed from the Low level to High level until the device is reset can be selected. However, if a Clock Stop instruction has been executed, the device is reset about 100 ms after the CE pin is changed to a High level. This pin does not accept a Low level or High level of less than 100 to 165 μs to prevent operation error due to noise. By using the CEJDG register (address 07H) of the register file, the input signal level of this pin can be detected. In this case also, the contents of the CEJDG register do not change at a Low level or High level of less than 110 to 165 μs. Shumit Trigger input with hysterisis feature is used for this pin. Note that a voltage higher than that of V_{DD} pin must not be supplied at power connection.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$ / FCG	Input Output	CMOS Push-Pull	Port 1A	Used as a 4-bit general purpose input/output port and also as an external gate counter ($P1A_0$ / FCG pin). The switching between the general purpose input/output port and an external gate counter is performed by the IFCMODE register (address 12H) of the register file. (1) **When the port is used as a 4-bit general purpose input/output port** The port can be specified as an input or output port in bit units (bit I/O). Input or output is specified by the P1A register (address 35H) of the register file. The P1ABIO register (address 70H of BANK1) of the port register is used for reading input data and setting output data. (2) **When the port is used as an external gate counter (FCG) ($P1A_0$ / FCG pin)** The counter counts the time from one rising edge to the next rising edge of the signal sent to the $P1A_0$ / FCG pin. A reference frequency (1 kHz, 100 kHz, 900 kHz) of the internal section is counted by a 16-bit counter. The external gate counter is specified by the IFCMODE register (address 12H) and IFCCONT register (address 23H) of the register file. The PIA_0 / FCG pin must be specified as the input port by the P1ABIO register (address 35H). Since the IFCMODE register and IFCCONT register control the frequency conter ($P1D_3$ / FMIFC and $P1D_2$ / AMIFC pins) and a clock

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$ / FCG	Input Output	CMOS Push-Pull	Port 1A	generator port ($P1B_0$ / CGP pin) also, an external gate counter, frequency counter, and a lock generator port cannot be used concurrently. At Power On Reset, execution of a Clock Stop instruction, and CE Reset, all of these pins are specified for input ports of the general input/output ports.
18 19 20 21	$P1B_3$ / PWM_2 $P1B_2$ / PWM_1 $P1B_1$ / PWM_0 $P1B_0$ / CGP	Output	N-ch open drain CMOS Push-Pull	Port 1B	Used as a 4-bit general output port, D/A converter ($P1B_2$ / PWM_2, $P1B_2$ / PWM_1, $P1B_1$ / PWN_0 pins), and a clock generator port ($P1B_0$ / CGP pin). The PWMMODE register (address 13H) of the register file is used for switching the general output port, D/A converter and a clock generator port. (1) **When the port is used as a 4-bit general purpose output port** The P1B register (address 71H of BANK1) of the port register is used for setting output data. The pins PIB_3 / PWM_2, PIB_2 / PWM_1, and PIB_0 / PWM_0 require Pull-UP resistance for N-ch open drain output. (Resisting pressure 16 V Max.) (2) **When the port is used as a D/A converter (PWM output) (pins $P1B_3$/ PWM_2, $P1B_2$ / PWM_1, and $P1B_1$ / PWM_0)** Each of pins $P1B_3$ / PWM_2, $P1B_2$ / PWM_1, and $P1B_1$ / PWM_0 can output an independent signal. A pulse width modulation (PWM) method is used as the output method, the frequency is 878.9 Hz (225 kHz/256) and duty is 0.25/256–255.25/256. (256 stages)

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>The duty must be set below the PWMR0 to PWMR2 registers (addresses from 05H to 07H) via a data buffer.
<table><tr><th>Function</th><th>Frequency</th><th>Duty</th></tr><tr><td>D/A converter</td><td>878.9 Hz</td><td>$\frac{0.25 + X}{256} \times 100\%$
X = 0 – 255</td></tr></table></td></tr>
<tr><td>18
19
20</td><td>P1B3 / PWM2
P1B2 / PWM1
P1B1 / PWM0</td><td>Output</td><td>N-ch open drain</td><td>Port 1B</td><td>These three pins are N-ch open drain output and the resisting pressure is 16 V Max.</td></tr>
<tr><td>21</td><td>P1B0 / CGP</td><td></td><td>CMOS Push-Pull</td><td></td><td>(3) When the port is used as a clock generator port (CGP) (P1B0 / CGP pin)
The P1B0 / CGP pin is set to a CGP mode by the PWMMODE register (address 13H) and IFCMODE register (address 12H) of the register file.
Two functions are available for a CGP mode, VDP (Variable Duty Pulse) and SG (Signal Generator).
The VDP function produces output in 64 stages, duty 2/67 – 65/67 at frequency 269 Hz.
The SG function produces output by dividing with the value of 4 to 130 (64 stages) using frequency 18 kHz as the reference frequency.
Both the VDP and SG functions set data as follows using the CGPR register (address 20H) via a data buffer.</td></tr>
</table>

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>18
19
20

21</td><td>P1B3 / PWM2
P1B2 / PWM1
P1B1 / PWM0

P1B0 / CGP</td><td>Output</td><td>N-ch open drain

CMOS Push-Pull</td><td>Port 1B</td><td>
<table>
<tr><th>Function</th><th>Frequency</th><th>Duty</th></tr>
<tr><td>VDP</td><td>269 Hz</td><td>$\frac{2+X}{67}$ x 100%
X = 0 – 63</td></tr>
<tr><td>SG</td><td>$\frac{18}{2(2+X)}$ kHz
X = 0 – 63</td><td>50%</td></tr>
</table>
At Power On Reset, execution of a Clock Stop instruction, these pins are specified as general purpose output ports.
At Power On Reset, undefined data is output. At execution of a Clock Stop instruction, the value of the general purpose output port is retained. At CE reset, the statuses (general purpose output port, A/D converter, CGP) which are set at that time are retained.
</td></tr>
<tr><td>22
23
24
24
25</td><td>P1C3
P1C2
P1C1
P1C0
P1C0</td><td>Output</td><td>CMOS Push–Pull</td><td>Port 1C</td><td>4-bit general purpose output port.
Output data is set via the P1C register (address 72H of BANK1) of the port register.
At Power On Reset, Undefined data is output.
At execution of a Clock Stop instruction or CE reset, the value which was output previously is kept.</td></tr>
<tr><td>26
27
28
29</td><td>P1D3 / FMIFC
P1D2 / AMIFC
P1D1 / ADC1
P1D0 / ADC0</td><td>Input</td><td>–</td><td>Port 1D</td><td>Used as a 4-bit general purpose input port, frequency counter (pins P1D3 / FMIFC and P1D2 / AMIFC), and also A/D converter (pins PID1 / ADC1 and PID0 / ADC0).
The IFCMODE register (address 12H) of the register file is used for switching the general purpose input port and A/D converter.</td></tr>
</table>

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>26
27
28
29</td><td>P1D3 / FMIFC
P1D2 / AMIFC
P1D1 / ADC1
P1D0 / ADC0</td><td>Input</td><td>–</td><td>Port 1D</td><td>The ADCCH register (address 14H) of the register file is used for switching the general input port and A/D converter.

(1) When the port is used as a 4-bit general purpose input port
The P1D register (address 73H of BANK1) of the port register is used for reading input data.
(2) When the port is used as a frequency counter (P1D3 / FMIFC and P1D2 / AMIFC)
Using the IFCMODE register of the register file, pins P1D3 / FMIFC and P1D2 / AMIFC can be used as frequency test pins. The following frequencies can be tested.

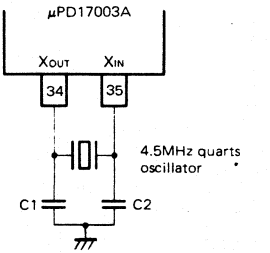
<table><tr><th>Input pin</th><th>Input frequency</th><th>Input oscillation</th></tr><tr><td>P1D3 / FMIFC</td><td>5 to 15 MHZ</td><td>0.3 Vp-p</td></tr><tr><td>P1D2 / AMIFC</td><td>0.1 to 1 MHz</td><td>0.3 Vp-p</td></tr></table>
As the test method, the frequency input within the gate time (1 ms, 4 ms, 8 ms, open) is counted by a 16-bit counter. However, the value divided by 2 is counted for the P1D3 / FMIFC pin.
At termination of the test (when the gate is closed), an interrupt request can be issued.
These functions can be used at detection of broadcast station by counting the intermediate frequency.
When the port is used as a frequency counter, cut the direct current section of the input signal with a condenser because an alternate current amplifier is used for input.</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
26 27 28 29	$P1D_3$ / FMIFC $P1D_2$ / AMIFC $P1D_1$ / ADC_1 $P1D_0$ / ADC_0	Input	–	Port 1D	The pin which was selected is used as an intermediate electric potential (about 1/2 V_{DD}). Pins which are not selected can be used as a general purpose input port. The alternate current ampilfier must be initialized by a program as required because it is not set to Disabled (prohibited state) even if the CE pin (pin number 13) is set to a Low level (if the amplifier is operating, the current consumed may increase the noise factor). Since the IFCMODE register also specifies an external gate counter ($P1A_0$ / FCG pin) and clock generator port ($P1B_0$ / CGP pin), the frequency counter, external gate counter, and clock generator port cannot be used concurrently. (3) **When the port is used as an A/D converter (pins $P1D_1$ / ADC_1 and $P1D_0$ / ADC_0)** The port can be used as an A/D converter of 6 bits by the ADCCH register (address 14H) of the register file. The A/D converter can use six channels by switching pins POD_3 / ADC_5 to POD_0 / ADC_2 (pin numbers from 75 to 78) in addition to pins $P1D_1$ / ACD_1 and $P1D_0$ / ACD_0. A consecutive comparison type is used as the conversion method and the reference voltage is created by dividing power supply voltage V_{DD} using the R string method.

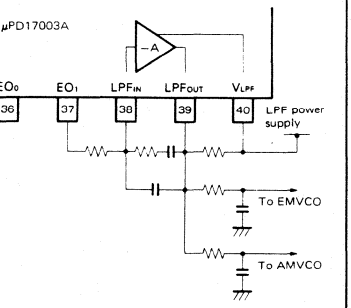
PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
26 27 28 29	$P1D_3$ / FMIFC $P1D_2$ / AMIFC $P1D_1$ / ADC_1 $P1D_0$ / ADC_0	Input	–	Port 1D	At Power On Reset, execution of a Clock Stop instruction, all these pins are specified as a general purpose input ports. At CE reset, the statuses (general purpose input port, frequency counter, and A/D converter) set at that time are retained.
30 41	V_{DD1} V_{DD2}	–	–	Power supply	Device power supply pin Voltage of 5 V ±10% is supplied at operation of CPU and peripheral functions. When only CPU is operating, the voltage can be reduced to 3.5 V. When the CE pin (pin number 13) is at a Low level and when a Clock Stop instruction is executed, oscillation of the quartz oscillator stops and a data set backup state is set. During the clock stop state, the voltage can be reduced to 2.2 V. When the voltage rises from 0 V to 4.5 V or when the voltage rises to 4.5 V again after decreasing to a degree less than 3.5 V (less than 2.2 V at clock stop), Power On reset is performed for the device. When Power On Reset is performed, the peripheral circuits, system registers, and register files are initialized and the program starts from address 0. The time spent from the voltage 0 V to 4.5 V must be within 500 ms. Resetting by a CE pin (CE Pin Reset) is also available in addition to Power On Reset described above for resetting a device. Since the values of timer carry FF if the register file differs between Power On Reset and CE Reset, blackout can be detected by detecting the timer carry FF.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT MODE</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>30
41</td><td>V_{DD1}
V_{DD2}</td><td>–</td><td>–</td><td>Power supply</td><td>A voltage higher than that of the V_{DD} pin must not be supplied to all the pins other than V_{DD} pins (V_{DD1} and V_{DD2}). In particular, care is necessary when the V_{DD} pin and the CE pin are started simultaneously. Latch-Up may occur. The V_{DD1} pin and V_{DD2} pin must be connected to an electrical potential. The V_{DD2} pin is used to supply power to quartz oscillation circuits (pins X_{IN} and X_{OUT}), error out circuits (pins EO_0 and EO_1), and low path filter circuits (pin LPF_{IN}). Pin V_{DD1} is used for supplying power to other sections.</td></tr>
<tr><td>31
32</td><td>VCOL
VCOH</td><td>Input</td><td>–</td><td>Local oscillation Low input

Local oscillation High input</td><td>Used for inputting local oscillation (VCO) frequency of PLL.
A direct division method (MF mode) and pulse swallow method (HF mode and VHF mode) are available as division methods and the method is specified by the PLLMODE register (address 21H) of the register file. The input pin, input frequency and division ratio by each division method are as follows.
<table>
<tr><th>Division method</th><th>Input pin</th><th>Input frequency (MHz)</th><th>Input voltage (Vp-p)</th><th>Division ratio</th></tr>
<tr><td>Direct division</td><td>VCOL</td><td>0.5 to 30</td><td>0.3</td><td>16 to $2^{16}-1$</td></tr>
<tr><td>Pulse swallow (HF)</td><td>VCOL</td><td>5 to 40</td><td>0.3</td><td>256 to $2^{16}-1$</td></tr>
<tr><td rowspan="2">Pulse swallow (VHF)</td><td rowspan="2">VCOH</td><td>9 to 150</td><td>0.3</td><td rowspan="2">256 to $2^{16}-1$</td></tr>
<tr><td>9 to 250</td><td>0.5</td></tr>
</table>
Since alternate current amplifier is used for input of these pins, the direct current section of the input signal must be cut using a condenser.
The pin specified by the PLLMODE register is used as an intermediate electrical potential (about 1/2 V_{DD}).</td></tr>
</table>

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
31 32	VCOL VCOH	Input	–	Local oscillation Low input Local oscillation High input	Pins which are not specified are pulled down in the internal section of the device. When PLL is disabled or when the CE pin is at a Low level, these pins are pulled down in the internal section of the device. At Power On Reset or execution of a Clock Stop instruction, a PLL Disabled state is set. At CE reset, the state specified by the PLLMODE register is set.
33	GND	–	–	Ground	Ground pin of the device
34 35	X_{OUT} X_{IN}	Output Input	CMOS –	Quartz oscillator	Quartz oscillator connection pin Connects a 4.5 MHz quarts oscillator as shown below.  The values of C1 and C2 are determined by the quartz oscillator which is used. When the values of C1 and C2 are increased to values which are too high, the oscillation activation feature may deteriorate or current consumption may increase. In general, the adjustment range of a trimmer condenser for oscillation frequency adjustment increases when the oscillator is connected to the X_{IN}

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
34 35	X_{OUT} X_{IN}	Output Input	CMOS –	Quartz oscillator	pin. However, the quartz oscillator which is actually used, including oscillation stabilizer, must be used for evaluation. An oscillation frequency cannot be adjusted accurately because of the problem at capacity, etc., if a probe is connected to the X_{OUT} pin or X_{IN} pin. Consequently, the frequency must be tested while testing the LCD driving wave form (125 Hz) or VCO oscillation frequency. Since the reference frequency of the timer of the internal section or PLL is used by dividing 4.5 MHz, if the value is shifted from 4.5 MHz, the values of the timer and reference frequency also shift in the same proportion.
36 37	EO_1 EO_0	Output	CMOS 3 states	Error out	Used as charge pump output pins of a PLL frequency synthesizer. When the value producing by dividing the local oscillation (VCO) frequency which is input to the VCOL pin (pin number 31) or VCOH pin (pin number 32) is higher than the reference frequency, a High level is output from these pins and when the value is lower than the reference frequency, a Low level is output. When the values match, floating occurs. A PLL frequency synthesizer can be structured by adding output of these pins to VCO (Voltage Controlled Oscillator) via LPF (Low Pass Filter). Either of the pins EO_1 and EO_2 can be used because the same signal is output. At a PLL Disabled state, these pins are set floating. That is, when the CE pin (pin number 13) is at a Low level or at Power On Reset, floating occurs.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
36 37	EO_1 EO_0	Output	CMOS 3 states	Error out	The PLL frequency synthesizer can detect a PLL unlocked state by the PLLULJDG register (address 05H) of the register file. Four types of time (0.5 μs, 1 μs, 2 μs, and Disable) can be selected as the delay time for detecting the PLL unlocated state using the PLULDLY register (address 15H) of the register file.
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output –	– N-ch open drain –	LPF Amplifier	Pins for a built-in CMOS operation amplifier for LPF (Low Pass Filter) Examples of an internal equivalent circuit of each pin and application of circuit are shown below. 

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
38	LPF_{IN}	Input	–	LPF Amplifier	Pull-Up resistance is required for the LPF_{OUT} pin because of N-ch open drain output. The resisting pressure is 16 V Max. A voltage higher than that of the LPF_{OUT} pin must be supplied to the V_{LPF} pin (16 V Max). At a PLL Disabled State, the LPF_{IN} pin is pulled up in the device internal section.
39	LPF_{OUT}	Output	N-ch open drain		
40	V_{LPF}	–	–		
42	$P2A_0$	Output	CMOS Push-Pull	Port 2A	1-bit general purpose output port. Output data is set via the P2A register (address 70H of BANK2) of the port register. At Power On Reset, undefined data is output. At execution of a Clock Stop instruction or CE reset, the value which was output previously is kept.
43	COM_1	Output	CMOS 3-value output	Common signal	Common signal output pins of the LCD controller/driver. The duty, bias, frame frequency, and driving voltage of the LCD controller/ driver are 1/2, 1/2, 250 Hz, and V_{DD} respectively. Display of up to 60 dots can be performed by the matrix with pins LCD_0 / $P0Y_0$ / KS_0 to LCD_{29} / $P0F_3$. Three types of voltages, 0, 1/2 V_{DD}, and V_{DD} are output from these pins. The light of the dot from which a potential difference of $\pm V_{DD}$ is produced between these pins and pins LCD_0 / $P0Y_0$ / KS_0 to LCD_{29} / $P0F_3$ comes on. When a Display Off mode is set by the LCDMODE register (address 10H of the LCDMODE register of the register file), a Low level is output at Power On Reset or execution of a Clock Stop instruction. At CE Reset, the state is kept if the mode is a Display On mode.
44	COM_0				

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	Used for segment signal output (pins LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0) of a LCD controller/driver, key source signal output (pins LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0), and also as a general output port (LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0). The LCDMODE register (address 10H) and LCDPORT register (address 11H) are used for outputting segment signals and key source signals, and switching general purpose output ports. (1) **When the pins are used for segment signal output of a LCD controller/driver (pins LCD_{29} / $P0F_3$ to LCD_0 / $P0Y_0$ / KS_0)** The duty, bias, and frame frequency (segment signal output 125 Hz) of a LCD controller/driver are 1/2, 1/2, and 250 Hz respectively. Display of up to 60 dots is enabled by using a matrix of these segment signal output pins, the COM_0 pin, and COM_1 pin (numbers 43 and 44). The light of the dot from which a potential difference of $\pm V_{DD}$ is produced between these segment signal output pins, and COM_0 and COM_1 pins comes on. Display data of an LCD controller/driver is set via LCD dot registers (addresses 60H to 6EH of BANK0). Data can also be set by LCD group registers (addresses 08H to 0FH) via a data buffer. A Display On mode and Display Off mode of a LCD controller/driver is set by the LCDMODE register of the register file.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	In Display Off mode, these segment signal output pins output a Low level. However, for pins which are specified for a general purpose output port by the LCDPORT register of the register file, data of the output port is output regardless of the display mode, On or Off. Sixteen pins from LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0 are also used for key source signal output of a key matrix as described in (2) and an LCD segment signal and a key source signal can be output concurrently. (2) **When the pins are used as a key source signal of a key matrix (pins LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0)** Using the LCDMODE register of the register file, sixteen pins from LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0 can be used as a key source output signal. A key source signal is output with a LCD segment signal in time sharing mode (key source signal output time 220 μs). When a key source signal is used, pins $P0D_3$ / ADC_5 to $P0D_0$ / ADC_2 (pin numbers 75 to 78) are used as the return signal input pins. Consequently, a key matrix of 16 key sources and 4 key input (up to 64) can be structured. A key source signal is output every 4 ms. Output data of a key source signal is set by the KSR register (address 42H) via a data buffer.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	When the LCD controller/driver is in Display Off mode (segment signal output = Low level) and when these pins are specified for a general purpose output port, a key source signal is not output. (3) **When the pins are used for a general purpose output port** Each pin can be specified for an output port as listed in the following table using the LCDPORT register (address 11H) of the register file.
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

Pin number	Pin name	Port name	Number bit
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Port 0F	4 bits
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$	Port 0E	4 bits
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$	Port 0X	6 bits
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0	Port 0Y	16 bits

Port 0F, Port 0E, Port 0X, and Port 0Y can be specified as general purpose output ports individually. Pins which are not specified for a general purpose output port can be used as LCD segment signal output pins.
Output data of each output port is set as listed below.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
45 to 48	LCD_{29} / $P0F_3$ to LCD_{26} / $P0F_0$	Output	CMOS Push-Pull	LCD segment signal	
49 to 52	LCD_{25} / $P0E_3$ to LCD_{22} / $P0E_0$				
53 to 58	LCD_{21} / $P0X_5$ to LCD_{16} / $P0X_0$				
59 to 74	LCD_{15} / $P0Y_{15}$ / KS_{15} to LCD_0 / $P0Y_0$ / KS_0				

Port name	Setting output data
Port 0F	• P0F register (address 6DH of BANK0) Used also for the LCDD13 register of the LCD dot register
Port 0E	• P0E register (Address 6BH of BANK0) Used also for the LCDD11 register of the LCD dot register
Port 0X	• P0XH and P0XL registers (Addresses 69H and 68H of BANK0) Used also for the LCDD9 and LCDD8 registers of the LCD dot register • Set by the P0X group register (0CH) via a data buffer
Port 0Y	• Set by a 0Y group register (42H) via a data buffer

At Power On Reset or execution of Clock Stop instruciton, all of these pins are specified for segment signal output and set to a Display Off mode. Consequently a Low level is output from all these pins.
At CE Reset, the statuses (segment signal output, key source signal output, and general purpose output port) which are set at that time are retained.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
75 76 77 78	$P0D_3$ / ADC_5 $P0D_2$ / ADC_4 $P0D_1$ / ADC_3 $P0D_0$ / ADC_2	Input	(Pull-Down Input with resistance)	Port 0D	Used for a 4-bit general purpose input port and also LCD segment key source signal return input, and also A/D converter input. The ADCCH register (address 14H) of the register file is used for switching the general purpose port and A/D converter. The pins $P0D_3$ / ADC_5 to $P0D_0$ / ADC_2 contain pull-down resistance so that they can be used as key return signal input pins of a key matrix. (1) **When the pins are used for general purpose input ports** Input data is read via the P0D register (address 72H of BANK0) of the port register. When pins are used for a general input port, the built-in pull down resistance is always set to ON. (2) **When the pins are used for key source signal return input of an LCD segment** When an LCD segment pins is used for key source, the built-in pull down resistance is set to ON only during output of a key source signal (220 μs) and the resistance is set to OFF during output of an LCD segment signal. The signals which were input to these pins during output of key source signals are fetched as key input data. Consequently, these pins must be used when a LCD segment signal output is used as the key source signal.

PIN NO.	SYMBOL	INPUT/ OUTPUT	OUTPUT MODE	PIN NAME	FUNCTION
75 76 77 78	$P0D_3$ / ADC_5 $P0D_2$ / ADC_4 $P0D_1$ / ADC_3 $P0D_0$ / ADC_2	Input	(Pull-Down Input with resistance)	Port 0D	(3) **When pins are used as an A/D converter** By the ADCCH register (address 14H) of the register file, the port can be used as a 6-bit A/D converter. A consecutive comparison method by a program is used as the A/D converter conversion method and the reference voltage is created by dividing power supply voltage V_{DD} using the R string method. An A/D converter can be used by switching six channels, pins $P1D_1$ / ADC_1 and $P1D_0$ / ADC_0 (pin numbers 28 and 29) in addition to pins from $P0D_3$ / ADC_5 to $P0D_0$ / ADC_2. The channel used is specified by the ADCCH register of the register file. The other five channels which are not specified for the A/D converter can be used as a general purpose input port. For the built-in pull-down resistance, only the pin which was set is set to OFF when it is set to A/D converter input by the ADCCH register. At Power On Reset or execution of a Clock Stop instruction, the pins are specified for a general purpose input port. At CE Reset, the status (general purpose input port, LCD segment key source, return input, and A/D converter) which are set at that point are retained.

1.2 NOTES ON USING A GENERAL PURPOSE PORT

1.2.1 Port Register Data Set

The port registers (registers P0A to P2A) on data memory are used for reading input data or setting output data of each of the ports, Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, and Port 2A.

In this case, the $P0A_3$ pin of Port 0A corresponds to the highest bit of port register P0A and the $P0A_0$ pin corresponds to the lowest bit.

These apply also to Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A. Output data of Port 0E, Port 0F, Port 0X, and Port 0Y is set by the LCD group register via the LCD dot register or a data buffer on the data memory.

1.2.2 Input/Output Ports (Port 0A, Port 0B, Port 0C, and Port 1A)

(1) **When each port is specified as an input port**

By executing an instruction (the address of the port register is specified for m of SKT m, #i, or ADD r, m) for reading the contents of each port register in the data memory, the status of each port pin is used as the value of the port register.

When an instruction (specified for r of MOV m, #i or ADD r, m) for writing data to each port register is executed, the value is written to the output data latch circuit.

(2) **When each port is specified as an output port**

When an instruction for writing data to each port register is executed, the value is written to the output data latch circuit and is output from each pin.

When an instruction for reading the contents of each port register is executed, the content of output data latch are used as the value of the port register. However, for pins P0A3/SDA and P0A2/SCL, the pin status is read as it is when the contents of the port register are read and the status may be different from the output data.

At Power On Reset, CE Reset, or execution of a Clock Stop instruction, all of these pins are set for input ports.

Since the contents of the output data latch circuit are undefined at Power On Reset, a Write instruction must be executed for the port register before setting data to the output port. Otherwise, undefined data is output. At CE Reset or execution of a Clock Stop instruction, the contents of the output data latch circuit do not change.

1.2.3 Output Ports (Port 1B, Port 1C, Port 0F, Port 0E, Port 0X, and Port 0Y)

An output port is used for writing the value of the port register to the output data latch circuit by executing an instruction for writing data in a port register and outputting data from each pin.

When a Read instruction is executed for a port register value, the port register value is set as the status of the output data latch circuit.

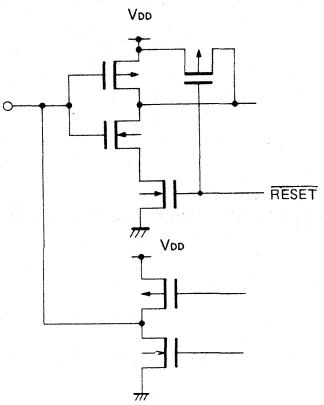
At Power On Reset, undefined data is output.

At CE Reset, the previous output data is kept at execution of a Clock Stop instruction. However, Port 0E, Port 0F, Port 0X, and Port 0Y output a Low level automatically at Power On Reset and at execution of a Clock Stop instruction.

1.3 PIN EQUIVALENT CIRCUITS

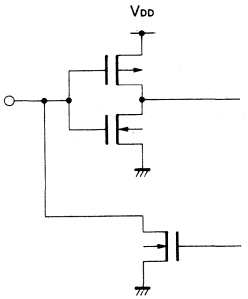
1.3.1 **P0A ($P0A_1$ / $\overline{SCK_1}$, $P0A_0$ / SO_1)**
P0B ($P0B_3$ / SI_1, POB_2 / $\overline{SCK_2}$, POB_1 / SO_2, $P0B_0$ / SI_2)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$) (*1)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, and $P1A_0$)

} (Input/output)

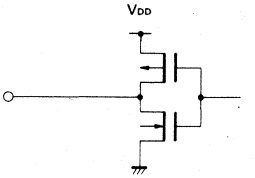


*1: The $\overline{RESET}$ signal is not provided to P0C.

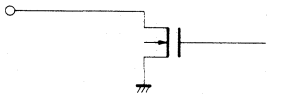
1.3.2 **P0A ($P0A_3$ / SDA and $P0A_2$ / SCL) (Input/Output)**



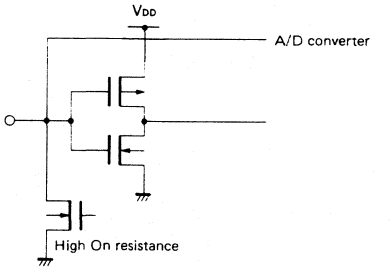
1.3.3 P1B (P1B0 / CGP)
P1C (P1C3, P1C2, P1C1, and P1C0)
P2A (P2A0)
LCD0 / P0Y0 / KS0 to LCD29 / P0F3
} (Output)



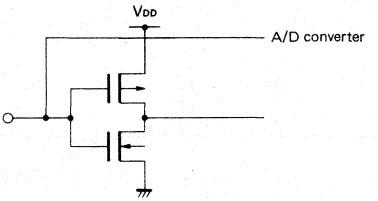
1.3.4 P1B (P1B3 / PWM2 and P1B2 / PWM1, and P1B1 / PWM0) (Output)



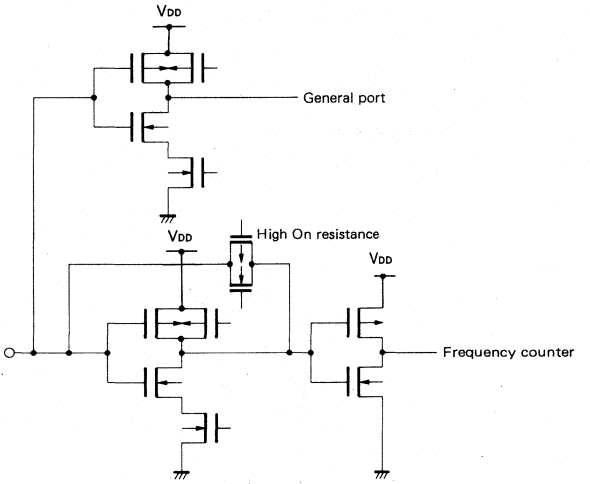
1.3.5 P0D (P0D3 / ADC5, P0D2 / ADC4, P0D1 / ADC3, and P0D0 / ADC2) (Input)



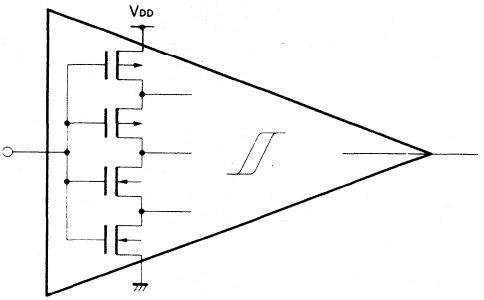
1.3.6 P1D (P1D1 / ADC1 and P1D0 / ADC0) (Input)



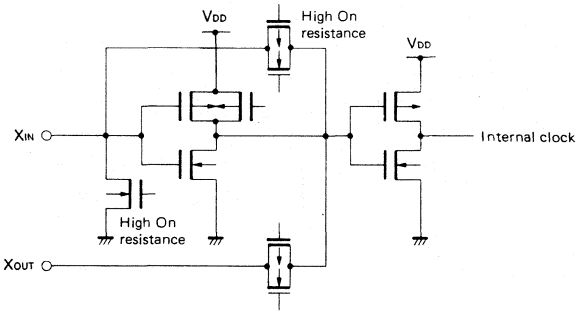
1.3.7 P1D (P1D3 / FMIFC, and P1D2 / AMIFC) (Input)



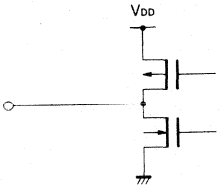
1.3.8 **CE**
INT1
INT0
(Schmit trigger input)



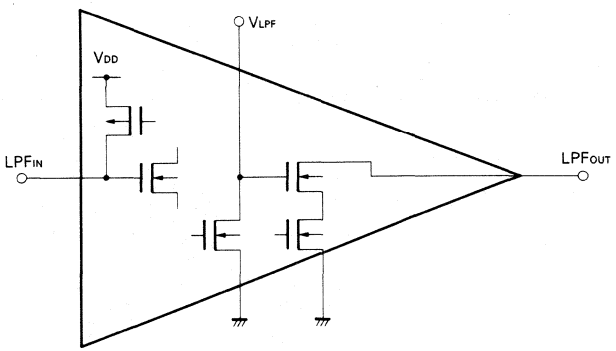
1.3.9 **XOUT (output) and XIN (input)**



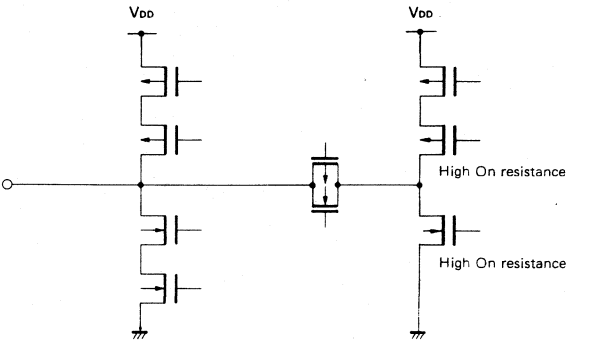
1.3.10 EO_1, EO_0 (Output)



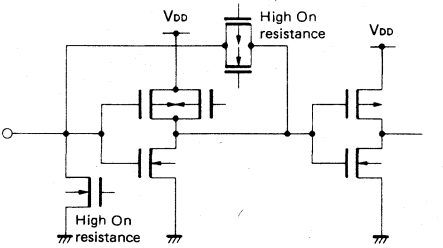
1.3.11 LPF_{IN} (input), LPF_{OUT} (output), and V_{LPF}



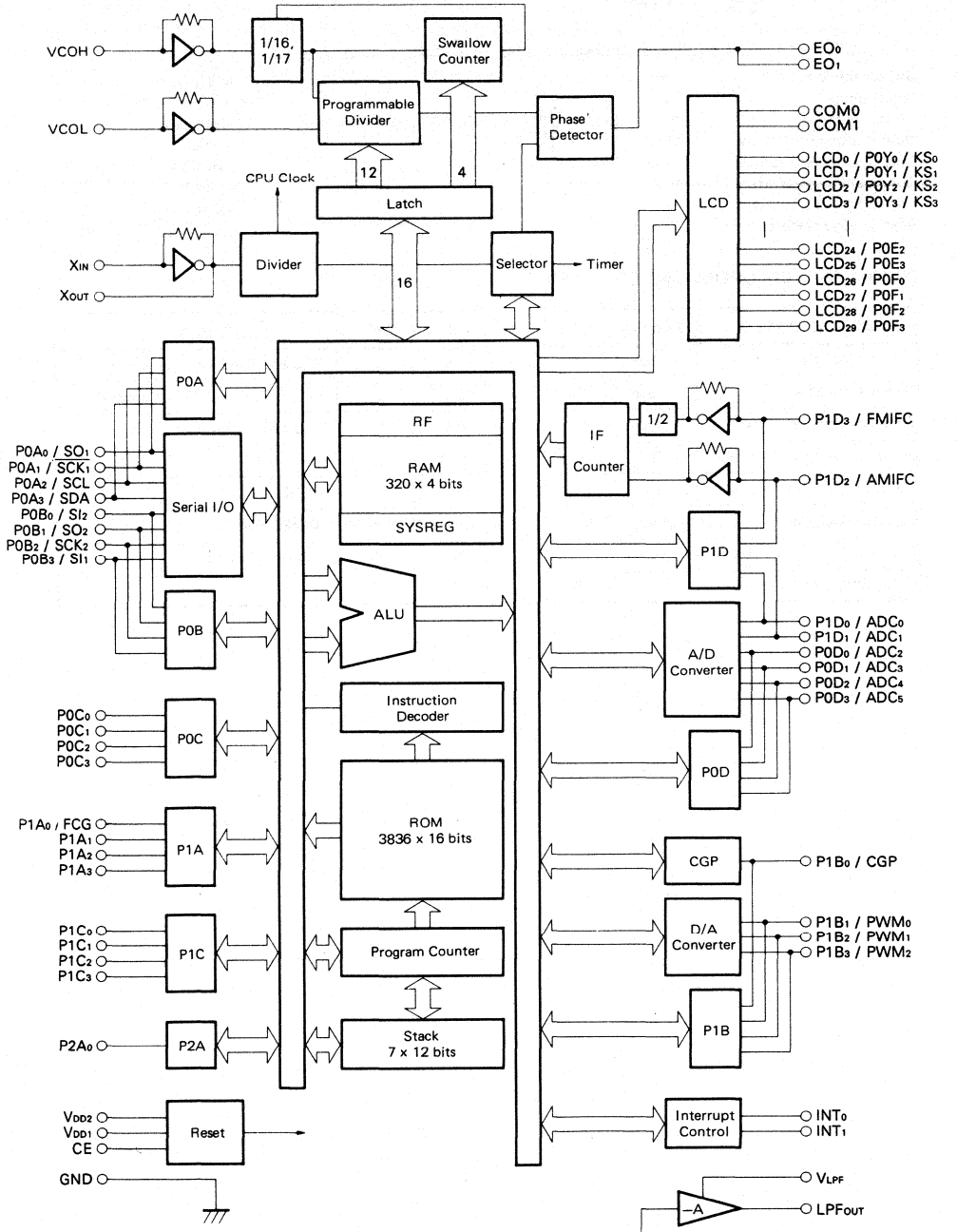
1.3.12 COM1 / COM0 (Output)



1.3.13 VCOH / VCOL (Input)



2. BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T_a = 25 ± 2 °C)

Source voltage	V_{DD}		−0.3 to +6.0	V
Input voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Excluding $P1B_1$ to $P1B_3$, $P0A_2$, $P0A_3$ and LPF_{OUT}	−0.3 to V_{DD} +0.3	V
Output withstand voltage	V_{BDS1}	$P1B_1$ to $P1B_3$, LPF_{OUT}	18.0	V
Output withstand voltage	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} +0.3	V
Output absorbing current	I_O		10.0	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Source voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU are operating
Source voltage	V_{DD2}	3.5	5.0	5.5	V	PLL is OFF and CPU is operating
Data holding voltage	V_{DDR}	2.2		5.5	V	Quartz oscillator OFF
Source voltage rise time	T_{rise}			500	ms	V_{DD} = 0 4.5 V
Input amplitude	V_{in1}	0.5		V_{DD}	V_{P-P}	VCOL, V COH
Input amplitude	V_{in2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output withstand voltage	V_{BDS}			16.0	V	P_1B_1 to $P1B_3$, LPF_{OUT}
Operating temperature	T_{opt}	−40		+85	°C	

DC CHARACTERISTICS (UNLESS OTHERWISE SPECIFIED, T_a = −40 to + 85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Source voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL are operating
Source voltage	V_{DD2}	3.5	5.0	5.5	V	CPU is operating and PLL is OFF.
Source current	I_{DD1}		1.2	2.4	mA	CPU is operating and PLL is OFF XIn pin Sinc wave Input (fin = 4.5 MHz, Vin, V_{DD}), T_a=25 °C
Source current	I_{DD2}		0.45	0.90	mA	CPU is operating, PLL is OFF, and HALT Instruction is used (20 Instructions executed per 1 ms). X↘ pin Sinc wave input fin 4.5 MHz, Vin = V_{DD}, T_a = 25°C
Data holding voltage	V_{DDR1}	3.5		5.5	V	Power failure detection by timer FF, quartz oscillator oscillating
Data holding voltage	V_{DDR2}	2.2		5.5	V	Power failure detection by timer FF, quartz oscillator not oscillating
Data holding voltage	V_{DDR3}	2.0		5.5	V	Data memory (RAM) holding
Data holding current	I_{DDR1}		2	15	μA	Quartz oscillator not oscillating T_a = 25°C
Data Holding current	I_{DDR2}		2	10	μA	Quartz oscillator not oscillating V_{DD} = 5.0 V T_a 25 °C
Intermediate level output voltage	V_{OM1}	2.3	2.5	2.7	V	COM_0 CGM_1 V_{DD} 5 V
High level input voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$, to PCA_3, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$, to $P1B_3$, $P1O_0$, to $P1O_3$, CE, INT_0, INT_1
High level input voltage	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$ to $P0O_3$
Low level input voltage	V_{IL}	0		0.2 V_{DD}	V	POA_0 to POA_3, POB_0 to POB_3, POC_0 to POC_3, POD_0, to POD_3, POA_0, to $P1C_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High level output current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1C_0$ to $P1A_3$, $P1B_0$ to $P1A_3$, V_{OH} = V_{DD} −1V
High level output current	I_{OH2}	−1.0	−4.0		mA	LOD_0 to LCI_{29} EO_0 EO_1 V_{OH} = V_{DD} − 1V
Low level output current	I_{OL1}	1.0	7.0		mA	$P0A_0$ to $P0A_3$, $P0B_0$, to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$, to $P1A_3$, $P1C_0$, to $P1C_3$, $P1B_0$, $P2A_0$ V_{OL} 1V
Low level output current	I_{OL2}	1.0	3.5		mA	LCD_0 to LCO_{29} EO_0 = $EI0_1$ V_{OL} 1 V
Low level output current	I_{OL3}	1.0	2.0		mA	$P1B_1$ to $P1B_3$ V_{OL} 1 V
Low level output current	I_{OL4}	1.0	10.0		mA	$P0A_2$ $P0A_3$ V_{OL} 1 V
High level output current	I_{IH1}	0.1	0.8		mA	VCOH pull-down V_{IH} = V_{DD}
High level input current	I_{IH2}	0.1	0.8		mA	VCOL pull-down V_{IH} = V_{DD}
High level input current	I_{IH3}	0.1	1.3		mA	P_{IN} pull-down V_{IH} = V_{DD}

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
High Level input current	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ to $P0D_3$ pull-down $V_{IH}=V_{DD}$
Output off leak current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ $V_{OH}=V_{DD}$
Output off leak current	I_{L2}			500	nA	$P1B_1$ to $P1B_3$, LPF_{OUT} $V_{OH}=16$ V
Output off leak current	I_{L3}			±100	nA	EO_0, EO_1 $V_{OH}=V_{DD1}$ $V_{OL}=0$V

AC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

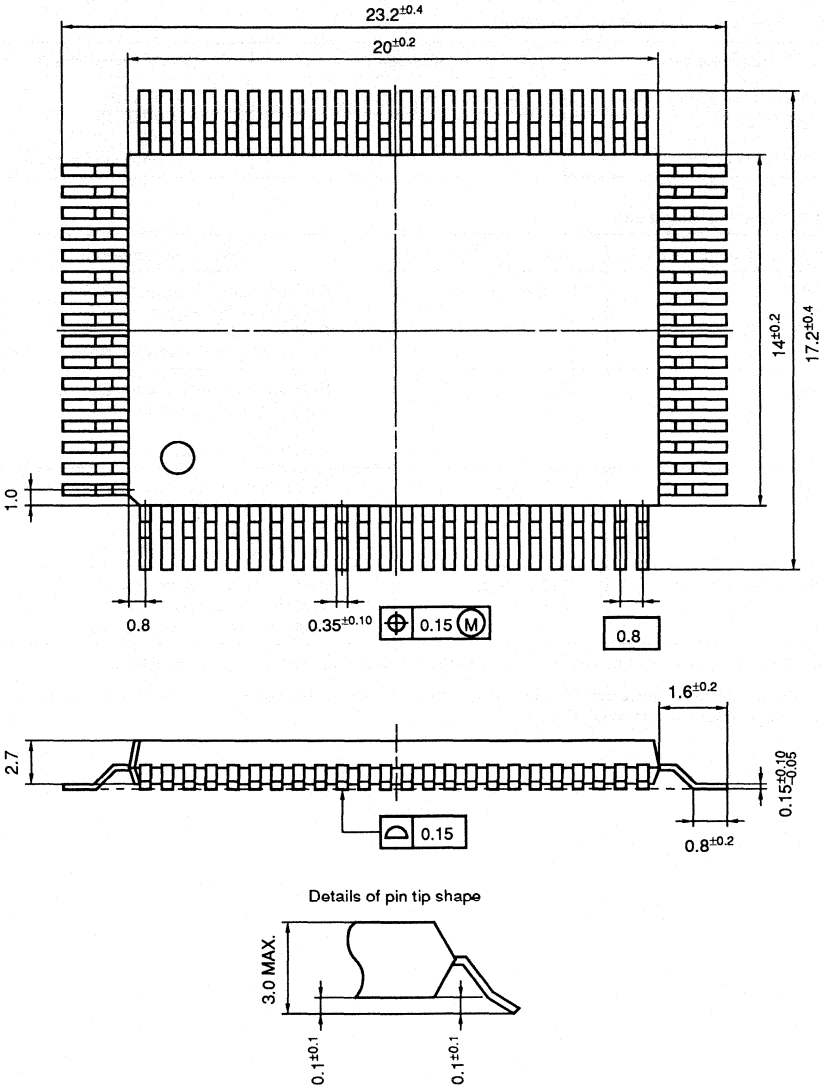
CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating frequency	f_{in1}	0.5		30	MHz	VCOL MF mode, sine wave input $V_{in}=0.3$ V_{P-P}
Operating frequency	f_{in2}	5		40	MHz	VCOL MF mode, sine wave input $V_{in}=0.3$ V_{P-P}
Operating frequency	f_{in3}	9		150	MHz	VCOL, sine wave input $V_{in}=0.3$ V_{P-P}
Operating frequency	f_{in4}	9		250	MHz	VCOL, sine wave input $V_{in}=0.3$ V_{P-P}
Operating frequency	f_{in5}	0.1		1	MHz	AMIFC, sine wave input $V_{in}=0.3$ V_{P-P}
Operating frequency	f_{in6}	5		15	MHz	FMIFC, sine wave input $V_{in}=0.3$ V_{P-P}
AD converting resolution				6	bit	
Absolute accuracy of AD conversion			±1	±1.5	LSB	T_a= + 10 to + 50°C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source current	I_{DD3}		15		mA	CPU and PLL are operating VCOL sine wave Input f_{in}=150 MHz V_{in}=0.5 VP-P V_{DD}=5 V T_a=25°C
High level output current	I_{OH4}		−0.2		mA	COM_0, COM_1 $V_{OH}=V_{DD}-1$ V
Intermediate level output current	I_{OM1}		−20		μA	COM_0, COM_1 $V_{OM}=V_{DD}+1$ V
Intermediate level output current	I_{OM2}		20		μA	COM_0, COM_1 $V_{OM}=1$ V
Low level output current	I_{OL5}		0.2		mA	COM_0, COM_1 $V_{OL}=1$ V

28. Package Information

80-pin, plastic QFP (14 x 20) package dimensions (Unit: mm)



S80GF-80-3B9

29. Recommended Soldering Conditions

The following conditions are recommended for soldering of uPD17003A. When using any soldering method or soldering condition other than the recommendation, please consult the NEC customer engineer.

Table 29-1 Recommended soldering conditions

Product name	Package	Recommended condition mark
μPD17003AGF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)	— IR30-00 — VP15-00 — WS60-00 — Heating of pin portion

Table 29-2 Soldering conditions

Recommended condition mark	Soldering method	Soldering condition
IR30-00	Infrared ray reflow	Package peak temperature: 230°C, Time: within 30 sec (over 210°C), Frequency: 1, Restricted No. of daysNote: None
VP15-00	VPS	Package peak temperature: 215°C, Time: within 40 sec (over 200°C), Frequency: 1, Restricted No. of daysNote: None
WS60-00	Wave soldering	Solder bath temperature: Below 260°C, Time: within 10 sec, Frequency: 1, Restricted No. of daysNote: None
Pin portion heating	Pin heating type	Pin temperature: Below 300°C, Time: within 10 sec, Restricted No. of daysNote: None

Note: No. of storage days after opening dry pack. Storage conditions are 25°C and 65% RH or less.

Remarks: For the details of the recommended soldering conditions of the surface mounted type, refer to "Mounting Manual for Surface-Mounted Devices" (IE1-616).

SINGLE CHIP MICROCONTROLLER FOR DIGITAL TUNING SYSTEM

The μPD17005 is a 4 bit single chip CMOS microcontroller equipped with the hardware exclusively for digital tuning systems.

Adoption of the μPD17000 architecture enables its CPU to directly operate the data memory, perform various calculations, or control the peripheral hardware with just one instruction. All instructions are single 16-bit words.

The μPD17005 integrates input/output ports, LCD drivers, A/D converters, D/A converters (PWM output), clock generator ports, digital tuning 150 MHz prescalars, PLL frequency synthesizers, low pass filter (LPF) amplifiers, and frequency counters into one chip.

With all these in one chip, the μPD17005 provides a high performance and multi-functional digital tuning system.

The one-time PROM (OTP) μPD17P005 is available for evaluating the μPD17005 program and low quantity production.

The μPD17003, which contains the compressed program memory (ROM), is compatible with this microcontroller.

FEATURES

- Employment of the μPD17000 architecture
- 16K byte (16 bits x 7932 steps) program memory (ROM)
- 432 nibble (4 bits x 432 nibbles) general purpose data memory (RAM)
- 4.44 μs (4.5 MHz crystal oscillator) instruction execution time
- Decimal calculation available
- Table referencing available
- Equipped with the PLL frequency synthesizer hardware
  Dual modular prescalars (up to 150 MHz), programmable dividers, phase comparators, charge pumps, and LPF amplifiers
- Abundant peripheral hardware
  General purpose input/output ports, LCD drivers, serial interfaces, A/D converters, D/A converters (PWM output), clock generator ports, frequency counters
- Enriched interrupt function
  External interrupt 2 channels
  Internal interrupt 3 channels
- Equipped with power on reset/CE pin reset/electrical blackout detection circuit
- CMOS low energy requirement
- Voltage: 5 V ±10 %

ORDERING INFORMATION

Order Code	Package
μPD17005GF-xxx-3B9	80-pin plastic QFP (bent lead)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

In case of using this interface mode note the following:

Duties when using I2C bus system

Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

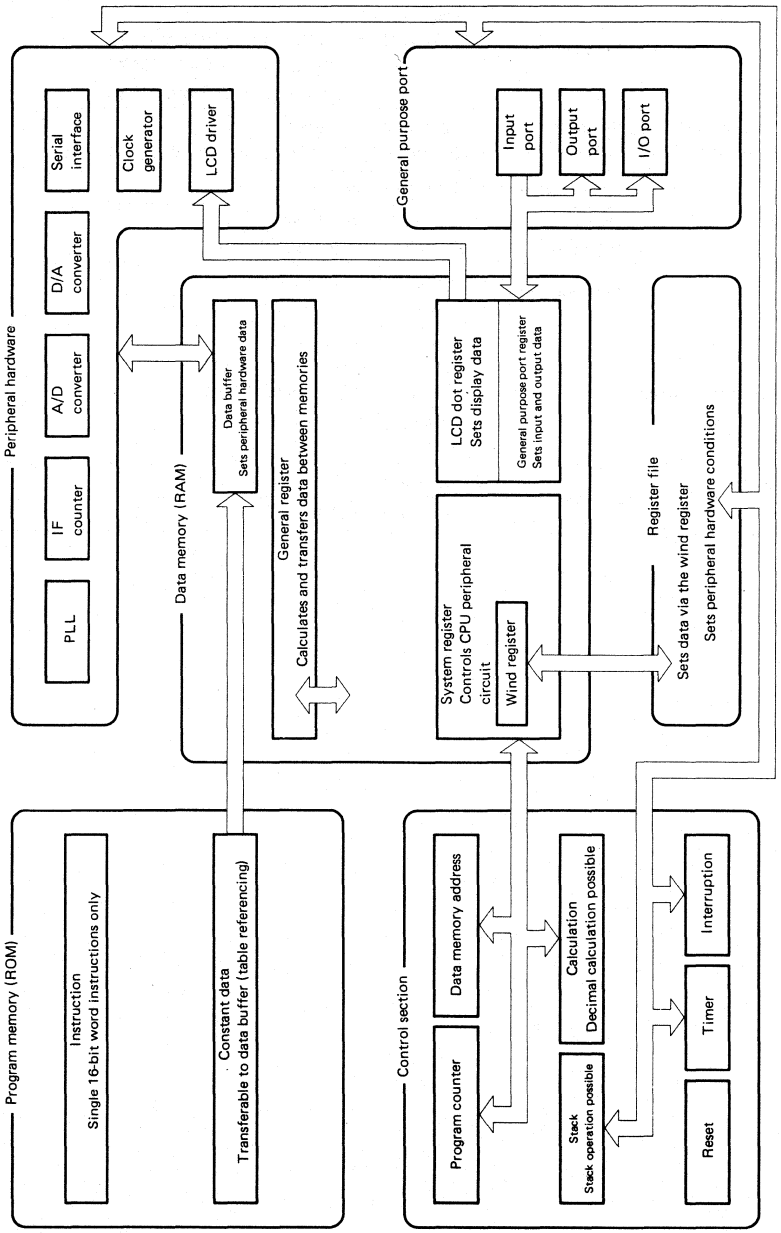
Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

TABLE OF μPD17005 FUNCTIONS

NAME	FUNCTION
Program memory (ROM)	16K bytes (16 bits x 7932 steps) Table reference area: up to 16 bits x 7932 steps
General purpose data memory (RAM)	432 nibbles (4 bits x 432 nibbles) Data buffer : 4 nibbles General register: 16 nibbles
System register	12 nibbles
Register file	33 nibbles
Port register (including LCD register)	24 nibbles
Instruction execution time	4.44 μs (with 4.5 MHz crystal oscillator)
Stack level	7 levels (stack operation possible)
General purpose port	16 input/output ports 8 input ports 9 output ports (+30: LCD segment pins)
Clock generator port (CGP)	One port Variable duty pulse (VDP) and signal generator (SG) functions
LCD driver	30 segment pins, 2 common pins, 1/2 duty, 1/2 bias, 250 Hz frame frequency, driving voltage V_{DD}, 16 segment pins shared with key source All 30 segments can be used as an output port. (separatable into 4, 4, 6, and 16 segment settings)
Serial interface	2 systems (3 channels) 8 bit 3 lines: 2 channels 8 bit 2 lines: 1 channel
D/A converter	8 bits x 3 lines (PWM output, up to 12 V)
A/D converter	6 bits x 6 lines (consecutive comparison by the software)
Interrupt	5 channels (maskable interrupt) External interrupt: 2 channels (INT_0 pin, INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, frequency counter)
Timer	2 systems Timer carry F/F (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms)
Reset	Power on reset (by turning on the power) CE pin reset (CE pin low → high) Electrical blackout detection

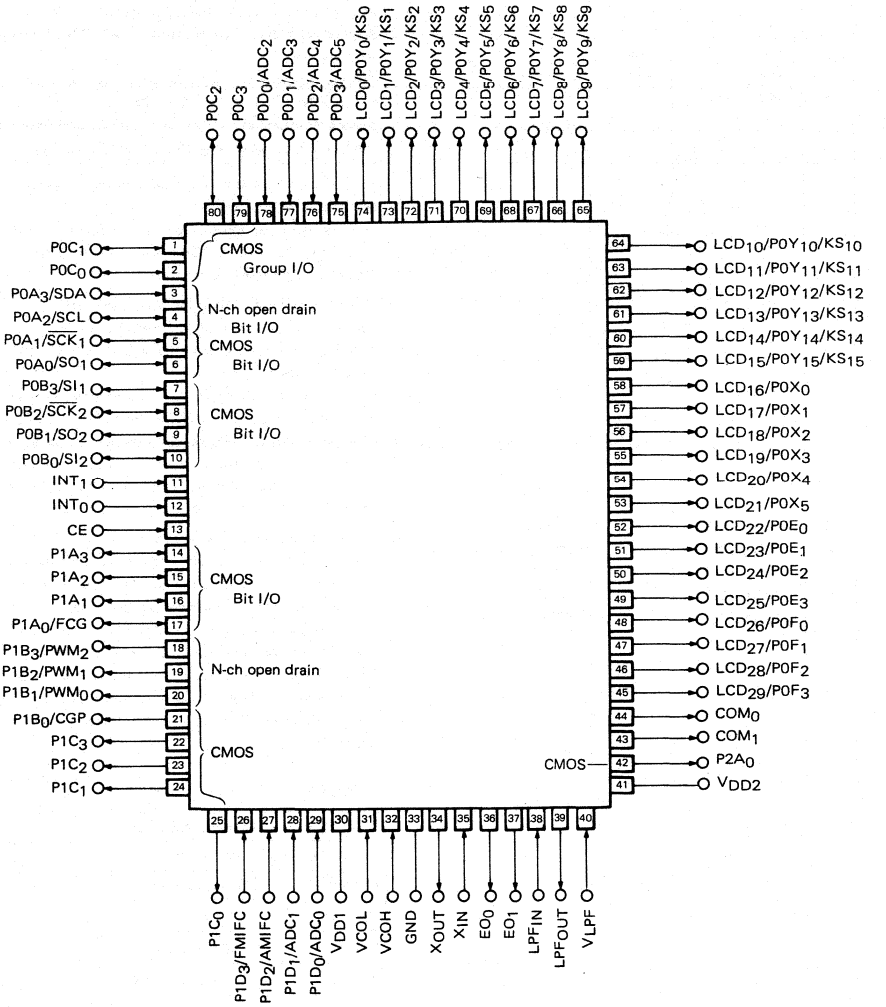
NAME		FUNCTION
PLL frequency synthesizer	Division	Two types Direct division (VCOL pin 20 MHz MAX.) Pulse swallow (VCOL pin 40 MHz MAX.) (VCOH pin 250 MHz MAX.)
	Reference frequency	12 choices by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	Two independent error outputs
	Phase comparator	Unlock detection by program Unlock F/F delay time selection
	LPF amplifier	CMOS operation amplifier Output voltage up to 12 V
Frequency counter		Frequency measuring $P1D_3$/FMIFC pin 0.1 to 1 MHz $P1D_2$/AMIFC pin 5 to 15 MHz External gate width measuring POA_1/FCG pin
Power voltage		5 V ±10 %
Package		80-pin plastic QFP

μPD17005 CONCEPT DIAGRAM



1. PINS

1.1 PIN CONFIGURATION (Top View)



1.2 PIN DESCRIPTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>79
80
1
2</td><td>P0C3
P0C2
P0C1
P0C0</td><td>Input/ output</td><td>CMOS push/pull</td><td>Port 0C</td><td>4 bit general purpose input/output port pins.
Specify input or output in 4-bit units. (Group I/O)
Specify input/output by the register file's P0CGPIO register (address 27H).
To read the input data or to set the output data, use the port register's P0C register (BANK0 address 27H).
These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting.</td></tr>
<tr><td>3
4

5
6</td><td>P0A3/SDA
P0A2/SCL

P0A1/$\overline{SCK}$1
P0A0/SO1</td><td>Input/ output</td><td>N-ch open drain

CMOS push/pull</td><td>Port 0A</td><td>Pins function both as a 4-bit general purpose input/output port and serial interface.
To switch from an input/output port to serial interface, use the register file's SIO1MODE register (address 08H) and the SIO2MODE register (address 02H).
(1) When used as an 4-bit input/output port:
Specify input or output in 1-bit units (bit I/O).
To specify input/output, use the register file's P0ABIO register (address 35H).
To read the input data or set the output data, use the port register's P0A register (BANK0 address 70H). The P0A3/SDA and P0A2/SCL pins require external pull up resistance because they are N-ch open drain. These pins are set to an input port during power resetting, clock stop instruction execution, and CE resetting.
(2) When used as a serial interface:
There are two serial interface lines: serial interface 1 and serial interface 2 including the Port 0B (7 to 10 pins).
The serial interfaces 1 and 2 can be used together at the same time. The serial interface 1 has 2 channels of 2 line and 3 line, and the serial interface 2 has 1 channel of 3 line.
To specify the serial interface 1, use the register file SIO1 MODE register; to specify the serial interface 2, use the register file SIO2MODE register. The following are the pin functions.
<table>
<tr><th>PIN NAME</th><th>FUNCTION</th><th colspan="2">OPERATING MODE</th></tr>
<tr><td>P0A3/SDA</td><td>Data input/output</td><td rowspan="2">2 lines</td><td rowspan="5">Serial inter- face 1</td></tr>
<tr><td>P0A2/SCL</td><td>Clock input/output</td></tr>
<tr><td>P0A1/$\overline{SCK}$1</td><td>Clock input/output</td><td rowspan="3">3 lines</td></tr>
<tr><td>P0A0/SO1</td><td>Data output</td></tr>
<tr><td>P0B3/SI1</td><td>Data input</td></tr>
<tr><td>P0B2/$\overline{SCK}$2</td><td>Clock input/output</td><td rowspan="3">3 lines</td><td rowspan="3">Serial inter- face 2</td></tr>
<tr><td>P0B1/SO2</td><td>Data output</td></tr>
<tr><td>P0B0/SI2</td><td>Data input</td></tr>
</table>
</td></tr>
</table>

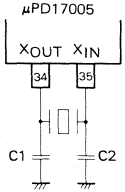
PIN. No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
3 4 5 6	$P0A_3$/SDA $P0A_2$/SCL $P0A_1/\overline{SCK_1}$ $P0A_0/SO_1$				The $P0A_3$/SDA and $P0A_2$/SLC pins require external pull up resistance because they are N-ch open drain. These pins are set as an input port of the general purpose input/output port during power on resetting, clock stop instruction execution, and CE resetting.
7 8 9 10	$P0B_3/SI_1$ $P0B_2/\overline{SCK_2}$ $P0B_1/SO_2$ $P0B_0/SI_2$	Input/ output	CMOS push-pull	Port 0B	Pins function both as a 4 bit general purpose input/output port and serial interface. To switch from input/output port to serial interface, use the register file's SIO1MODE register (address 08H) and the SIO2MODE register (address 02H). (1) When used as an 4-bit input/output port: Specify input or output in 1-bit units (bit I/O). To specify input/output, use the register file's P0BBIO register (address 35H). To read the input data or set the output data, use the port register's P0A register (BANK0 address 71H). These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting. (2) When used as an serial interface: There are two serial interface lines: serial interface 1 and serial interface 2 including the Port 0A (3 to 6 pins). These pins are set as an input port of the general purpose input/output port during power resetting, clock stop instruction execution, and CE resetting.
11 12	INT_1 INT_0	Input	–	Interrupt	Input pins for external interrupt request signal Interrupt requests are issued at the rising or falling edge of the signal input through these pins. To specify the rising or falling edge, use the register file's INTEDGE register (address 1FH), INT_0 pin, or INT_1 pin. Interrupt requests are not accepted unless permitted (maskable interrupt). The EI instruction permits all interrupts, and the INT_0 pin or INT_1 pin separately also gives permission. To give interrupt permissions, use the register file's INTPM2 register (address 2FH). Interrupt requests are accepted if permitted. Interrupts accepted by the INT_0 pin shift the flow of the program to address 05H, and interrupts accepted by the INT_1 pin shift the flow of the program to address 04H. Interrupts accepted by the INT_0 pin are executed before interrupts accepted by the INT_1 pin, if issued simultaneously. The issuer of the interrupt request can be checked by the register file's INTREQ2 register (address 3) even when the interrupt is not accepted. The register file's INTJDG register (address 0FH) checks the status of these pins and assigns them as a general purpose input port while the interrupt function is not being used. These pins are set as an input port during power resetting, clock stop instruction execution, and CE resetting.

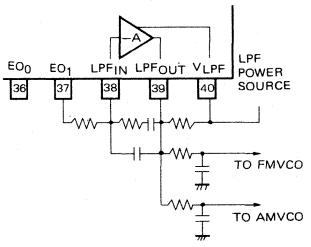
PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
13	CE	Input	–	Chip enables	Input pin for device selection signal or reset signal Device selection is selecting PLL actions or standby status as described below. The PPL frequency synthesizer is enabled when the CE pin is set to high. The PPL frequency synthesizer is disabled when the CE pin is set to low. When the CE pin is set to low, the CPU and the internal crystal oscillation circuit are disabled by the clock stop instruction execution and the data memory is retained by the low energy requirement current (up to 15 μA). (when the CE pin is set to high, the clock stop instruction is executed as the NOP instruction.) During the clock stop instruction execution, the LCD driver display mode is turned off (LCD_0 to LCD_{27}, COM_0, COM_1 pins set to low) and the input/output ports (Port 0A, Port 0B, Port 0C, Port 1A) are set as input ports. The CE pin functioning as a reset signal input pin is described below. When the CE pin is reset to high from low, the internal timer carrier F/F synchronizes and resets the device. When the device is reset, the flow of the program shifts to address 0 and the input/output ports become input ports. The time required from pin resetting to device resetting can be selected from 1, 5, 100, 250 ms, which are offered by the carrier F/F. However, when the clock stop instruction is executed, the device will be reset 100 ms after the CE is reset to high. This pin does not accept anything lower than 110 μs or anything higher than 165 μs in order to prevent mis-operation caused by noise. For this reason, the content of the register is not updated. Also, to detect the pin status, use the register file's CEJDG register (address 07). This pin features Schmidt trigger input with the hysteresis characteristics. Do not apply voltage higher than the V_{DD} pin when turning on the power.
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$/FCG	Input/ output	CMOS push-pull	Port 1A	Pins functioning both as a 4-bit general purpose input/output port or external gate counter ($P1A_0$/FCG pin). To switch from an input/output port to external gate counter, use the register file's IFCMODE register (address 12H) and the SIO2MODE register (address 02H). (1) When used as a 4-bit input/output port: Specify input or output in 1-bit units (bit I/O). To specify input/output, use the register file's P1A register (address 35H). To read the input data or set the output data, use the port register's P1ABIO register (BANK1 address 70H). These pins are set as input ports during power resetting, clock stop instruction execution, and CE resetting.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
14 15 16 17	$P1A_3$ $P1A_2$ $P1A_1$ $P1A_0$/FCG	Input/ output	CMOS push-pull	Port 1A	(2) When using as an external gate counter (FCG) ($P1A_0$/FCG pin): These pins measure the time interval between two rising edges of the $P1A_0$/FCG pin. To measure the internal reference frequencies (1 kHz, 100 kHz, 900 kHz), use the 16-bit counter. To specify the external gate counter, use the register file's IFCMODE register (address 12H) and IFCCONT register (address 23H). To set the $P1A_0$/FCG pin as an input port, use the P1ABIO register (BANK0 address 35H). Use the external gate counter, frequency counter and clock generator port separately, because the IFCMODE register and IFCCONT register also control the frequency counter ($P1D_3$/FMIFC and $P1D_2$/AMIFC pins) and the clock generator port ($P1B_0$/CGP pin). These pins are set as input ports during power on resetting, clock stop instruction execution, and CE resetting.
18 19 20 21	$P1B_3/PWM_2$ $P1B_2/PWM_1$ $P1B_1/PWM_0$ $P1B_0$/CGP	Output	N-ch open drain CMOS push-pull	Port 1B	Pins functioning as a 4-bit general purpose input/output port, D/A converter ($P1B_2/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins), and clock generator port ($P1B_0$/CGP pin). To switch from an input/output port to D/A converter or to clock generator port, use the register file's PWMMODE register (address 13H). (1) When used as a 4-bit input/output port: To set the output data, use the port register's P1B register (BANK1 address 71H). The $P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins require pull up resistance because they are for open drain output (up to 16 V). The data output during power resetting is unstable. The previous values are retained during clock stop instruction execution or CE resetting. (2) When used as a D/A converter (PWM output) ($P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins): The $P1B_3/PWM_2$, $P1B_2/PWM_1$, and $P1B_1/PWM_0$ pins separately output signals. The output format has a pulse width modulation (PWM) to 878.9 Hz (225/256 kHz) frequency and 0.25/0.26 to 255.25/256 duty (256 gradations). To set the duty, use the PWMR0 to PWMR2 register (address 05 to 07) via the data buffer. $(\text{Duty} = \frac{0.25 + X}{256} \quad X = 0 \text{ to } 255)$ These three pins are for N-ch open drain output and withstands up to 16 volts. These pins are set as a general purpose output port during clock stop instruction execution. The status of these pins functioning as a D/A converter output is retained during CE resetting.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
18 19 20 21	P1B$_3$/PWM$_2$ P1B$_2$/PWM$_1$ P1B$_1$/PWM$_0$ P1B$_0$/CGP	Output	N-ch open drain CMOS push-pull	Port 1B	(3) When used as a clock generator port (CGP) (P1B$_0$/CGP pin): To set the P1B$_0$/CGP pin to CGP mode, use the register file's PWMMODE register (address 13H) and IFGMODE register (address 12H). The CGP mode has VDP (variable duty pulse) and SG (signal generator) functions. The VDP function outputs 269 Hz frequency duties at 64 gradations from 2/67 to 65/67. The SG function divides and outputs the standard 18 kHz frequency by 4 to 130 (64 gradations). To set the data for VDP and SG functions, use the CGPR register (address 20H) via the data buffer. VDP duty = $\frac{2+X}{67}$ X = 0 to 63 SG divider = $\frac{18\text{ kHz}}{2(2+X)}$ The P1B$_0$/CGP pin is set as a general purpose output port during clock stop instruction execution and power resetting. The status of these pins functioning as a clock generator port output is retained during CE resetting.
22 23 24 25	P1C$_3$ P1C$_2$ P1C$_1$ P1C$_0$	Output	CMOS push-pull	Port 1C	4-bit general purpose output ports. To set the output data, use the port register's P1C register (BANK1 address 72). The data output during power resetting is unstable. The previous values are retained during clock stop instruction execution or CE resetting.
26 27 28 29	P1D$_3$/FMIFC P1D$_2$/AMIFC P1D$_1$/ADC$_1$ P1D$_0$/ADC$_0$	Input	–	Port 1D	Pins functioning as a 4-bit general purpose input port, frequency counter (P1D$_3$/FMIFC, P1D$_2$/AMIFC pins) and A/D converter (P1D$_1$/ADC$_1$, PAD$_0$/ADC$_0$ pins). To switch from input port to frequency counter, use the register file's IFCMODE register (address 12H). To switch from input port to A/D converter, use the register file's ADCCH register (address 14H). (1) When used as a 4 bit input/output port: To read the input data, use the port register's P1D register (BANK1 address 73H). (2) When used as a frequency counter: To use the P1D$_3$/FMIFC and P1D$_2$/AMIFC pins as a frequency measuring pin, use the register file IFCMODE register. The measurable frequency bands for the P1D$_3$/FMIFC pins are 5 to 15 MHz (0.3 Vp-p input) and 0.1 to 1 MHz (0.3 Vp-p input) for the P1D$_2$/AMIFC pin. To measure, count the frequencies input in the gate time (1 ms, 4 ms, 8 ms, open) by the 16 bit counter. The P1D$_3$/FMIFC pin counts the values divided by 1/2. Interrupt requests can be issued after the measuring is completed (when the gate closes). These functions can be utilized for detecting broadcasting stations by counting the intermediate frequencies. When used as a frequency counter, cut DC input signals by the condenser because the AC amplifier accepts inputs only.

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
26 27 28 29	$P1D_3$/FMIFC $P1D_2$/AMIFC $P1D_1/ADC_1$ $P1D_0/ADC_0$	Input	–	Port 1D	The intermediate voltage of the selected pins are set to approx. 1/2 V_{DD}. Non-selected pins are used as a general purpose input port. Initialize the AC amplifier by programming as necessary, because it is not disabled by resetting the CE pin (No. 13) to low. (Noise from the active amplifier may increase the current consumption.) Use the frequency counter, external gate counter, and clock generator port separately because the IFCMODE register specifies the external gate counter ($P1A_0$/FCG pin) as well as the clock generator port ($P1B_0$/CGP pin). These pins are set as a general purpose input port during power resetting and clock stop instruction execution. These pins continue acting as a frequency counter during CE resetting. (3) Used as an A/D converter ($P1D_1/ADC_1$, $P1D_0/ADC_0$ pin): To use these pins as a 6-bit A/D converter, use the register file's ADCCH register (address 14H). Up to six channels can be switched for the $P1D_1/ADC_1$, $P1D_0/ADC_0$ pins as well as the $P0D_3/ADC_5$ to $P0D_0/ADC_2$ pins (75 to 78 pins). Use the consecutive comparison by programming to convert from A to D and reference voltage is created by R string method, in which the power voltage is divided up. These pins are set as a general purpose input port during power resetting and clock stop instruction execution. These pins continue acting as an A/D converter during CE resetting.
30 41	V_{DD1} V_{DD2}	–	–	Power	Device power pin. These pins supply 5 V ±10 % voltage to the CPU and peripheral functions under operation. These pins lower the voltage to 3.5 V if the CPU alone is being operated. When the CE pin (No. 13) executes the clock stop instruction at low, the crystal oscillator stops oscillation and enters the data memory backup state. During this time, the power voltage is lowered to 2.2 V. When the power voltage rises from 0 to 4.5 V or when the power voltage falls below 3.5 V (2.2 V for clock stop instruction) and rises to 4.5 V, the device enters the power resetting state. After power resetting, the peripheral circuit, system register, and register files are initialized, and the program starts from address 0. The power voltage rising time from 0 to 4.5 V should be up to 500 ms. In addition to power on resetting, just explained, the CE pin also resets the device (CE pin low → high). Electric blackouts can be detected by detecting the timer carrier F/F values of the register file, which are different during power resetting and CE resetting.

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>30
41</td><td>V_{DD1}
V_{DD2}</td><td>–</td><td>–</td><td>Power</td><td>Do not apply a voltage higher than the V_{DD} pin to the rest of the pins. Pay special attention to both V_{DD} pin and CE pin rising simultaneously, otherwise resulting in latch up. Always connect the V_{DD1} and V_{DD2} pins to the same potential. The V_{DD2} pin supplies power to the crystal oscillation circuit (X_{IN} and X_{OUT} pins), error out circuit (EO_0 and EO_1 pins), and low pass filter circuit (LPF_{IN} and LPF_{OUT} pins); the V_{DD1} pin supplies power to all other parts.</td></tr>
<tr><td>31
32</td><td>VCOL
VCOH</td><td>Input</td><td>–</td><td>Oscillation low input
Oscillation high input</td><td>Pin for entering PLL oscillation frequency (VCO).
To specify one of the two division methods, direct division (MF mode) and pulse swallow (HF mode and VHF mode), use the register file's PLLMODE register (address 21H).
The following shows the input pins, input frequencies, and division ratios for each division methods.
<table>
<tr><th>Division method</th><th>Input pin</th><th>Input frequency</th><th>Input voltage</th><th>Division ratio</th></tr>
<tr><td>Direct division MF mode</td><td>VCOL</td><td>0.5–30 MHz</td><td>0.3 Vp-p</td><td>16 to $2^{16}-1$</td></tr>
<tr><td>Pulse swallow HF mode</td><td>VCOL</td><td>5–40 MHz</td><td>0.3 Vp-p</td><td>256 to $2^{16}-1$</td></tr>
<tr><td rowspan="2">Pulse swallow VHF mode</td><td rowspan="2">VCOH</td><td>9–150 MHz</td><td>0.3 Vp-p</td><td rowspan="2">256 to $2^{16}-1$</td></tr>
<tr><td>9–250 MHz</td><td>0.5 Vp-p</td></tr>
</table>
Cut DC input signals by the condenser because these pins accept AC amplifier inputs only. The pin specified by the PLLMODE register is set to intermediate voltage (approx. 1/2 V_{DD}). The pins that are not specified are internally pulled down. These pins are internally pulled down during PLL disabled and low CE pin states.
These pins disable the PLL during power on resetting and clock stop instruction execution.
These pins enter the PLLMODE register specified state during CE resetting.</td></tr>
<tr><td>33</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>Device ground pin</td></tr>
<tr><td>34
35</td><td>X_{OUT}
X_{IN}</td><td>Output
Input</td><td>CMOS</td><td>Crystal oscillator</td><td>Crystal oscillator
The following shows the method for connecting the 4.5 MHz crystal oscillator.
 
</td></tr>
</table>

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
34 35	X_{OUT} X_{IN}	Output Input	CMOS	Crystal oscillator	The crystal oscillator in use determines the values of C1 and C2. Large C1 and C2 values degrade the oscillation start characteristic and increase the consumption current. Although the trimmer condenser connected to the X_{IN} pin is generally considered to adjust wider range of oscillation frequencies, it is recommended that it be connected to the crystal oscillator in use for a better oscillation stability. If probes are connected to the X_{OUT} pin or X_{IN} pin, the oscillation frequencies cannot be adjusted correctly owing to probe capacitance. Thus, adjust while measuring the LCD driving waveform (125 MHz) of the number of VCO oscillation frequencies. When the oscillation frequency is off the 4.5 MHz setting the oscillation frequencies of the internal timer and LL reference frequency are also off in the same proportion because they employ a divided 4.5 MHz.
36 37	EO_1 EO_0	Output	CMOS 3 state	Error out	Output pin for PLL frequency synthesizer charge pump. These pins output high level when the divided VCO frequency input through the VCOL pin (No. 31) and VCOH pin (No. 32) is higher than the reference frequency; these pins output low level when the divided VCO frequency input through the VCOL pin (No. 31) and VCOH pin (No. 32) is lower than the reference frequency. These pins are set to floating when the divided VCO frequency matches the reference frequency. To construct the PLL frequency synthesizer, use the external low pass filter (LPF) and apply these pin outputs to the voltage control oscillator (VCO). The EO_1 pin and EO_2 pin output the same signals, so use either pin. These pins are set to floating during PLL disabled state, i.e., during low CE pin (No. 13) or power resetting. To detect the PLL unlock state, use the register file's PLLULJDG register (05H). To select one of the four delay times (0.5 μs, 1 μs, 2 μs, disable) for PLL unlock state detection, use the register file's PLULDLY register (address 15H).
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output —	N-ch open drain	LPF amplifier	Low pass filter (LPF) CMOS operation amplifier built-in pin. The following is the example of a pin internal equivalent circuit and application circuit. μPD17005 

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
38 39 40	LPF_{IN} LPF_{OUT} V_{LPF}	Input Output —	N-ch open drain	LPF amplifier	The LPF_{OUT} pin requires pull up resistance because it is for N-ch open drain output. It withstands voltage up to 16 V. Apply a voltage, which is higher than that applied to the LPF_{OUT} pin, but not exceeding 16 V, to the V_{LPF} pin. The LPF_{OUT} pin is internally pulled up during PLL disabled state.
42	$P2A_0$	Output	CMOS push-pull	Port 2A	1 bit output port pin. To set the data, use the port register's P2A register (BANK2 address 70H). The data output during power on resetting is unstable. The previous output values are retained during clock stop instruction execution and CE resetting.
43 44	COM_1 COM_0	Output	CMOS	Common signal	Output pin for LCD driver common signal. The LCD driver has 1/2 duty, 1/2 bias, a 250 Hz frame frequency, and V_{DD} driving voltage. Up to 60-dot display can be done by matrix with the LCD_0/$P0Y_0/KS_0$ to $LCD_{29}/P0F_3$ pins. These pins output three voltages: ground, 1/2 V_{DD}, and V_{DD}. Dots light up when $\pm V_{DD}$ potential difference is generated between these pins and $LCD_0/P0Y_0/KS_0$ to $LCD_{29}/P0F_3$ pins. These pins output low during power resetting and clock stop instruction execution, provided that the display mode was turned off by the register file's LCDMODE register (address 10H). The output status of these pins is retained during CE resetting, provided that the display mode is turned on.
45 to 48 49 to 52 53 to 58 59 to 74	$LCD_{29}/P0F_3$ to $LCD_{26}/P0F_0$ $LCD_{25}/P0E_3$ to $LCD_{22}/P0E_0$ $LCD_{21}/P0X_5$ to $LCD_{16}/P0X_0$ $LCD_{15}/$ $P0Y_{15}/KS_{15}$ to $LCD_0/$ $P0Y_0/KS_0$	Output	CMOS push-pull	LCD segment signal	Pins functioning as LCD driver segment signal output pins ($LCD_{29}/P0F_3$ to $LCD_0/P0Y_0/KS_0$ pins), key matrix source signal output pins ($LCD_{15}/P0Y_{15}/KS_0$ to $LCD_0/P0Y_0/KS_0$ pins), and general purpose output port ($LCD_{29}/P0F_3$ to $LCD_0/P0Y_0/KS_0$ pins). To switch from segment signal to key source signal or to general purpose output port, use the register file LCDMODE register (address 10H) or the LCDPORT register (address 11H). (1) When using as an LCD driver segment signal output pin ($LCD_{29}/P0F_3$ to $LCD_0/P0Y_0/KS_0$ pins): The LCD driver has a 1/2 duty, 1/2 bias, and 250 Hz frame frequency (125 Hz segment signal output). Up to 60 dot display can be done by matrix with these segment signal output pins and COM_0 pin and COM_1 pin (No. 44 and 43). Dots light up when $\pm V_{DD}$ potential difference is generated between these pins and $LCD_0/P0Y_0/KS_0$ to $LCD_{29}/P0F_3$ pins. To set the LCD driver display data, use the LCD dot register (BANK0 address 60H to 6EH), or the LCD group register (address 08H to 0FH) via the data buffer. To turn the LCD driver display on or off, use the register file's LCDMODE register. When the display mode is turned off, these segment signal output pins are set to low. But the pins, which are specified as a general purpose output port

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
45 to 48	$LCD_{29}/P0F_3$ to $LCD_{26}/P0F_0$	Output	CMOS push-pull	LCD segment signal	by the register file's LCDPORT register, output the output port data regardless of the display mode. These pins output low during power resetting and clock stop instruction execution. The output status of these pins are retained during CE resetting, provided that the display mode is turned on. The $LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$ pins can output both the segment signal and key source signal of the 16 key matrix at the same time. (2) When using as a key matrix source signal: To set these 16 $LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$ pins as a key source signal output pin, use the register file's LCDMODE register. The key source signals are output with the LCD segment signals by time division. (Key source signal output time: 220 μs). To use the key source signal, set the $P0D_3/ADC_5$ to $P0D_0/ADC_2$ pins as a key return signal input pin (No. 75 to 78). Therefore, the key matrix with 16 key sources and four input keys is configured. Key source signals are output every 4 ms. To set the output data of the key source signal, use the key source register (address 42H) via the data buffer. The key source signal is not output when the LCD driver display mode is turned off (the segment signal output is low) or when these pins are set as a general purpose output port. The key source signal is not output during power on resetting and clock stop instruction execution. The output status of these pins are retained during CE resetting. (3) When used as an output port: The following table shows how to set these pins as an output port using the register file's LCDPORT register (address 11H).
49 to 52	$LCD_{25}/P0E_3$ to $LCD_{22}/P0E_0$				
53 to 58	$LCD_{21}/P0X_5$ to $LCD_{16}/P0X_0$				
59 to 74	$LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$				

PIN No.	PIN Name	Port name	Number of bits
45 to 48	$LCD_{29}/P0F_3$ to $LCD_{26}/P0F_0$	Port 0F	4 bits
49 to 52	$LCD_{25}/P0E_3$ to $LCD_{22}/P0E_0$	Port 0E	4 bits
53 to 58	$LCD_{21}/P0X_5$ to $LCD_{16}/P0X_0$	Port 0X	6 bits
59 to 74	$LCD_{15}/P0Y_{15}/KS_{15}$ to $LCD_0/P0Y_0/KS_0$	Port 0Y	16 bits

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>INPUT/ OUTPUT</th><th>OUTPUT FORMAT</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>45
to
48

49
to
52

53
to
58

59
to
74</td><td>$LCD_{29}/P0F_3$
to
$LCD_{26}/P0F_0$

$LCD_{25}/P0E_3$
to
$LCD_{22}/P0E_0$

$LCD_{21}/P0X_5$
to
$LCD_{16}/P0X_0$

$LCD_{15}/$
$P0Y_{15}/KS_{15}$
to
$LCD_0/$
$P0Y_0/KS_0$</td><td>Output</td><td>CMOS push-pull</td><td>LCD segment signal</td><td>The Port 0F, Port 0E, Port 0X, and Port 0Y can be specified separately as an output port, otherwise they function as an LCD segment signal output pin. The following table shows how to set output data in each port.

<table><tr><th>Port name</th><th>Output data setting</th></tr><tr><td>Port 0F</td><td>P0F register (BANK0 address 6DH) also functions as the LCD dot register's LCDD 13 register.</td></tr><tr><td>Port 0E</td><td>P0E register (BANK0 address 6BH) also functions as the LCD dot register's LCDD 11 register.</td></tr><tr><td>Port 0X</td><td>P0XH, and P0XL registers (BANK0 address 69H and 68H) also function as the LCD dot register's LCDD 9 register and LCDD 8 register, respectively. To set the output data, use the P0X group register (0CH) via the data buffer.</td></tr><tr><td>Port 0Y</td><td>To set the output data, use the P0Y group register (42CH) via the data buffer.</td></tr></table>
These pins are set as a segment signal output pin and thus output low level during power resetting and clock stop instruction execution.
The previous output status is retained during CE resetting.</td></tr>
<tr><td>75
76
77
78</td><td>$P0C_3/ADC_5$
$P0C_2/ADC_4$
$P0C_1/ADC_3$
$P0C_0/ADC_2$</td><td>Input</td><td>Input with pull down</td><td>Port 0C</td><td>Pins functioning as a 4-bit general purpose input port and A/D converter input pin.
To switch from the input port to A/D converter, use the register file's ADCCH register (address 14H).

(1) When used as an input port:
To read the input data, use the port register's POC register (BANK0 address 72H).
The $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins have a built-in pull-down resistance enabling them to be used as a key return signal input pin of the key matrix. To use the LCD segment pin as the key source, turn off the pull-down resistance during key source signal output (220 μs), and turn on the pull-down resistance during segment signal output (220 μs). Always keep the pull-down resistance on when the LCD segment pin is not used as the key source.
Turn off the pull-down resistance of the pin set as an A/D converter by the register file's ADCCH register.

(2) When used as an A/D converter:
To set these pins as a 6 bit A/D converter, use the register file's ADCCH register (address 14H).
Use the consecutive comparsion by programming to convert from A to D. The reference voltage is created by the R string method, in which the power voltage is divided up.
Up to six channels can be switched for the $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins as well as the $P1D_1/ADC_1$, $P1D_0/ADC_0$</td></tr>
</table>

PIN No.	SYMBOL	INPUT/ OUTPUT	OUTPUT FORMAT	PIN NAME	DESCRIPTION
75 76 77 78	$P0C_3/ADC_5$ $P0C_2/ADC_4$ $P0C_1/ADC_3$ $P0C_0/ADC_2$	Input	Input with pull down	Port 0C	pins (No. 28 and 29). To specify the desired channel, use the register file's ADCCH register. The other five channels function as general purpose input ports. The pull-down resistance built-in $P0C_3/ADC_5$ to $P0C_0/ADC_2$ pins are equipped with a pull-down resistance. When these pins are set as an A/D converter input pin by the ADCCH register, the pull-down resistance is turned off. The A/D converter pins are re-specified to the general purpose input port during power resetting and clock stop instruction execution. These pins function as an A/D converter during CE resetting.

1.3 NOTES ON USING GENERAL PURPOSE PORT

1.3.1 Port register data bit

To read the input data or set the output data in the Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A, use port registers (P0A to P2A register) in the data memory.

The $P0A_3$ pin and the $P0A_0$ pin of the Port 0A correspond to the most significant bit and the least significant bit of the port register P0A, respectively.

The same rule applies to the Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A.

To set the output data in the Port 0E, Port 0F, Port 0X, and Port 0Y, use the LCD group register via the LCD dot register or the data buffer in the data memory.

1.3.2 Input/output ports (Port 0A, Port 0B, Port 0C, Port 1A)

(1) When a port is specified as an input port:

Execute the instruction to read the contents of the port register in the data memory (provided that the port register address is defined as m of the SKT m, #i instruction or ADD r, m instruction). The port pin status is stored as the port register value. Execute the instruction to write in the port register (provided that the port register address is defined as m of the MOV m, #i instruction or r of the ADD r, m instruction), and the values are written in the output data latch circuit.

(2) When a port is specified as an output port:

Executes the instruction to write in the port register. The values are written in the output data latch circuit and output through each pin. Execute the instruction to read the contents of the port register. The output data latch content is stored as the port register value. However, when the read instruction is executed through the $P0A_3$/SDA and $P0A_2$/SCL pins, the pin status is read and different data may be output.

These pins are set as an input port during power resetting, CE resetting or clock stop instruction execution. Write the output latch content, which becomes unstable during power resetting, in the port register before setting it in the output port, otherwise the output data will be unstable. The output data latch content is not updated during clock stop instruction execution or CE resetting.

1.3.3 Output ports (Port 1B, Port 1C, Port 0F, Port 0E, Port 0X, and Port 0Y)

Output ports write port register values in the output latch and outputs them through the pins.

Execute the instruction to read the port register value. The latch status is stored as the port register value.

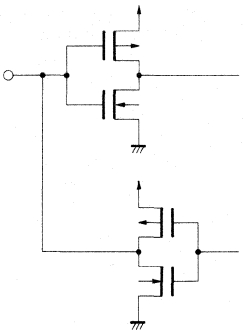
The data output during power on resetting is unstable.

The previous output data is retained during CE resetting or clock stop instruction execution.

The Port 0E, Port 0F, Port 0X, and Port 0Y automatically output low level during power on resetting or clock stop instruction execution.

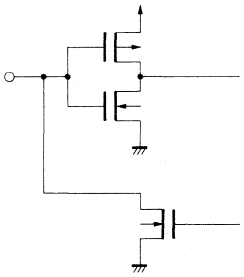
1.4 PIN EQUIVALENT CIRCUITS

1.4.1 P0A ($P0A_1/\overline{SCK}_1$, $P0A_0/SO_1$)
P0B ($P0B_3/SI_1$, $P0B_2/\overline{SCK}_2$, $P0B_1/SO_2$, $P0B_0/SI_1$)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)



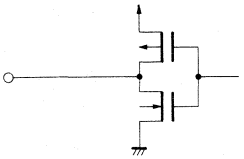
(Input/output)

1.4.2 P0A ($P0A_3$/SDA, $P0A_2$/SCL)



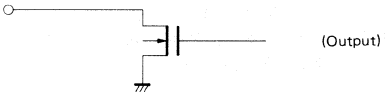
(Input/output)

1.4.3 P0C ($P0C_3/P0C_2$, $P0C_1$, $P0C_0$)
P1B ($P1B_0$/CGP)
P1C ($P1C_3$, $P1C_2$, $P1C_1$, $P1C_0$)
P2A ($P2A_0$)
$LCD_0/P0Y_0/KS_0$ to $LCD_{29}/P0F_3$

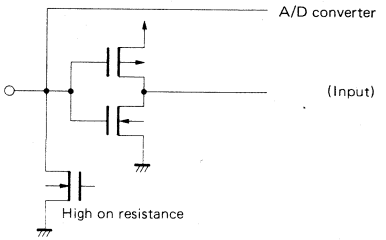


(Output)

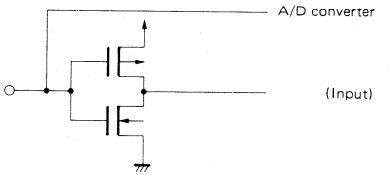
1.4.4 P1B ($P1B_3/PWM_2$, $P1B_2/PWM_1$, $P1B_0/PWM_0$)



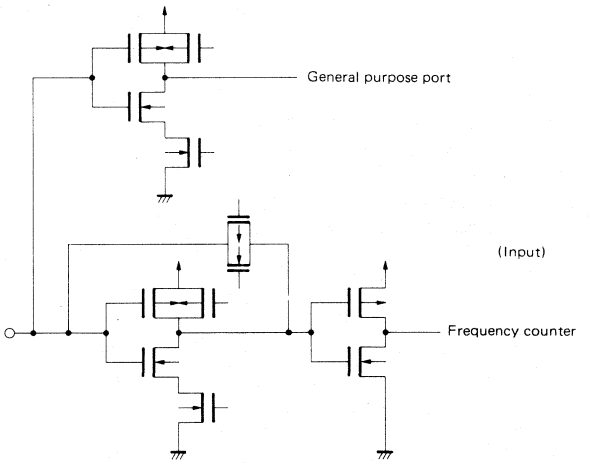
1.4.5 P0D ($P0D_3/ADC_5$, $P0D_2/ADC_4$, $P0D_1/ADC_3$, $P0D_0/ADC_2$)



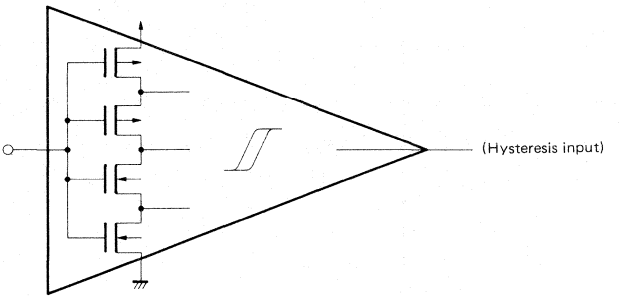
1.4.6 P1D ($P1D_1/ADC_1$, $P1D_0/ADC_0$)



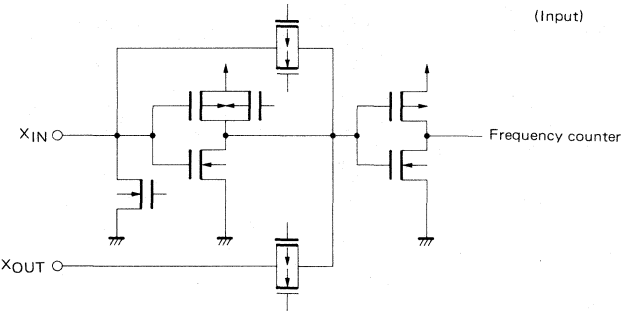
1.4.7 P1D ($P1D_3/FMIFC$, $P1D_2/AMIFC$)



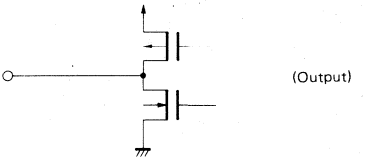
1.4.8 CE
INT_1
INT_0



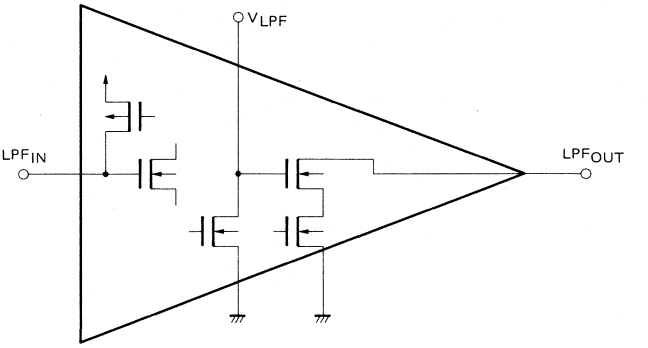
1.4.9 X_{OUT}, X_{IN}



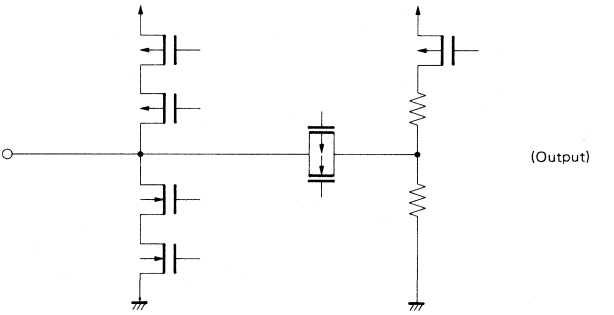
1.4.10 EO_1, EO_0



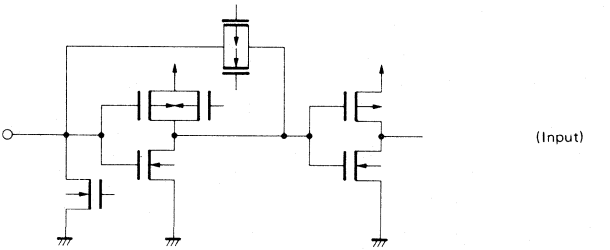
1.4.11 LPF_{IN}, LPF_{OUT}, V_{LPF}



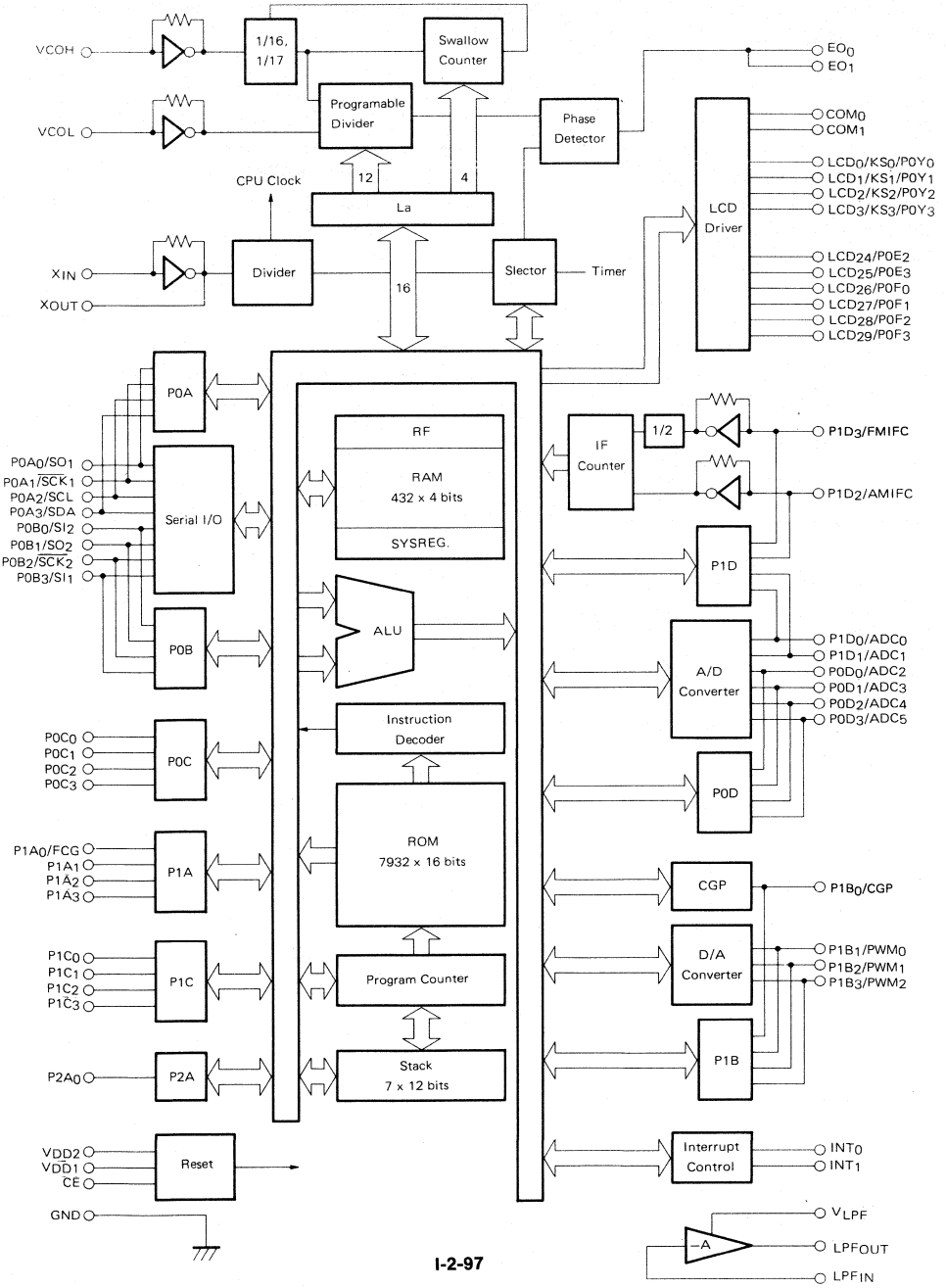
1.4.12 COM_1, COM_0



1.4.13 VCOH
VCOL



2. BLOCK DIAGRAM



5. ELECTRIC CHARACTERISTICS (TENTATIVE)

5.1 ABSOLUTE MAXIMUM RATINGS (T_a = 25 ±2 °C, unless otherwise)

Power Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	−0.3 to V_{DD} + 0.3 (excluding $P1B_1$ to $P1B_3$, $P0A_2$, $P0A_3$, LPF_{OUT})	V
Maximum Output Voltage	V_{BDS1}	18.0 ($P1B_1$ to $P1B_3$, LPF_{OUT})	V
Maximum Output Voltage	V_{BDS2}	V_{DD} + 0.3 ($P0A_2$, $P0A_3$)	V
Output Absorption Current	I_O	10.0	mA
Operating Temperature	T_a	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

5.2 RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Voltage	V_{DD1}	4.5	5.0	5.5	V	With PLL and CPU active
Power Voltage	V_{DD2}	3.5	5.0	5.5	V	With CPU active and PLL not active
Data Retention Voltage	V_{DDR}	2.2		5.5	V	No crystal oscillation
Power Voltage Rising Time	T_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Magnitude	Vin1	0.5		V_{DD}	V_{P-P}	VCOL, VCOH
Input Magnitude	Vin2	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Maximum Output Voltage	V_{BDS}	0.0		16.0	V	$P1B_1$ to $P1B_3$, LPF_{OUT}
Operating Temperature	T_a	−40		85	°C	

5.3 ELECTRIC CHARACTERISTICS

(T_a = −40 to +85 °C and V_{DD} = 4.5 to 5.5 V, RH ≦ 70 %, unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Rower Voltage	V_{DD1}	4.5	5.0	5.5	V	With CPU and PLL active
Power Voltage	V_{DD2}	3.5	5.0	5.5	V	With CPU active and PLL not active
Power Current	I_{DD1}		1.2	2.4	mA	With CPU active and PLL not active Positive wave input (fin = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C X_{IN} pin
Power Current	I_{DD2}		0.45	0.90	mA	With CPU active and PLL not active HALT instruction in use (execute 20 instructions per 1 ms) Positive wave input (fin = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C X_{IN} pin
Data Retention Voltage	V_{DDR1}	3.5	5.0	5.5	V	Use electrical blackout detection by timer F/F Crystal oscillation
Data Retention Voltage	V_{DDR2}	2.2	5.0	5.5	V	Use electrical balckout detection by timer F/F No crystal oscillation
Data Retention Voltage	V_{DDR3}	2.0	5.0	5.5	V	Data memory (RAM) retention
Data Retention Current	I_{DDR1}		5	15	μA	No crystal oscillation T_a=25 °C
Data Retention Current	I_{DDR2}		5	10	μA	No crystal oscillation V_{DD}=5.0 V, T_a=25 °C
Intermediate Level Output Voltage	V_{CM1}	2.3	2.5	2.7	V	COM_0, COM_1 V_{DD}=5 V
High Level Output Voltage	V_{IH1}	0.8 V_{DD}	0.6 V_{DD}		V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$ to $P1A_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High Level Output Voltage	V_{IH2}	0.6 V_{DD}	0.5 V_{DD}		V	$P0D_0$ to $P0D_3$
Low Level Output Voltage	V_{IL1}		0.4 V_{DD}	0.2 V_{DD}	V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1D_0$ to $P1D_3$, CE, INT_0, INT_1
High Level Output Current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$ to $P0A_1$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1C_0$ to $P1C_3$, $P1B_0$ V_{OH}=V_{DD}−1 V
High Level Output Current	I_{OH2}	−1.0	−4.0		mA	LCD_0 to LCD_{29}, EO_0, EO_1 V_{OH}=V_{DD}−1 V

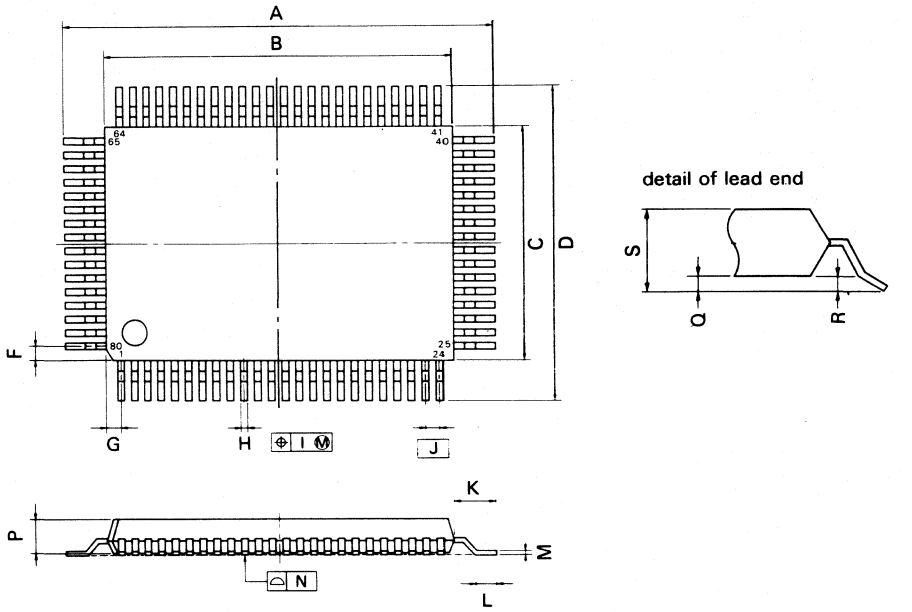
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Low Level Output Current	I_{OL1}	1.0	7.0		mA	$P0A_0$, $P0A_1$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1C_0$ to $P1C_3$, $P1B_0$ $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL2}	1.0	3.5		mA	LCD_0 to LCD_{29}, EO_0, EO_1 $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL3}	1.0	2.0		mA	$P1B_1$ to $P1B_3$ $V_{OL}=1$ V
Low Level Output Current	I_{OL4}	1.0	10.0		mA	$P0A_2$, $P0A_3$ $V_{OL}=1$ V
High Level Input Current	I_{IH1}	0.1	0.8		mA	VCOH at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH2}	0.1	0.8		mA	VCOL at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH3}	0.1	1.3		mA	X_{IN} at pull-down $V_{IH}=V_{DD}$
High Level Input Current	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ to $P0D_3$ at pull-down $V_{IH}=V_{DD}$
Maximum Output Voltage	V_{BDS}	0		16	V	$P1B_1$ to $P1B_3$, LPF_{OUT}
Output Off-Leak Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ $V_{OH}=V_{DD}$
Output Off-Leak Current	I_{L2}			500	nA	$P1B_1$ to $P1B_3$ $V_{OH}=16$ V
Output Off-Leak Current	I_{L3}			100	nA	EO_0, EO_1 $V_{OH}=V_{DD}$, $V_{OL}=0$ V
AD Conversion Resolution				6	bit	
AD Conversion Absolute Accuracy			1	1.5	LSB	$T_a=-10$ to 50 °C
Operating Frequency	f_{in1}	0.5		30	MHz	VCOL MF mode Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in2}	5		40	MHz	VCOL HF mode Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in3}	9		150	MHz	VCOH Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in4}	9		250	MHz	VCOH Positive wave input $V_{IN}=0.5$ V_{P-P}
Operating Frequency	f_{in5}	0.1		1	MHz	AMIFC Positive wave input $V_{IN}=0.3$ V_{P-P}
Operating Frequency	f_{in6}	5		15	MHz	FMIFC Positive wave input $V_{IN}=0.3$ V_{P-P}

(Reference characteristics)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Current	I_{DD3}		15		mA	With CPU and PLL active VCOH Positive wave input fin = 150 MHz, Vin = 0.5 V_{P-P}, V_{DD} = 5 V, T_a = 25 °C
High Level Output Current	I_{OH4}		−0.2		mA	COM_0, COM_1 $V_{OH}=V_{DD}-1$ V
Intermediate Level Output Current	I_{OM1}		20		μA	COM_0, COM_1 $V_{OM}=V_{DD}$
Intermediate Level Output Current	I_{OM2}		−20		μA	COM_0, COM_1 V_{OM}=0 V
Low Level Output Current	I_{OL6}		0.2		mA	COM_0, COM_1 V_{OL}=1 V

PACKAGE DIMENSION

80 PIN PLASTIC QFP (14×20)



S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{-0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{-0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{-0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17005GF-3B9

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 220 °C or below, Reflow time: 30 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	IR20-162
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	VP15-162
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	WS60—162
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "partial heating method".

ONE-TIME PROM 4-BIT SINGLE-CHIP MICROCONTROLLER WITH BUILT-IN HARDWARE FOR DIGITAL TUNING SYSTEM

The μPD17P005 is a product with the built-in mask ROM of μPD17005 replaced with the one-time PROM.

μPD17P005 allows the user to write any program and is suitable for prototyping or small volume production in the system development of the μPD17005 or μPD17003A (ROM, RAM scale-down version of μPD17005).

The analog characteristics (PLL) of μPD17P005 are different from the μPD17005 or the μPD17003A cases. Using device really should be evaluated about time constance.

See also μPD17005 or μPD17003A data when reading this data sheet.

FEATURES

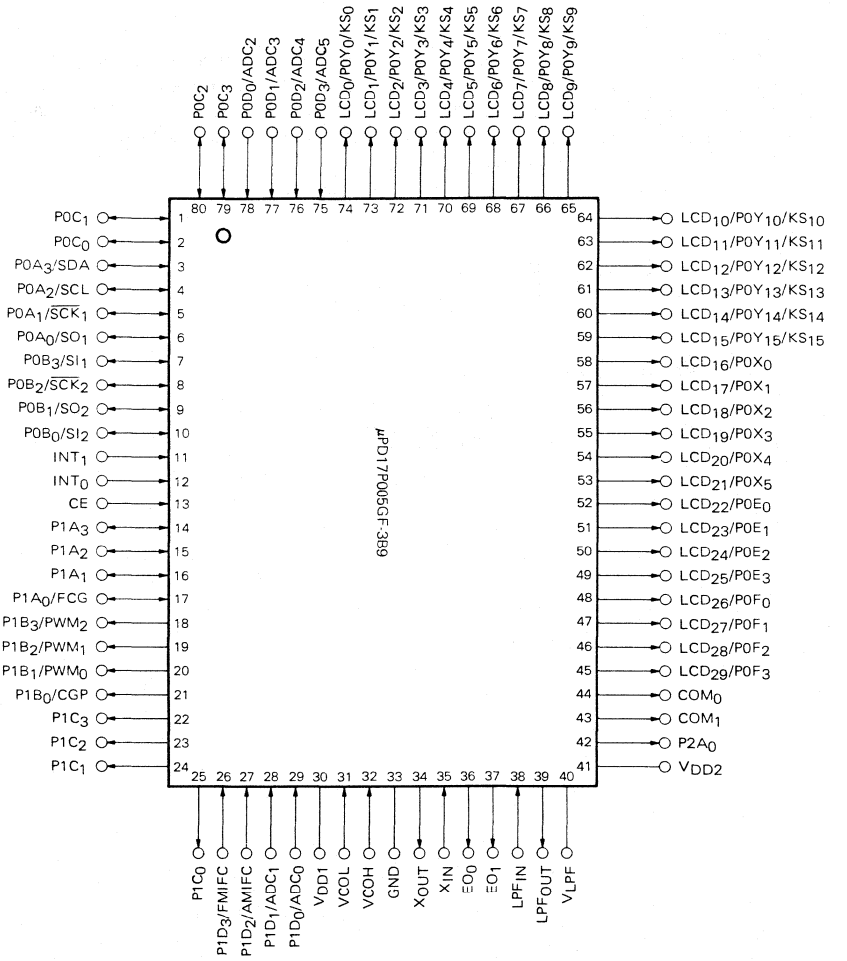
- μPD17005, μPD17003A compatible.
- Built-in one time PROM ROM: 16 KB (7932 steps x 16 bits)
- Single supply 5 V ±10 %

ORDERING INFORMATION

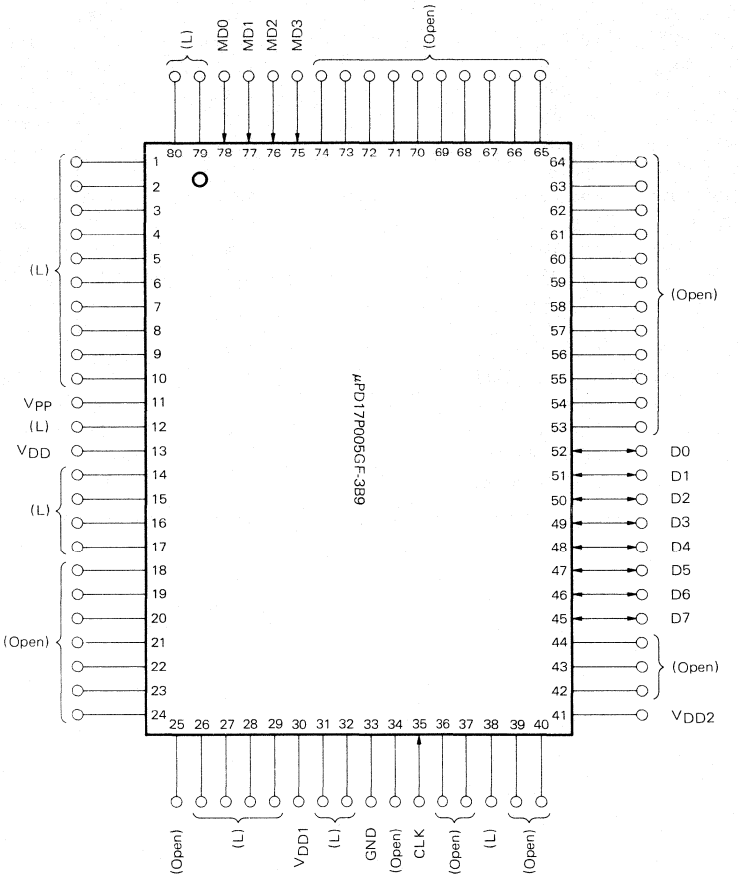
Order Code	Package	Quality Grade
μPD17P005GF-3B9	80-pin plastic QFP (14 x 20)	Standard

PIN CONFIGURATION (Top View)

(1) Normal operation mode



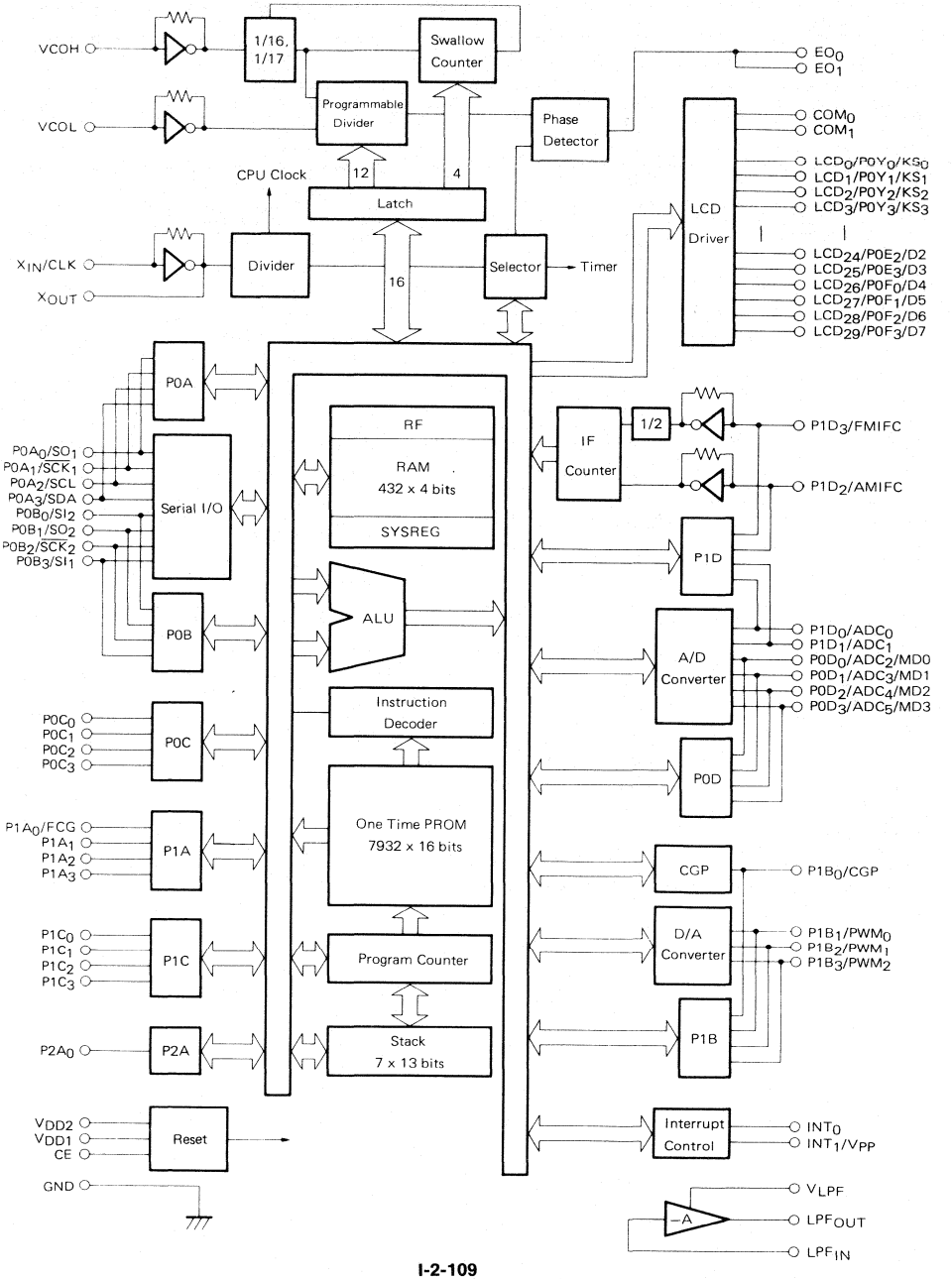
(2) PROM programming mode



Note: ( ): Treatment of pins that are not used in PROM programming mode.
L: Separately connect to respective ground via a resistor (470 Ω)
Open: Do not connect.

$P0A_0$-$P0A_3$	:	Port 0A
$P0B_0$-$P0B_3$	:	Port 0B
$P0C_0$-$P0C_3$	:	Port 0C
$P0D_0$-$P0D_3$	:	Port 0D
$P0E_0$-$P0E_3$	:	Port 0E
$P0F_0$-$P0F_3$	:	Port 0F
$P0X_0$-$P0X_5$	:	Port 0X
$P0Y_0$-$P0Y_{15}$	:	Port 0Y
$P1A_0$-$P1A_3$	:	Port 1A
$P1B_0$-$P1B_3$	:	Port 1B
$P1C_0$-$P1C_3$	:	Port 1C
$P1D_0$-$P1D_3$	:	Port 1D
$P2A_0$	:	Port 2A
SDA	:	Serial data input/output
SCL	:	Serial clock input/output
$\overline{SCK}_1$, $\overline{SCK}_2$	:	Serial clock input/output
SO_1, SO_2	:	Serial data output
SI_1, SI_2	:	Serial data input
INT_0, INT_1	:	External interrupt input
CE	:	Chip enable input
FCG	:	External gate counter input
PWM_0-PWM_2	:	D/A converter output
CGP	:	Clock generator port
FMIFC	:	Frequency counter input
AMIFC	:	Frequency counter input
ADC_0-ADC_5	:	A/D converter input
VCOL	:	Local oscillation low input
VCOH	:	Local oscillation high input
X_{IN}, X_{OUT}	:	Crystal resonator connecting pin
EO_0, EO_1	:	Error-out output
LPF_{IN}	:	LPF amplifier input
LPF_{OUT}	:	LPF amplifier output
COM_0, COM_1	:	LCD common signal output
LCD_0-LCD_{29}	:	LCD segment signal output
KS_0-KS_{15}	:	Key source signal output
CLK	:	Clock input for PROM
MD0-MD3	:	Mode selection for PROM
D0-D7	:	Data input/output for PROM
V_{PP}	:	Power Supply for PROM
V_{LPF}	:	LPF amplifier source
V_{DD1}, V_{DD2}	:	Power source
GND	:	Ground

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 Port Pin

Pin Name	Input/ output	Dual function pin (*)	Function	Reset
$P0A_0$	Input/ output	SO_1	4-bit input/output port (Port 0A) Input/output settable in 1-bit.	Input
$P0A_1$		$\overline{SCK}_1$		
$P0A_2$		SCL	N-ch open-drain. 5 V withstand voltage	
$P0A_3$		SDA		
$P0B_0$	Input/ output	SI_2	4-bit input/output port (Port 0B) Input/output settable in 1-bit.	Input
$P0B_1$		SO_2		
$P0B_2$		$\overline{SCK}_2$		
$P0B_3$		SI_1		
$P0C_0$–$P0C_3$	Input/ output	–	4-bit input/output port (Port 0C) Input/output settable in 1-bit.	Input
$P0D_0$–$P0D_3$	Input	ADC_2–ADC_5 (MD0–MD3)	4-bit input port (Port 0D) Pull-down resistor built-in.	–
$P0E_0$–$P0E_3$	Output	LCD_{22}–LCD_{25} (D0–D3)	4-bit output port (Port 0E)	–
$P0F_0$–$P0F_3$	Output	LCD_{26}–LCD_{29} (D4–D7)	4-bit output port (Port 0F)	–
$P0X_0$–$P0X_5$	Output	LCD_{16}–LCD_{21}	6-bit output port (Port 0X)	–
$P0Y_0$–$P0Y_{15}$	Output	LCD_0/KS_0–LCD_{15}/KS_{15}	16-bit output port (Port 0Y)	–
$P1A_0$	Input/ output	FCG	4-bit input/output port (Port 0A) Input/output settable in 1-bit.	Input
$P1A_1$–$P1A_3$		–		
$P1B_0$	Output	CGP	4-bit output port (Port 1B)	–
$P1B_1$–$P1B_3$		PWM_0–PWM_2	N-ch open-drain. 16 V withstand voltage	
$P1C_0$–$P1C_3$	Output	–	4-bit output port (Port 1C)	–
$P1D_0$	Input	ADC_0	4-bit input port (Port 1D)	–
$P1D_1$		ADC_1		
$P1D_2$		AMIFC		
$P1D_3$		FMIFC		
$P2A_0$	Output	–	1-bit output port (Port 2A)	–

*: Pins in parentheses are dual function pins in PROM programming mode.

1.2 Pin for Other Than Port (In Normal Operation Mode)

Pin Name	Input/output	Dual function pin (*)	Function	Reset
SO_1	Output	$P0A_0$	Serial data output pin	Input
$\overline{SCK}_1$	Input/output	$P0A_1$	Serial clock input/output pin	
SCL	Input/output	$P0A_2$	Serial clock input/output pin	
SDA	Input/output	$P0A_3$	Serial data input/output pin	
SI_2	Input	$P0B_0$	Serial data input pin	Input
SO_2	Output	$P0B_1$	Serial data output pin	
$\overline{SCK}_2$	Input/output	$P0B_2$	Serial clock input/output pin	
SI_1	Input	$P0B_3$	Serial data input pin	
INT_0	Input	–	Edge-sensitive vector interrupt input pin (detection edge selectable)	–
INT_1		(V_{PP})		
CE	Input	–	Operation select pin and reset signal input pin	–
FCG	Input	$P1A_0$	External gate counter input pin	–
CGP	Output	$P1B_0$	Clock generator port output pin	–
PWM_0–PWM_2	Output	$P1B_1$–$P1B_3$	D/A converter output pin. N-ch open-drain. 16 V withstand voltage	–
ADC_0–ADC_1	Input	$P1D_0$–$P1D_1$	Analog input pin to D/A converter	–
ADC_2–ADC_5		$P0D_0$–$P0D_3$ (MD0–MD3)	Key source signal return output pin	
COM_0, COM_1	Output	–	Common signal output pin of LCD controller/ Driver	–
LCD_0–LCD_{15}	Output	$P0Y_0/KS_0$–$P0Y_{15}/KS_{15}$	Segment signal output pin of LCD controller/ Driver	–
LCD_{16}–LCD_{21}		$P0X_0$–$P0X_5$		
LCD_{22}–LCD_{25}		$P0E_0$–$P0E_3$ (D0–D3)		
LCD_{26}–LCD_{29}		$P0F_0$–$P0F_3$ (D4–D7)		
KS_0–KS_{15}	Output	$LCD_0/P0Y_0$–$LCD_{15}/P0Y_{15}$	Key source signal output pin of key matrix	–
AMIFC	Input	$P1D_2$	Frequency counter input pin	–
FMIFC		$P1D_3$		
VCOL	Input	–	Local oscillation frequency input pin	–
VCOH		–		
X_{IN}	Input	(CLK)	Crystal resonator	–
X_{OUT}	Output	–		
EO_0	Output	–	Charge pump output pin of PLL frequency synthesizer	–
EO_1				
LPF_{IN}	Input	–	Amplifier input pin for low-pass filter	–
LPF_{OUT}	Output	–	Amplifier output pin for low-pass filter N-ch open-drain. 16 V withstand voltage	–

Pin Name	Input/ output	Dual function pin (*)	Function	Reset
V_{LPF}	–	–	Amplifier supply pin for low-pass filter	–
V_{DD1}	–	–	Device supply pin. 6 V applied in program memory write/read/verify mode.	–
V_{DD2}				
GND	–	–	Ground pin	–

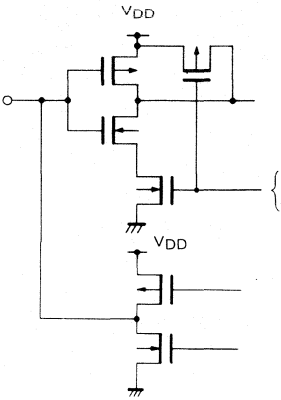
*: Pins in parentheses are dual function pins in PROM programming mode.

1.3 Pin for Other Than Port (In PROM Programming Mode)

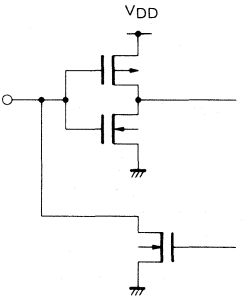
Pin Name	Input/output	Dual function pin	Function	Reset
CLK	Input	X_{IN}	Clock input pin at program memory write/ read/verify.	–
D_0–D_7	Input/output	$LCD_{22}/P0E_0$–$LCD_{29}/P0F_3$	Data input/output pin at program memory write/read/verify.	–
MD0–MD3	Input	$P0D_0/ADC_2$–$P0D_3/ADC_5$	Operation mode select pin at program memory write/read/verify.	–
V_{PP}	–	INT_1	Program voltage application pin at program memory write/read/verify. 12.5 V applied at program memory write/read/ verify. Used as INT_1 pin in normal operation mode.	–

1.4 Equivalent Circuit for Pin

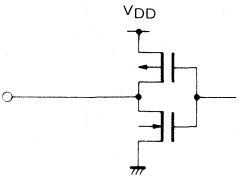
1.4.1 P0A ($P0A_1/\overline{SCK}_1$, $P0A_0/SO_1$)
P0B ($P0B_3/SI_1$, $P0B_2/\overline{SCK}_2$, $P0B_1/SO_2$, $P0B_0/SI_2$)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$) (Note)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
D0-D7
} (Input/Output)



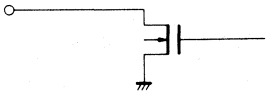
1.4.2 P0A ($P0A_3$/SDA, $P0A_2$/SCL) (Input/output)



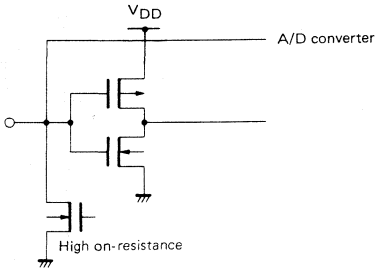
1.4.3 P1B ($P1B_0$/CGP)
P1C ($P1C_3$, $P1C_2$, $P1C_1$, $P1C_0$)
P2A ($P2A_0$)
$LCD_0/P0Y_0/KS_0$-$LCD_{29}/P0F_3$
} (Output)



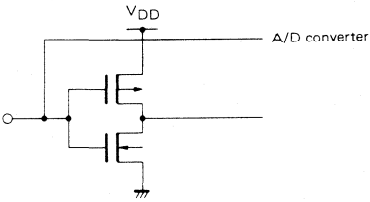
1.4.4 P1B (P1B$_3$/PWM$_2$, P1B$_2$/PWM$_1$, P1B$_1$/PWM$_0$) (Output)



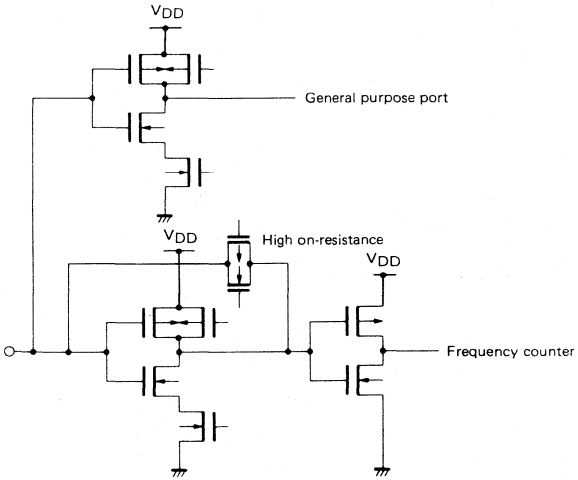
1.4.5 P0D (P0D$_3$/ADC$_5$/MD3, P0D$_2$/ADC$_4$/MD2, P0D$_1$/ADC$_3$/MD1, P0D$_0$/ADC$_2$/MD0) (Input)



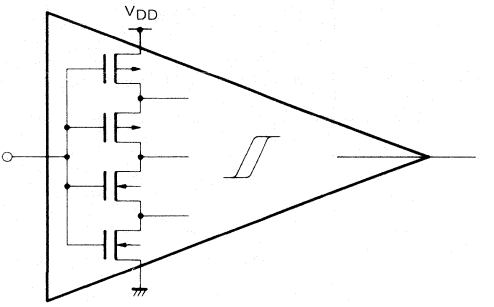
1.4.6 P1D (P1D$_1$/ADC$_1$, P1D$_0$/ADC$_0$) (Input)



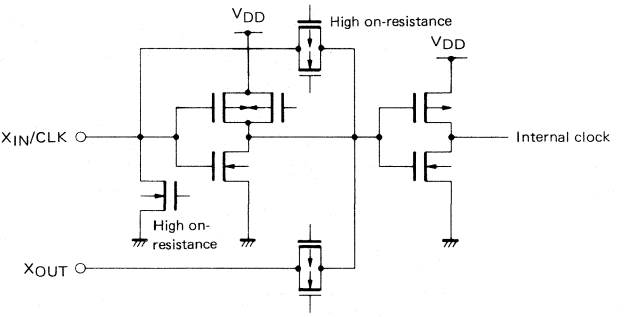
1.4.7 P1D (P1D$_3$/FMIFC, P1D$_2$/AMIFC) (Input)



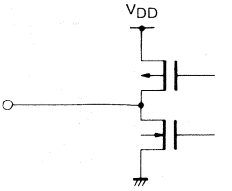
1.4.8 CE, INT_1/V_{PP}, INT_0 (Schmitt triggered input)



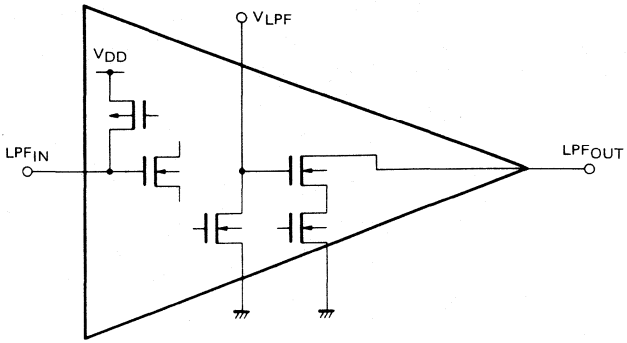
1.4.9 X_{OUT} (Output), X_{IN}/CLK (Input)



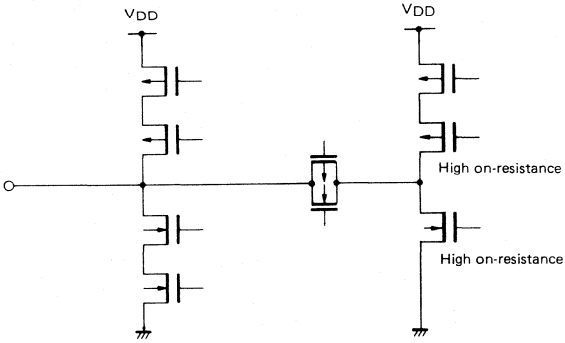
1.4.10 EO_1, EO_0 (Output)



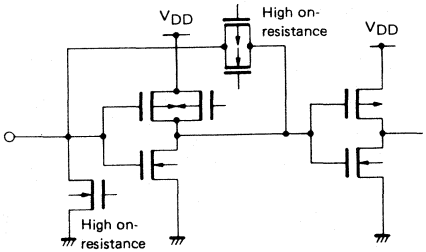
1.4.11 LPF_{IN} (Input), LPF_{OUT} (Output), V_{LPF}



1.4.12 COM_1, COM_0 (Output)



1.4.13 VCOH, VCOL (Input)



2. FUNCTION LIST

Item \ Model	μPD17003A	μPD17005	μPD17P005
ROM (x 16 bits)	3836	7932	7932 (PROM)
Table reference area	256	7932	
RAM (x 4 bits)	320	432	
Data buffer	4		
General register	16		
System register	12 nibbles		
Register file	33 nibbles (control register)		
General-purpose port register	24 nibbles		
Insturction execution time	4.44 μs (4.5 MHz crystal resonator used)		
Stack level	7-level (stack operation available)		
General-purpose port: Input/output port	16 units		
General-purpose port: Input port	8 units		
General-purpose port: Output port	9 units (+30: LCD segment pin)		
Clock generator port	1 unit		
LCD controller/driver	• 30 segments, 2 commons 1/2 duty, 1/2 bias, frame frequency 250 Hz, drive voltage V_{DD} 16 segment pins, also working as key source All of 30 segments can be used as output ports. (4, 4, 6, 16 segments: independently settable.)		
Serial interface	• 2 systems 8-bit 3-wire: 2-channel 8-bit 2-wire: 1-channel		
D/A converter	• 8-bits x 3 (PWM output, output withstand voltage 16 V max.)		
A/D converter	• 6 bits x 6 (successive approximation by software)		
Interrupt	• 5 channels (Maskable interrupt) External interrupt: 2 channels (INT_0 pin, INT_1 pin) Internal interrupt: 3 channels (timer, serial interface 1, frequency counter)		
Timer	• 2 systems Timer carry FF (1, 5, 100, 250 ms) Timer interrupt (1, 5, 100, 250 ms)		
Reset function	• Power-ON reset (at power on) • Reset by CE pin (CE pin goes from low to high.) • Power failure detection function		

Item \ Model		μPD17003A	μPD17005	μPD17P005
PLL frequency synthesizer	Dividing method	• 2 types: Direct dividing method: (VCOL pin 20 MHz max.) Pulse swallowing: (VCOL pin 40 MHz max.) (VCOH pin 250 MHz max.)		
	Reference frequency	• 12 types selectable by program. 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz		
	Charge pump	• Two independent error-out output		
	Phase comparator	• Unlock detection available by program. Unlock FF delay time selectable.		
	Amplifier for LPF	• CMOS operational amplifier, output withsatnd voltage 16 V max.		
Frequency counter		• Frequency measurement $P1D_3$/FMIFC pin: 5 to 15 MHz $P1D_2$/AMIFC pin: 0.1 to 1 MHz • External gate width measurement $P0A_1$/FCG pin		
Supply voltage		• V_{DD} = 4.5 to 5.5 V (PLL and CPU operations) • V_{DD} = 3.5 to 5.5 V (PLL stop, CPU operation) • V_{DD} = 2.2 to 5.5 V (Crystal resonator stop)		
Package		80-pin plastic QFP		

3. WRITE/READ/VERIFY THE ONE-TIME PROM (PROGRAM MEMORY)

The program memory built in μPD17P005 is a 15864 x 8-bit electrically writable one-time PROM. This PROM is accessed in 1-word, 16-bit in normal operation mode and in 1-word, 8-bit in program memory write/read/verify mode. In this case, the upper 8 bits of 1-word, 16 bits are allocated to even address and the lower 8 bits to odd address, respectively.

At PROM write/read/verify, set to PROM mode and use those pins shown in Table 3-1.

Addresses are updated by the clock input from the CLK pin instead of the address input.

Table 3-1 Pins to be used at program memory write/read/verify

Pin Name	Function
V_{PP}	Program voltage application pin. 12.5 V applied. Used as INT1 pin in normal operation mode.
CLK	Address update clock input pin
MD0–MD3	Operation mode select pin
D0–D7	8-bit data input/output pin
V_{DD1}, V_{DD2}	Supply voltage application pin. 6 V applied 5 V ±10 % applied in normal operation mode.

The built-in PROM is written using the specified PROM programmer and dedicated program adapter. Use the following PROM programmer and program adapter.

PROM programmer: AF-9703 (Ando Electric Co.)
AF-9704 (Ando Electric Co.)

Program adapter: AF-9803 (Ando Electric Co.)

3.1 Operation Mode at Program Memory Write/Read/Verify

The μPD17P005 changes to the program memory write/read/verify mode when +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin.

According to the setting of the MD0–MD3, this mode is set to the operation mode as shown in Table 3-2.

All input pins not used in program memory write/read/verify mode are connected to the ground via the pull-down resistance (470 Ω).

Table 3-2 Operation mode at program memory write/read/verify

Designation of operation mode						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	0 clear of program memory address
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	X	H	H	Program inhibit mode

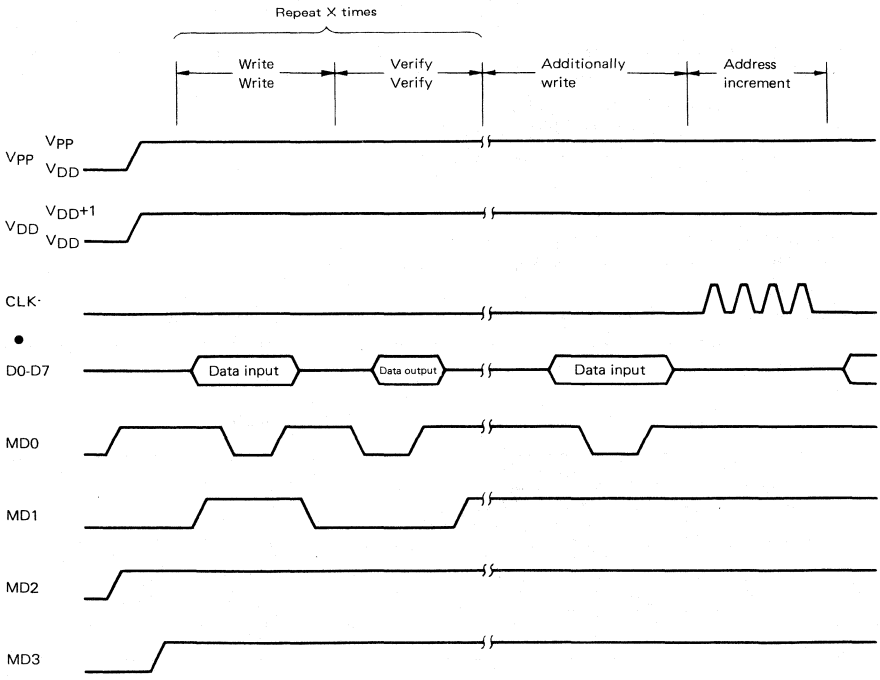
Remark X: L or H

3.2 Program Memory Write Procedure

The program memory write procedure is as follows and High-speed write is avilable.

(1) Pull down the input pins not in use to the ground via the resistance. Set the CLK pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) 0 clear mode of program memory address.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Program inhibit mode
(7) Write data in 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (1) if written. If not, repeat steps (7) to (9).
(10) Times written in (7) to (9): X) x 1 ms additional writing
(11) Program inhibit mode
(12) The program memory address is updated (+1) by inputting 4 pulse signals to the CLK pin.
(13) Repeat (7) to (12) up to the final address.
(14) 0 clear mode of program memory address
(15) Change the V_{DD}/V_{PP} pin voltage to 5 V.
(16) Power OFF

Steps (2) to (12) are schematically shown below.

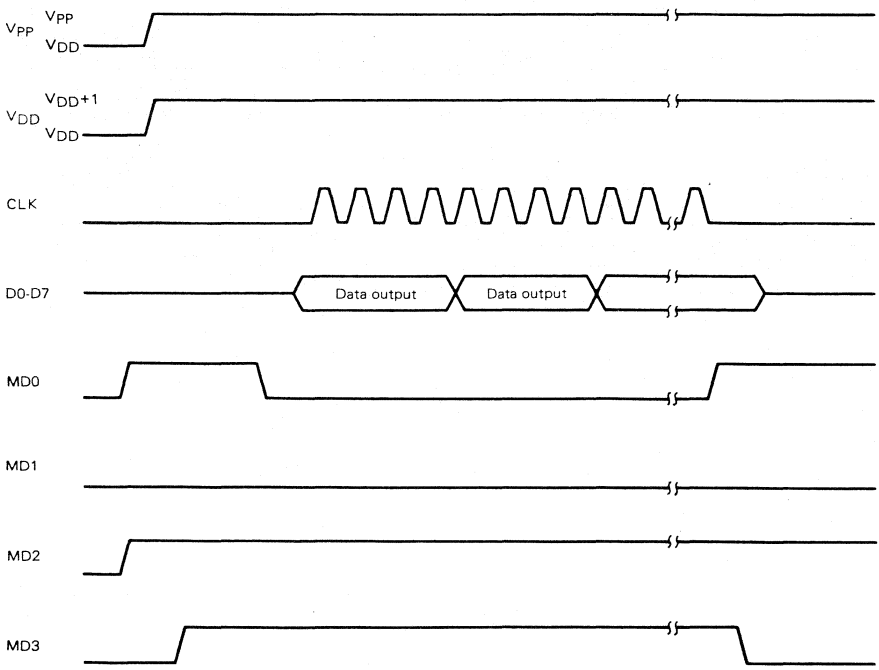


3.3 Program Memory Read Procedure

The μPD17P005 can read the contents of program memory by the following procedures.

(1) Pull down the input pins not in use to the ground via the resistance. Set the CLK pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 μs.
(4) 0 clear mode of program memory address.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Program inhibit mode
(7) Verify mode. Sequentially output the data of one address each time 4 clock pulse signals are input to the CLK pin.
(8) Program inhibit mode
(9) 0 clear mode of program memory address
(10) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(11) Power OFF

Steps (2) to (9) are shown below.



4. ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATING (T_a = 25 ±2 °C)

Supply Voltage	V_{DD}		−0.3 to +6.0	V
Input Voltage	V_I		−0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	Except $P1B_1$–$P1B_3$, $P0A_2$, $P0A_3$, LPF_{OUT}	−0.3 to V_{DD} + 0.3	V
Ouput Withstand Voltage	V_{BDS1}	$P1B_1$–$P1B_3$, LPF_{OUT}	18.0	V
Output Withstand Voltage	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} + 0.3	V
High level Output Current	I_{OH}	1 pin	−12	mA
		All pins	−20	mA
Low Level Output Current	I_{OL}	1 pin	12	mA
		All pins	20	mA
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATION CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU operations
Supply Voltage	V_{DD2}	3.5	5.0	5.5	V	PLL stop, CPU operation
Data Retention Voltage	V_{DDR}	2.2		5.5	V	Crystal resonator stop
Supply Voltage Rise Time	t_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Amplitude	V_{in1}	0.5		V_{DD}	V_{P-P}	VCOL,VCOH
Input Amplitude	V_{in2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output Withstand Voltage	V_{BDS}			16.0	V	$P1B_1$–$P1B_3$, LPF_{OUT}
Operating Temperature	T_{opt}	−40		+85	°C	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL operations
Supply Voltage	V_{DD2}	3.5	5.0	5.5	V	CPU operation, PLL stop
Data Retention Voltage	V_{DDR1}	3.5		5.5	V	At power failure detection by timer F/F. At crystal oscillation.
Data Retention Voltage	V_{DDR2}	2.2		5.5	V	At power failure detection by timer F/F. When crystal oscillation is stopped.
Data Retention Voltage	V_{DDR3}	2.0		5.5	V	Data memory (RAM) Retention
Data Retention Current	I_{DDR1}		2	15	μA	When crystal oscillation is stopped. T_a=25 °C
Data Retention Current	I_{DDR2}		2	10	μA	When crystal oscillation is stopped. V_{DD}=5.0 V, T_a=25 °C
Intermediate Level Output Voltage	V_{OM1}	2.3	2.5	2.7	V	COM_0, COM_1, V_{DD}=5 V
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1D_0$–$P1D_3$, CE, INT_0, INT_1
High Level Input Voltage	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$–$P0D_3$
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD}	V	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P0D_0$–$P0D_3$, $P1A_0$–$P1A_3$, $P1D_0$–$P1D_3$, CE, INT_0, INT_1
High Level Output Current	I_{OH1}	−1.0	−5.0		mA	$P0A_0$, $P0A_1$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1C_0$–$P1C_3$, $P1B_0$, $P2A_0$ V_{OH}=V_{DD}−1 V
High Level Output Current	I_{OH2}	−1.0	−4.0		mA	LCD_0–LCD_{29}, EO_0, EO_1 V_{OH}=V_{DD}−1 V
Low Level Output Current	I_{OL1}	1.0	7.0		mA	$P0A_0$–$P0A_3$, $P0B_0$–$P0B_3$, $P0C_0$–$P0C_3$, $P1A_0$–$P1A_3$, $P1C_0$–$P1C_3$, $P1B_0$, $P2A_0$ V_{OL}=1 V
Low Level Output Current	I_{OL2}	1.0	3.5		mA	LCD_0–LCD_{29}, EO_0, EO_1 V_{OL}=1 V
Low level Output current	I_{OL3}	1.0	2.0		mA	$P1B_1$–$P1B_3$ V_{OL}=1 V
Low Level Output Current	I_{OL4}	1.0	10.0		mA	$P0A_2$, $P0A_3$ V_{OL}=1 V
High Level Input Current	I_{IH1}	0.1	0.8		mA	At VCOH pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH2}	0.1	0.8		mA	At VCOL pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH3}	0.1	1.3		mA	At X_{IN} pull-down. V_{IH}=V_{DD}
High Level Input Current	I_{IH4}	0.05	0.13	0.30	mA	At $P0D_0$–$P0D_3$ pull-down. V_{IH}=V_{DD}
Output Leakage Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ V_{OH}=V_{DD}
Output Leakage Current	I_{L2}			500	nA	$P1B_1$–$P1B_3$, LPF_{OUT} V_{OH}=16 V
Output Leakage Current	I_{L3}			±100	nA	EO_0, EO_1 V_{OH}=V_{DD}, V_{OL}=0 V

AC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{in1}	0.5		30	MHz	VCOL MF mode Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in2}	5		40	MHz	VCOL HF mode Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in3}	9		150	MHz	VCOH Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in4}	0.1		1	MHz	AMIFC Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in5}	0.44		0.46	MHz	AMIFC Sine wave input V_{in} = 0.05 V_{P-P}
Operating Frequency	f_{in6}	5		15	MHz	FMIFC Sine wave input V_{in} = 0.3 V_{P-P}
Operating Frequency	f_{in7}	10.5		10.9	MHz	FMIFC Sine wave input V_{in} = 0.06 V_{P-P}
Analog-to Digital Conversion Resolution				6	bit	
Analog-to-Digital Conversion Total Error			±1	±1.5	LSB	T_a = –10 to +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTIC	SYMBOL	STANDARD VALUE				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply Current	I_{DD3}		15		mA	CPU and PLL operations VCOH sine wave input f_{in} = 150 MHz, V_{in} = 0.5 V_{P-P} V_{DD} = 5 V, T_a = 25 °C
High Level Output Current	I_{OH4}		–0.2		mA	COM_0, COM_1 V_{OH} = V_{DD}–1 V
Intermediate Level Output Current	I_{OM1}		–20		μA	COM_0, COM_1 V_{OM} = V_{DD}–1 V
Intermediate Level Output Current	I_{OM2}		20		μA	COM_0, COM_1 V_{OM} = 1 V
Low Level Output Current	I_{OL5}		0.2		mA	COM_0, COM_1 V_{OL} = 1 V

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			±10	μA	V_{IN} = V_{IL} or V_{IH}
High Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low Level Output Voltage	V_{OL}			1.0	V	I_{OL} = 1 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Be sure to keep V_{PP} below +13.5 V including overshoot.

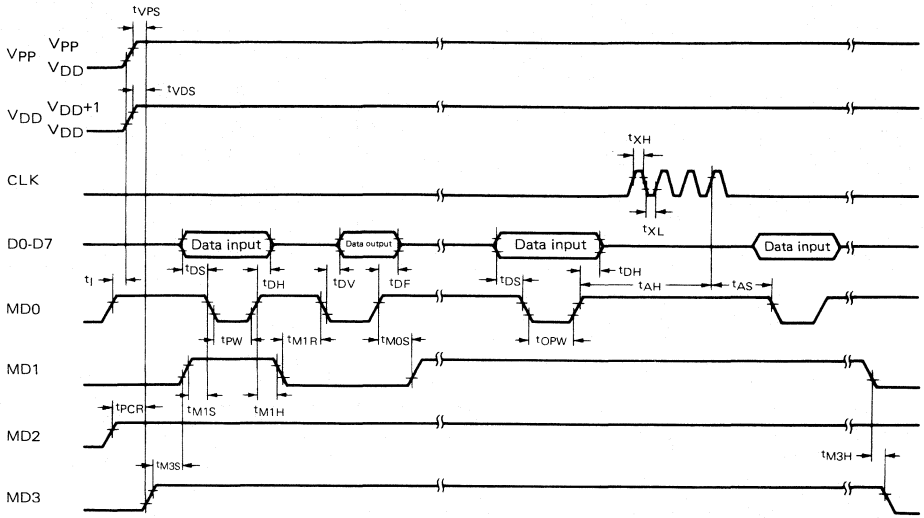
2: Be sure to apply V_{DD} before V_{PP} and cut it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

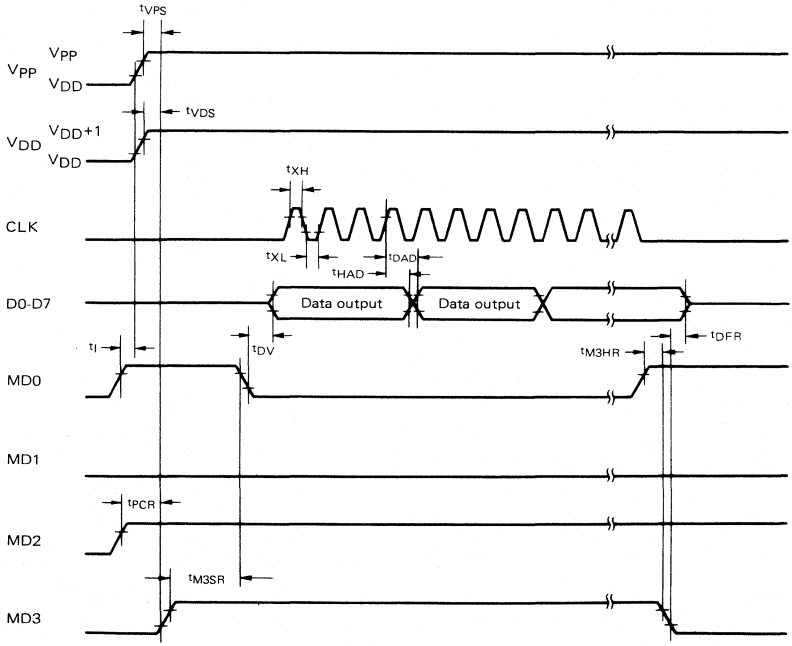
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Setup Time (*) (vs MD0 ↓)	t_{AS}	2			μs	
MD1 Setup Time (vs MD0 ↓)	t_{M1S}	2			μs	
Data Setup Time (vs MD0 ↓)	t_{DS}	2			μs	
Address Hold Time (*) (vs MD0 ↑)	t_{AH}	2			μs	
Data Hold Time (vs MD0 ↑)	t_{DH}	2			μs	
MD0 ↑ to Data Output Float Delay Time	t_{DF}	0		130	ns	
V_{PP} Setup Time (vs MD3 ↑)	t_{VPS}	2			μs	
V_{DD} Setup Time (vs MD3 ↑)	t_{VDS}	2			μs	
Initial Program Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs MD1 ↑)	t_{MOS}	2			μs	
MD0 ↓ to Data Output Delay Time	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs MD0 ↑)	t_{M1H}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recover Time (vs MD0 ↓)	t_{M1R}	2			μs	
Program Counter Reset Time	t_{PCR}	10			μs	
CLK Input High/Low Level Width	t_{XH}, t_{XL}	0.125			μs	
CLK Input Frequency	f_X			4.19	MHz	
Initial Mode Set Time	t_I	2			μs	
MD3 Setup Time (vs MD1 ↑)	t_{M3S}	2			μs	
MD3 Hold Time (vs MD1 ↓)	t_{M3H}	2			μs	
MD3 Setup Time (vs MD0 ↓)	t_{M3SR}	2			μs	At program memory read.
Address (*) to Data Output Delay Time	t_{DAD}	2			μs	At program memory read.
Address (*) to Data Output Hold Time	t_{HAD}	0		130	ns	At program memory read.
MD3 Hold Time (vs MD0 ↑)	t_{M3HR}	2			μs	At program memory read.
MD3 ↓ to Data Output Float Delay Time	t_{DFR}	2			μs	At program memory read.

*: The internal address signal is incremented by one (+1) at the 3rd CLK input fall and is not connected to the pin.

PROGRAM MEMORY WRITE TIMING

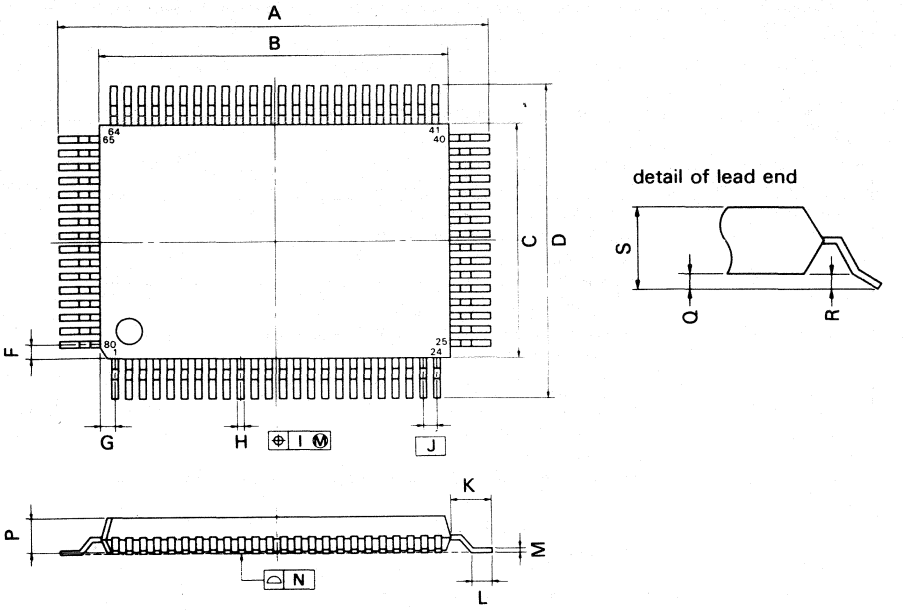


PROGRAM MEMORY READ TIMING



5. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×20)



S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

6. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17P005GF

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	IR30-162
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	VP15-162
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	WS60-162
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17006 is a 4-bit single-chip CMOS microcontroller for use with a digital tuning system.

The CPU employs 17K architecture which enables to directly operate a data memory by one instruction and to control various operations and peripheral hardware. Each instruction is comprised to one 16-bit word.

The peripheral hardware incorporates a variety of input/output ports, a serial interface, a clock generator port, a prescalar for digital tuning, a PLL frequency synthesizer, a timer for remote controlled decoding, etc.

To cope with the RDS (Radio Data System) various timer functions, interrupt functions and external SRAM interface functions are incorporated.

Thus, a high-performance, multi-functional digital tuning sytem can be constructed.

The μPD17P006* having an on-chip one-time PROM is also available for mask ROM product, μPD17006 program evaluation and small production.

An easy-to-use incircuit emulator (IE-17K) and an assembler (AS17K) are available as μPD17006 system development tools.

*: Under development

FEATURES

- 4-bit microcontroller for digital tuning
- Program memory (ROM):
  24K bytes (12288 x 16 bits)
- General-purpose data memory (RAM):
  896 nibbles (896 x 4 bits)
- Instruction execution time:
  1.78 μs (when a 4.5 MHz crystal oscillator is used.)
- Stack level: 7
- A set of 46 easy-to-understand instructions
- Decimal operation enable
- 12K-step table reference enable
- On-chip PLL frequency synthesizer and 150 MHz prescalar
- 12 kinds of reference frequencies can be selected using appropriate programs
- 2-system error output (EO_{00}, EO_{01} and EO_{10} systems)
- On-chip IF counter (AMIFC, FMIFC)
- On-chip 8-bit serial interface
  2 systems with 3 channels:
  2-wire and 3-wire interfaces
- On-chip D/A converter:
  9 bits x 3 channels (PWM output)
  Usable as a modulo timer
- On-chip A/D converter: 8 bits x 6 channels
  Hardware (32 μs) and software conversion
  Also serves as an external event counter.
- Various timer functions
  12-bit modulo timer (remote controlled: 10, 50 μs)
  8-bit module timer (RDS clock synchronization: 10, 100 μs)
  8-bit modulo timer (general-purpose: 10, 100, 500, 1000 μs)
  Timer carry (general-purpose: 100 ms)
- Various interrupts
  External interrupt: 2 channels (INT_1, INT_2 pins)
  Internal interrupt: 4 channels (timer: 3 channels, serial interface: 1 channel)
  Dual-function interrupt:
  2 channels (serial interface: 2 channels, A/d converter, IF counter and timer overflow)
- General-purpose input/output ports
  Input/output port: 48
  Input port: 8 (with 4 on-chip pull-down resistors)
  Output port: 11
- On-chip function of parallel interface with the external SRAM
- On-chip power-ON reset, CE reset and power failure detection circuit
- CMOS Low power consumption
- Supply voltage: 5 V ±10 %
- 80-pin plastic QFP

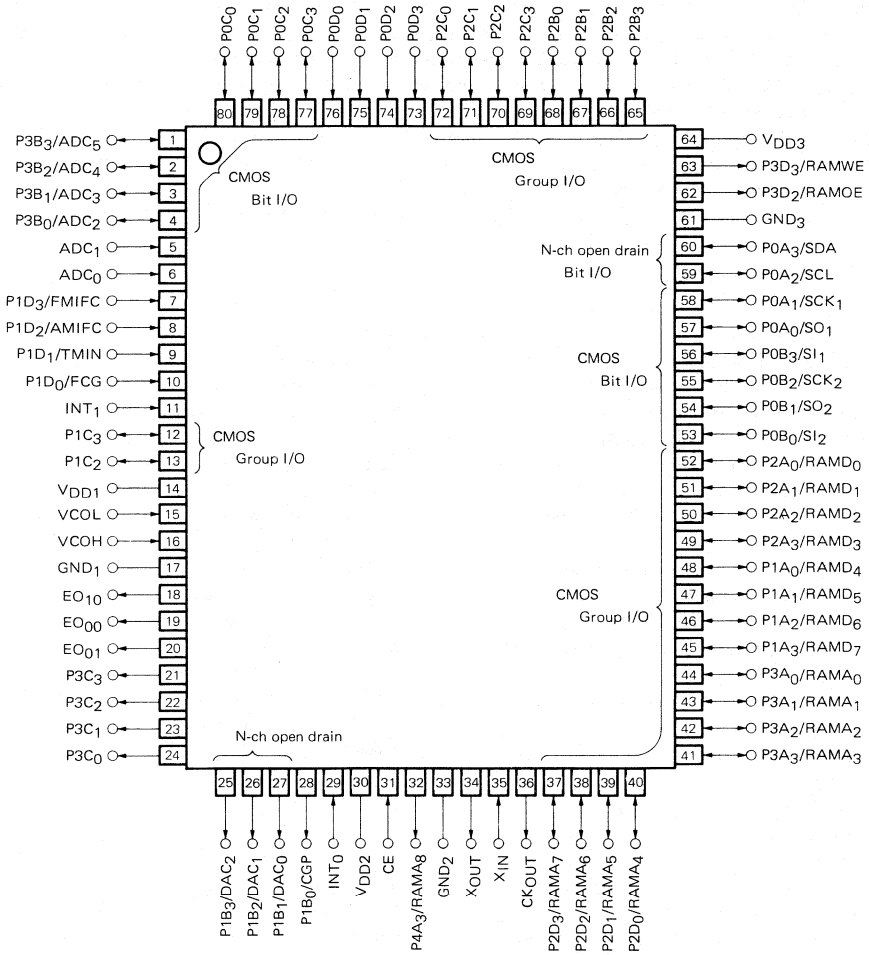
Notes on Serial interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

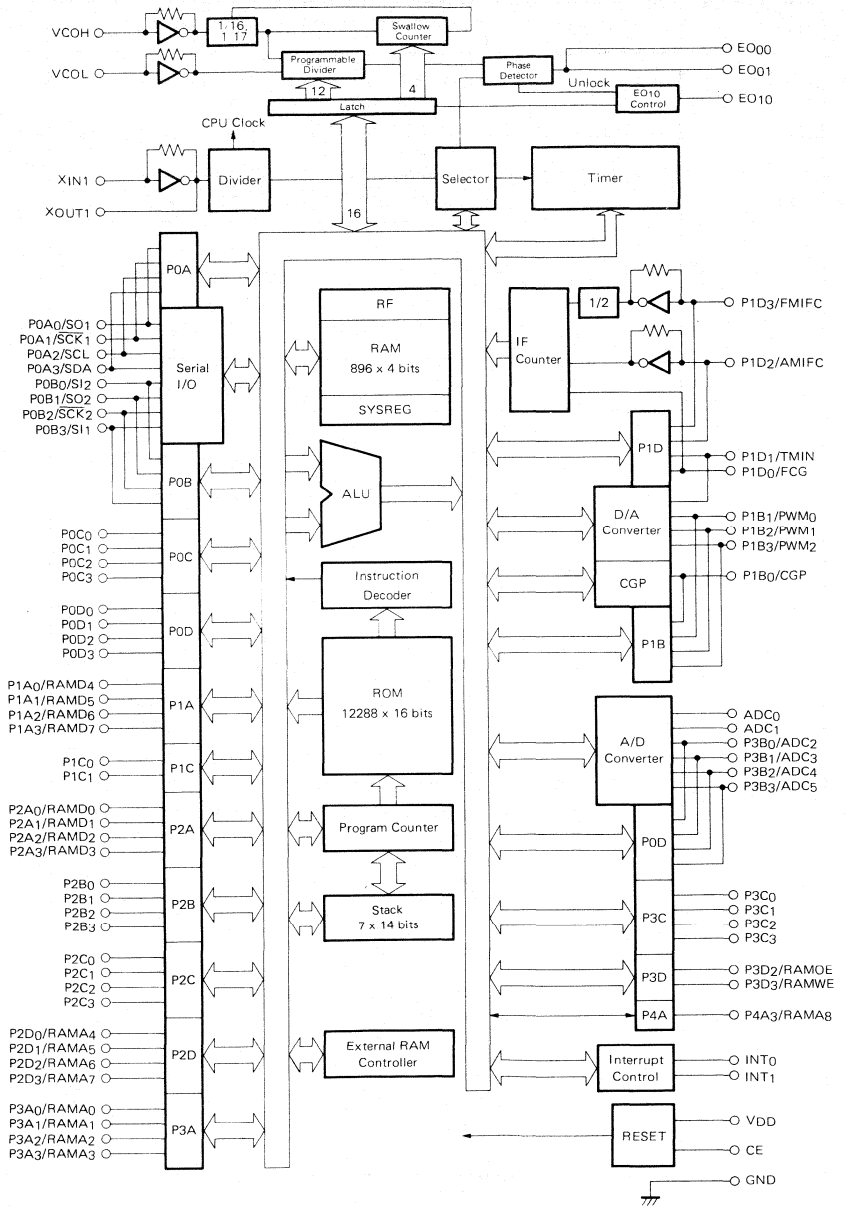
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIRAGRAM



1. Terminal definitions

1.1 Terminal definition summary

<table>
<tr><th>Terminal</th><th>Symbol</th><th>Definition</th><th>Output format</th></tr>
<tr><td>1 - 4</td><td>P3B3/ADC5
–
P3B0/ADC2</td><td>Port 3B and A/D converter output.
• P3B3 - P3B0
- 4-bit CMOS I/O port
• ADC5 - ADC2
- 8-bit resolution CMOS I/O port
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Input (P3B3 - P3B0)</td></tr></table></td><td>CMOS
push-pull</td></tr>
<tr><td>5
6</td><td>ADC1
ADC0</td><td>8-bit resolution A/D converter input.
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Floating</td></tr></table></td><td>–</td></tr>
<tr><td>7
8
9
10</td><td>P1D3/FMIFC
P1D2/AMIFC
P1D1/TM1IN/TM1G1
P1D0/FCG</td><td>Port 1D, frequency counter and event counter, external gate counter input.
• P1D3 - P1D0
- 4-bit input port
• FMIFC, AMIFC
- Frequency counter input
Measurable frequency
<table><tr><th>Input terminal</th><th>Input frequency</th><th>Input amplitude</th></tr><tr><td>P1D3/FMIC</td><td>5-15MHz</td><td>0.3V p-p</td></tr><tr><td>P1D2/AMIF</td><td>0.1-1MHz</td><td>0.3V p-p</td></tr></table>These terminal inputs eliminate the input signal's alternating current component.
• TM1IN
- Event counter input (combined with modulo timer1)
• FCG
- External gate counter input (combined with frequency counter)
• TM1G1
- External gate counter input (combined with modulo timer 1)
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Input (P1D3 - P1D0)</td></tr></table></td><td>–</td></tr>
</table>

1.1 Continued

<table>
<tr><td>11
29</td><td>INT1/TM1G0
INT0</td><td>External interrupt request signal and external gate counter input
• INT1, INT0
- External interrupt request signal inputs
- Rise or fall selectable
• TM1G0
- External gate counter input (combined with modulo timer 1)
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Input (INT1 - INT0)</td></tr></table></td><td>—</td></tr>
<tr><td>12
13</td><td>P1C3
P1C2</td><td>2-bit CMOS output ports.
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Low-level output</td></tr></table></td><td>CMOS push-pull</td></tr>
<tr><td>14
30
64</td><td>VDD0
VDD1
VDD2</td><td>Positive power source.
5V ± 10% is supplied to operate the CPU and peripherals. It is possible to preserve data with 2.2V during a clock stop. The mPD17006 can be reset with the built-in power-on reset circuit when VDD rises.
Do not add a high power source from VDD to any terminals except the VDD terminals (VDD0, VDD1 and VDD2). In particular, take care that VDD and CE rise simultaneously. This becomes a cause of a latch-up.
VDD0 is the power source for the PLL system, and VDD1 and VDD2 are the power sources for the digital system.
VDD1 and VDD2 are not necessarily connected to the same electrical potential.</td><td>—</td></tr>
<tr><td>15
16</td><td>VCOL
VCOH</td><td>Inputs the PLL's local oscillator (VCO) frequency. The divided frequency method is direct division (MF mode) and pulse swallow method (HF mode and VHF mode).
<table><tr><th>Division method</th><th>Input term.</th><th>Input freq. (MHz)</th><th>Input power Vp-p</th><th>Freq. ratio</th></tr><tr><td>Direct division (MF)</td><td>VCOL</td><td>0.5 to 30</td><td>0.3</td><td>16 - 2^{12}-1</td></tr><tr><td>Pulse swallow (HF</td><td>VCOH</td><td>5 to 40</td><td>0.3</td><td>256 - 2^{16}-1</td></tr><tr><td>Pulse swallow (VHF)</td><td>VCOH</td><td>9 to 150</td><td>0.3</td><td>256 - 2^{16}-1</td></tr></table></td><td>—</td></tr>
</table>

1.1 Continued

<table>
<tr><td>17
33
61</td><td>GND0
GND1
GND2</td><td>Ground.
GND0 is the PLL ground, GND1 and GND2 are the digital system grounds.</td><td>–</td></tr>
<tr><td>18
19
20</td><td>EOBST
EO0
EO1</td><td>Output from the frequency synthesizer charge pump.
• EOBST
Error out boost output.
After PLL data is written, if a high level or low level is output through 4 basic synchronous continuity, the high level or low level continues to be output. If a reverse signal is output, it becomes floating.
Selection can be made only through programming.
• EO0, EO1
When an input local oscillator (VCO) frequency gets its divided value from the standard frequency is high at VCOL (pin 15) or VCOH (pin 16), a high level is output from EO0 and EO1, and a low level is output in the case of a low frequency. When they agree, it becomes floating. It makes no difference which of the EO0 and EO1 terminals are used in order to have the same signal output.
Power-on reset | Clock reset | CE reset
Floating</td><td>3-state CMOS</td></tr>
<tr><td>21 - 24</td><td>P3C3 - P3C0</td><td>4-bit CMOS output ports.
Power-on reset | Clock reset | CE reset
Power level output | Reserved</td><td>CMOS push-pull</td></tr>
</table>

1.1 Continued

<table>
<tr>
<td>25 - 27</td>
<td>P1B3/PWM2
-
P1B1/PWM1</td>
<td>Port 1B and D/A converter and clock generator ports.

• P1B3 - P1B0
- 4-bit output port
• PWM2 - PWM0
- D/A converter output
- Various independent signal outputs
- Output method: PWM data establishment

<table>
<tr><th>Function</th><th>Frequency</th><th>Duty</th></tr>
<tr><td>D/A converter</td><td>4.390 kHz</td><td>$\frac{0.25 + X}{512} \times 100\%$ (x = 0 - 511)</td></tr>
</table>
</td>
<td>N-channel open-drain 16V</td>
</tr>
<tr>
<td>28</td>
<td>P1B0/CGP</td>
<td>• CGP
- Clock generator port
- Data establishment for both VDP (variable-duty pulse) and SG (signal generator) functions

<table>
<tr><th>Function</th><th>Frequency</th><th>Duty</th></tr>
<tr><td>VDP</td><td>269kHz</td><td>$\frac{2 + X}{67} \times 100\%$ (x = 0 - 63)</td></tr>
<tr><td>SG</td><td>18/2(2-X) kHz (X = 0 - 63)</td><td>50%</td></tr>
</table>

<table>
<tr><th>Power-on reset</th><th>Clock reset</th><th>CE reset</th></tr>
<tr><td>Indeterminate data output</td><td colspan="2">Reserved</td></tr>
<tr><td colspan="3">(P1B3 - P1B0)</td></tr>
</table>
</td>
<td>CMOS push-pull</td>
</tr>
</table>

1.1 Continued

<table>
<tr><td>31</td><td>CE</td><td>Selection of mPD17006 operation and reset signal input.
(1) Device operation selection
The PLL frequency synthesizer can be operated when CE is at a high level. The PLL frequency synthesizer is disabled when CE is low. In addition, when CE is low, a low-power backup state is possible as a clock stop condition.

(2) Reset signal input
If CE changes from a low level to a high level, the internal basic timer 0 carry goes to FF, and the device is reset (CD reset).
This terminal receives less than ??ms of low level or high level in order to prevent operating errors due to noise. In addition, this terminal can detect inout sighal levels via programming. It cannot detect changes in input signal high or low levels below ??ms.
This terminalbecomes a Schmitt trigger having hysteresis characteristics
Do not high power from VDD when committing tne power source.</td><td>–</td></tr>
<tr><td>32</td><td>P3D3/RAMA8</td><td>Address output for accessing port 3D and ERAM.

• P3D3
- 1-bit output port
• RAMA8
- ERAM address output
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Low-level output (P3D3)</td></tr></table></td><td>Output
push-pull</td></tr>
<tr><td>34</td><td>XOUT</td><td rowspan="2">Crystal oscillator connection.
Connect 4.5MHz crystal oscillator</td><td>CMOS push-pull</td></tr>
<tr><td>35</td><td>XIN</td><td>–</td></tr>
<tr><td>36</td><td>CKOUT</td><td>Clock output for external microcomputer.
Outputs 4.5MHz sine wave (output amplitude is ??Vp-p.
<table><tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr><tr><td colspan="3">Low-level output</td></tr></table></td><td>Output
push-pull</td></tr>
</table>

1.1 Continued

37 - 40 41 - 44	P2D3/RAMA7 - P2D0/RAMA4 P3A3/RAMA3 - P3A0/RAMA0	Address outputs for accessing port 2D, port 3A and ERAM. • P2D3 - P2D0 - 4-bit CMOS I/O port - Can be established as input/output in 4-bit units • P3A3 - P3A0 - 4-bit CMOS I/O port - Can be established as input/output in 4-bit units • RAMA7 - RAMA0 - ERAM address output Power-on reset | Clock reset | CE reset Input (P2D3 - P2D0, P3A3 -P3A0)	CMOS push-pull

Note: Refer to Appendix A when connecting the crystal oscillator.

45 - 48 49 - 52	P1A3/RAMD7 - P1A0/RAMD4 P2A3/RAMD3 - P2A0/RAMD0	I/O that performs port 1A, port 2A and SRAM data read and write. • P1A3 - P1A0 - 4-bit CMOS I/O port - Can be established as input/output in 1-bit units • P2A3 - P2A0 - 4-bit CMOS I/O port - Can be established as input/output in 1-bit units • RAMD7 - RAMD0 - External SRAM data I/O Power-on reset | Clock reset | CE reset Input (P1A3 - P1A0, P2A3 - P2A0)	CMOS push-pull

1.1 Continued

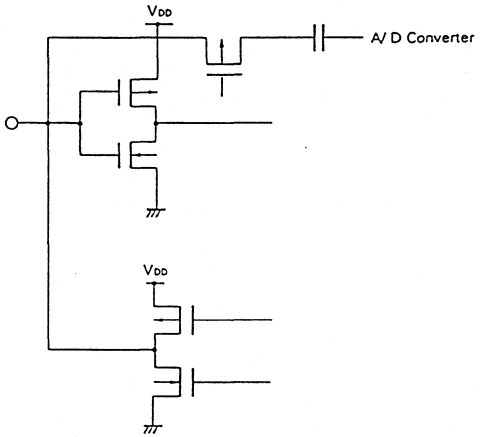
<table>
<tr>
<td>53
54
55
56
57
58</td>
<td>P0B0/SI1
P0B1/SO1
P0B2/$\overline{SCK1}$
P0B3/SI0
P0A0/SO0
P0A1/$\overline{SCK0}$</td>
<td>P0B, P0A and serial interface I/O
• P0B0 - P0B3
- 4-bit CMOS I/O port
- Can be established as input/output in 1-bit units
• P0A0 - P0A3
- 4-bit CMOS I/O port
- Can be established as input/output in 1-bit units
• SDA, SCL
- SDA: Serial data I/O
- SCL: Serial clock I/O
• $\overline{SCK}$, SO, SI
- $\overline{SCK}$: Serial data clock I/O
- SO: Serial data output
- SI: Serial data input
• $\overline{SCK}$, SO, SI
- $\overline{SCK}$: Serial clock I/O
- SO: Serial data output
- SI: Serial data input
Serial interface operating mode
<table>
<tr><th>Terminal designation</th><th colspan="2">Operating mode</th></tr>
<tr><td>P0A3/SDA</td><td rowspan="2">2 lines</td><td rowspan="4">Serial interface 0</td></tr>
<tr><td>P0A2/SCL</td></tr>
<tr><td>P0A1/$\overline{SCK0}$</td><td rowspan="2">3 lines</td></tr>
<tr><td>P0A0/SO0</td></tr>
<tr><td>P0B2/$\overline{SCK1}$</td><td rowspan="3">3 lines</td><td rowspan="3">Serial interface 1</td></tr>
<tr><td>P0B1/SO1</td></tr>
<tr><td>P0B0/SI1</td></tr>
</table>
<table>
<tr><td>Power-on reset</td><td>Clock reset</td><td>CE reset</td></tr>
<tr><td colspan="3">Input
(P0B0 - P0B3, P0A0 - P0A3)</td></tr>
</table>
</td>
<td>CMOS push-pull</td>
</tr>
<tr>
<td>59
60</td>
<td>P0A2/SCL
P0A3/SDA</td>
<td></td>
<td>N-channel open drain</td>
</tr>
</table>

1 Continued

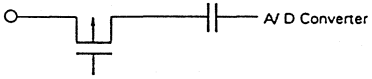
62 63	P4A2/RAM0B P4A3/RAMWE	Port 4A and external SRAM read/write signal output. • P4A2, P4A3 - 2-bit CMOS output port • RAM0E, RAMWE - RAM0E: External SRAM read signal output - RAMWE: External SRAM write signal output Power-on reset | Clock reset | CE reset Low level output (P4A2, P4A3)	CMOS push-pull
65 - 68	P2B3 - P2B0	4-bit CMOS I/O port. Can be established as input/output in 4-bit units. Power-on reset | Clock reset | CE reset Input	CMOS push-pull
69 - 72	P2C3 - P2C0	4-bit CMOS I/O port. Can be established as input/output in 4-bit units. Power-on reset | Clock reset | CE reset Input	CMOS push-pull
73 - 76	P0D0 - P0D3	4-bit input port. Power-on reset | Clock reset | CE reset Input	CMOS push-pull
77 - 80	P0C3 - P0C0	4-bit CMOS I/O port. Can be established as input/output in 4-bit units. Power-on reset | Clock reset | CE reset Input	CMOS push-pull

1.2 PIN EQUIVALENT CIRCUITS

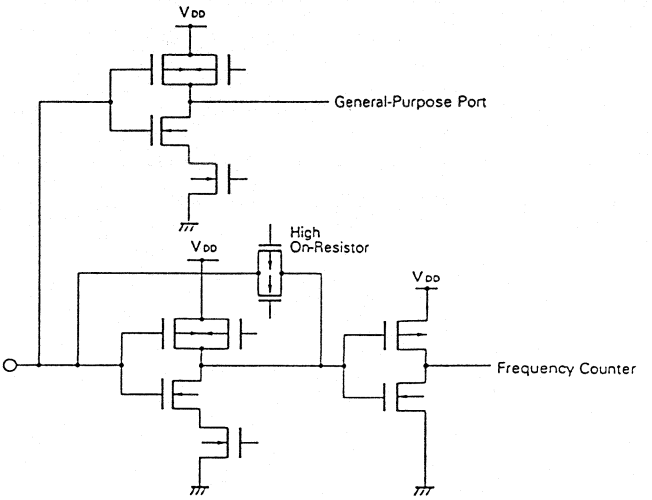
(1) P3B (P3B3/ADC5, P3B2/ADC4, P3B1/ADC3, P3B0/ADC2) (input/output)



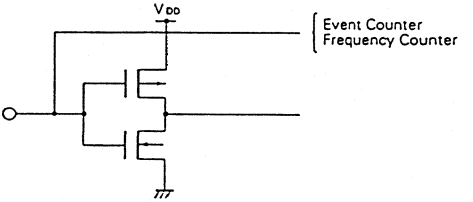
(2) ADC1, ADC0 (input)



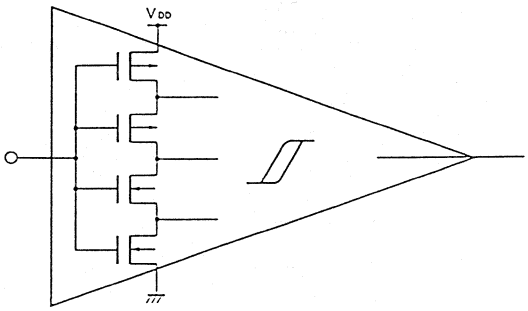
(3) P1D (P1D3/FMIFC, P1D2/AMIFC) (input)



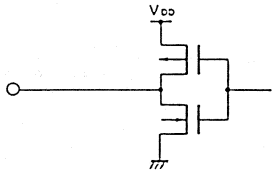
(4) P1D (P1D1/TM1IN, P1D0/FCG) (input)



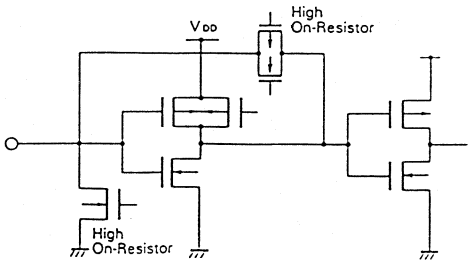
(5) CE, INT1, INT0 (hysteresis input)



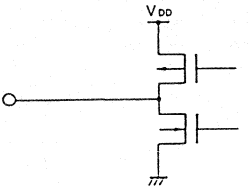
(6) P1C (P1C3, P1C2)
P3C (P3C3, P3C2, P3C1, P3C0)
P1B (P1B0/CGP)
P3D (P3D3/RAMA8)
P4A (P4A3/RAMWE, P4A2/ RAMOE)
(output)



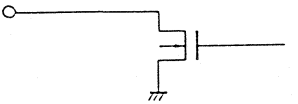
(7) VCOH, VCOL (input)



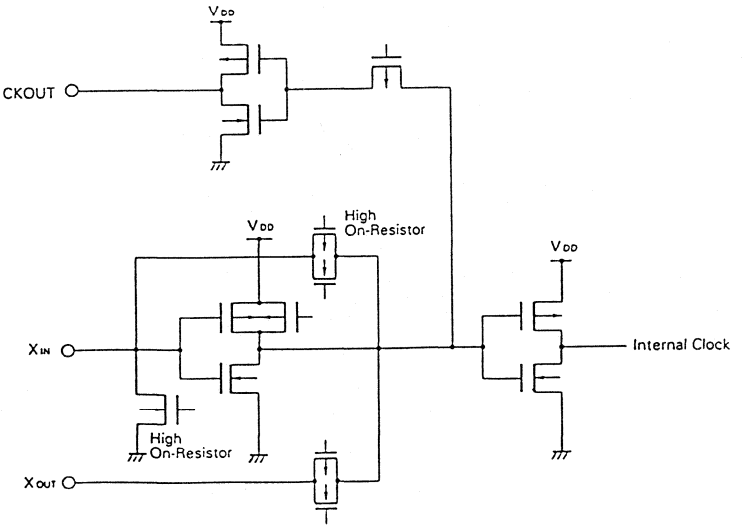
(8) EO_{10}, EO_{00}, EO_1 (output)



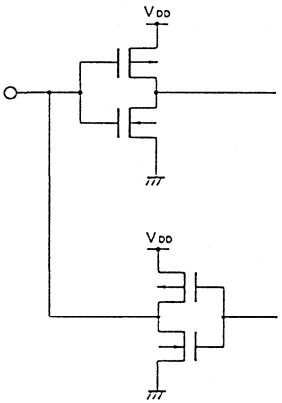
(9) P1B (P1B3/PWM2, P1B2/PWM1, P1B1/PWM0) (output)



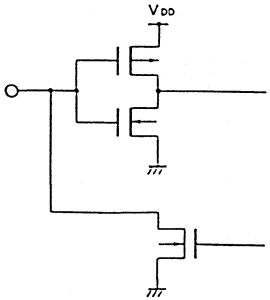
(10) X_{OUT} (output), X_{IN} (input), CKOUT (output)



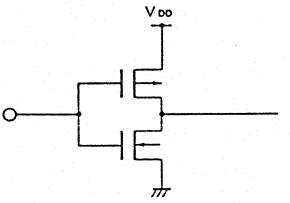
(11) P2D ($P2D_3$/$RAMA_7$, $P2D_2$/$RAMA_6$, $P2D_1$/$RAMA_5$, $P2D_0$/$RAMA_4$)
P3A ($P3A_3$/$RAMA_3$, $P3A_2$/$RAMA_2$, $P3A_1$/$RAMA_1$, $P3A_0$/$RAMA_0$)
P1A ($P1A_3$/$RAMD_7$, $P1A_2$/$RAMD_6$, $P1A_1$/$RAMD_5$, $P1A_0$/$RAMD_4$)
P2A ($P2A_3$/$RAMD_3$, $P2A_2$/ $RAMD_2$, $P2A_1$/$RAMD_1$, $P2A_0$/$RAMD_0$)
P0B ($P0B_3$/SI_0, $P0B_2$/$\overline{SCK_1}$, $P0B_1$/SO_1, $P0B_0$/SI_1)
P0A ($P0A_1$/$\overline{SCK_0}$, $P0A_0$/SO_0)
P2B ($P2B_3$, $P2B_2$, $P2B_1$, $P2B_0$)
P2C ($P2C_3$, $P2C_2$, $P2C_1$, $P2C_0$)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
} (input/output)



(12) P0A ($P0A_3$/SDA, $P0A_2$/SCL) (input/output)



(13) P0D ($P0D_3$, $P0D_2$, $P0D_1$, $P0D_0$) (input)



μPD17006 ELECTRICAL CHARACTERISTICS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C Unless otherwise specified)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to $+V_{DD}$+0.3	V
Output Voltage	V_O	−0.3 to $+V_{DD}$+0.3 (Excluding POA_2, POA_3, $P1B_1$∼$P1B_3$)	V
Output Withstand Voltage	V_{BDS1}	−0.3 to 13 ($P1B_1$∼$P1B_3$)	V
Output Withstand Voltage	V_{BDS2}	−0.3 to V_{DD}+0.3 (POA_2, POA_3)	V
High Level Output Current	I_{OH}	−10 (One pin)	mA
		−20 (All pin)	mA
Low Level Output Current	I_{OL}	10 (One pin)	mA
		20 (All pin)	mA
Total Loss	Pt	450	°C
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}	CPU and PLL are operating	4.5	5.0	5.5	V
Supply Voltage	V_{DD2}	CPU is operating, PLL is OFF	4.5	5.0	5.5	V
Data Retention Voltage	V_{DDR}	Crystal oscillation stopped	2.3		5.5	V
Supply Voltage Rising Time	t_{rise}	VDD = 0 to 4.5V			500	ms
Input Oscillation Voltage	V_{in1}	VCOL, VCOH pin	0.5		V_{DD}	Vp-p
Input Oscillation Voltage	V_{in2}	FMIFC, AMIFC pin	0.5		V_{DD}	Vp-p
Output Withstand Voltage	V_{BDS}	$P1B_1$∼$P1B_3$ pin	0.0		12.0	V
Operating Temperature	T_{opt}		−40		+85	°C

DC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V Ta = -40 to +85 °C RH ≦ 70% Unless otherwise specified)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD1}	CPU and PLL is operating	4.5	5.0	5.5	V
Supply Voltage	V_{DD2}	CPU is operating, PLL is OFF	4.0	5.0	5.5	V
Supply Current	I_{DD1}	CPU is operating, PLLis OFF, X_{IN} pin sine wave input (f_{in}=4.5MHz, $V_{in}=V_{DD}$) V_{DD}=5V, Ta=25°C		3.0	6.0	mA
Supply Current	I_{DD2}	CPU is operating, PLLis OFF, HALT instruction is used (20instructions excused per 1ms) X_{IN} pin sine wave input (f_{in}=4.5MHz, $V_{in}=V_{DD}$) V_{DD}=5V, Ta=25°C		1.5	2.0	mA
Data Retention Voltage	V_{DDR1}	Crystal oscillation is operating Power failure detection by TMCY	3.5		5.5	V
Data Retention Voltage	V_{DDR2}	Crystal oscillation is stopped Power failure detection by TMCY	2.3		5.5	V
Data Retention Voltage	V_{DDR3}	Data memory(RAM) retention	2.0		5.5	V
Data Retention Current	I_{DDR1}	Crystal oscillation stopped Ta=25°C		2	10	μA
High Level input Voltage	V_{IH1}	NOTE 1	$0.8V_{DD}$			V
Low Level input Voltage	V_{IL}	NOTE 1			$0.2V_{DD}$	V
High Level Output Current	I_{OH1}	NOTE 2	- 1.0	- 2.0		mA
High Level Output Current	I_{OH2}	EO_0, EO_1, EOBST $V_{OH}=V_{DD}$-1V	- 1.0	- 3.0		mA
Low Level Output Current	I_{OL1}	NOTE 2	1.0	2.0		mA
Low Level Output Current	I_{OL2}	EO_0, EO_1, EOBST V_{OL}=1V	1.0	3.0		mA
Low Level Output Current	I_{OL3}	$P1B_1$～$P1B_3$ V_{OL}=1V	1.0	2.0		mA
Low Level Output Current	I_{OL4}	POA_2, POA_3 V_{OL}=1V	1.0	10.0		mA

NOTE 1: POA0 TO POA3, POB0 TO POB3, POC0 TO POC3, POD0 TO POD3, P2A0 TO P2A3, P2B0 TO P2B3, P2C0 TO P2C3, P2D0 TO P2D3, P3A0 TO P3A3, P3B0 TO P3B3, CE. INT0, INT1

NOTE 2: POA0, POA1, POB0 TO POB3, POC0 TO POC3, P1A0 TO P1A3, P1B0, P1C2, P2A0 TO P2A3, P2B0 TO P2B3, P2C0 TO P2C3, P2D0 TO P2D3, P3A0 TO P3A3, P3B0 TO P3B3, P3C0 TO P3C3, P3D3, P4A2, P4A3

27.4 AC CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V, Ta = -40 to +85 ℃, RH ≦ 70% Unless otherwise specified)

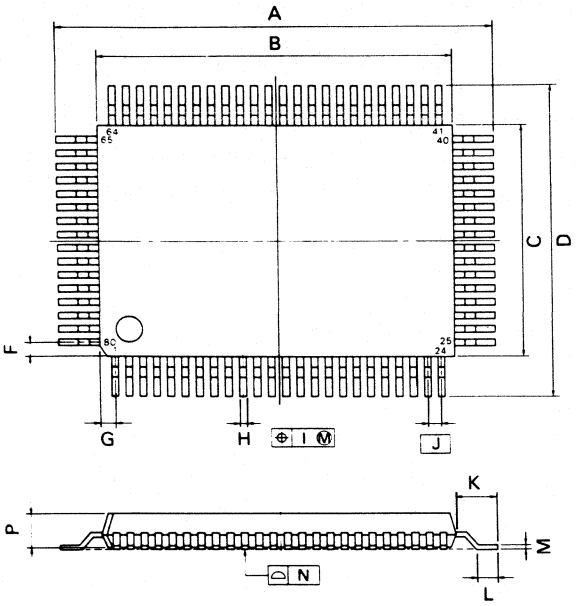
ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Current	I_{IH1}	VCOH pull-down $V_IH=V_{DD}$	0.1	0.8		mA
High Level Input Current	I_{IH2}	VCOH pull-down $V_IH=V_{DD}$	0.1	0.8		mA
High Level Input Current	I_{IH3}	XIN pull-down $V_IH=V_{DD}$	0.1	1.3		mA
Output OFF Leak Current	I_{L1}	POA_2, POA_3 $V_{OH}=V_{DD}$			1	μA
Output OFF Leak Current	I_{L2}	$P1B_1$～$P1B_3$ V_{OH}=13V			1	μA
Output OFF Leak Current	I_{L3}	EO_0, EO_1, EOBST $V_{OH}=V_{DD}$, V_{OL}=0V			±1	μA
A/D Converter Resolution					8	bit
A/D Converter Absolute Accuracy		Ta=-10 to +50℃		±1.5		LSB
Operating Frequency	f_{in1}	VCOL, MF mode(sine wave) V_{in}=0.3Vp-p	0.5		25	MHz
Operating Frequency	f_{in2}	VCOH(sine wave) V_{in}=0.3Vp-p	15		150	MHz
Operating Frequency	f_{in3}	AMIFC(sine wave) V_{in}=0.3Vp-p	0.1		1	MHz
Operating Frequency	f_{in4}	FMIFC(sine wave) V_{in}=0.3Vp-p	5		15	MHz

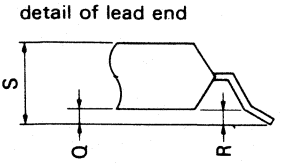
27.5 REFERENCE ELECTRICAL CHARACTERISTICS

Supply Current	I_{DD3}	CPU and PLL are operating VCOH(sine wave), f_{in}=150MHz, V_{in}=0.3Vp-p V_{DD}=5V, Ta=25℃		15		mA

PACKAGE DIMENSION

80 PIN PLASTIC QFP (14×20)





S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{-0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{-0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{-0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	$0.15^{-0.10}_{0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

ONE-TIME PROM VERSION 4-BIT SINGLE-CHIP MICROCONTROLLER WITH DEDICATED ON-CHIP DIGITAL TUNING SYSTEM HARDWARE

The μPD17P006 is a version of the μPD17006 in which the on-chip mask ROM is replaced by one-time PROM.

Since the μPD17P006 can be programmed by the user, it is suitable for pre-production use in μPD17006 system development and for limited production.

This data sheet should be read in conjunction with documentation on the μPD17006.

The electrical specifications (Supply current, etc.) and PLL analog characteristics of the μPD17P006 differ from those of the μPD17006. Please note these differences before undertaking volume production design of an application set.

FEATURES

- μPD17006 compatible
- On-chip one time PROM: 12288 × 16 bits
- Operating voltage range: 5 V ± 10 %

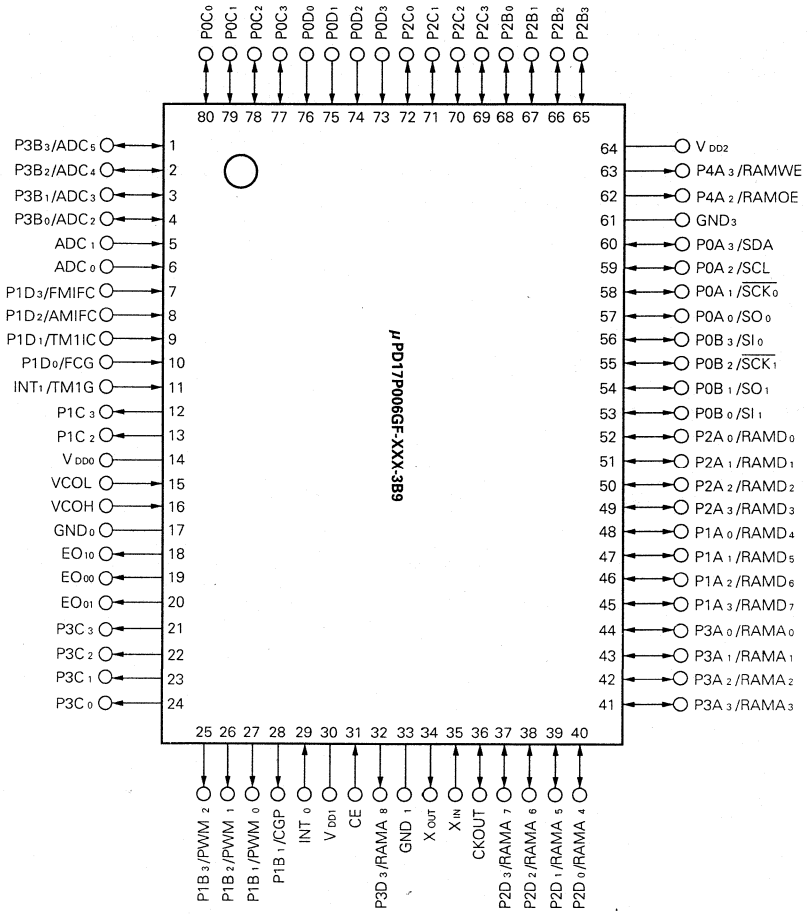
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P006GF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)	Standard

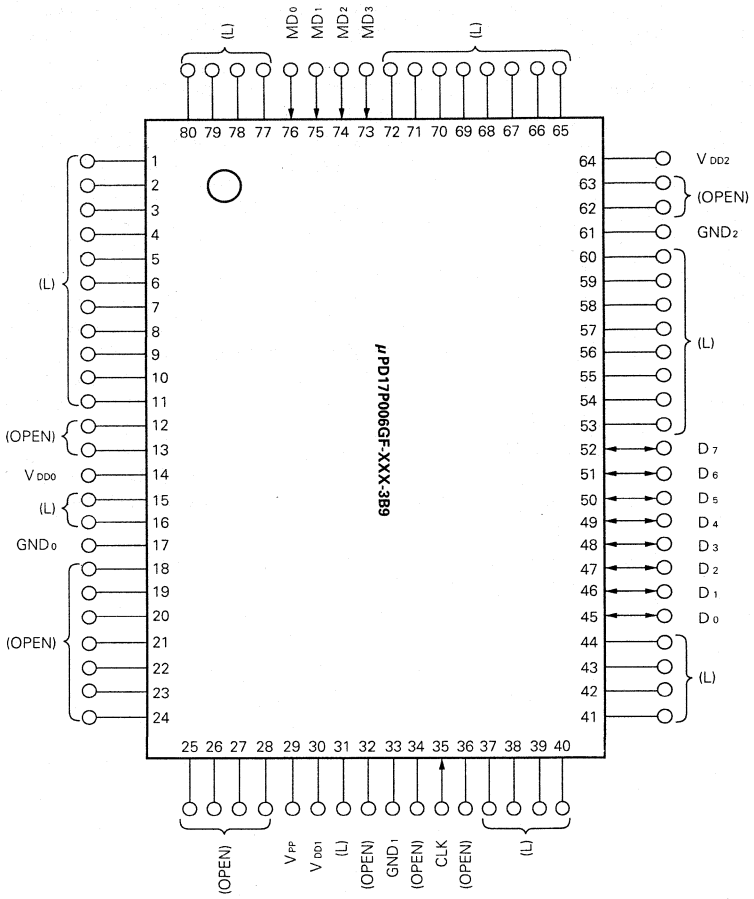
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION (TOP View)

(1) Normal operating mode



(2) PROM Programming mode



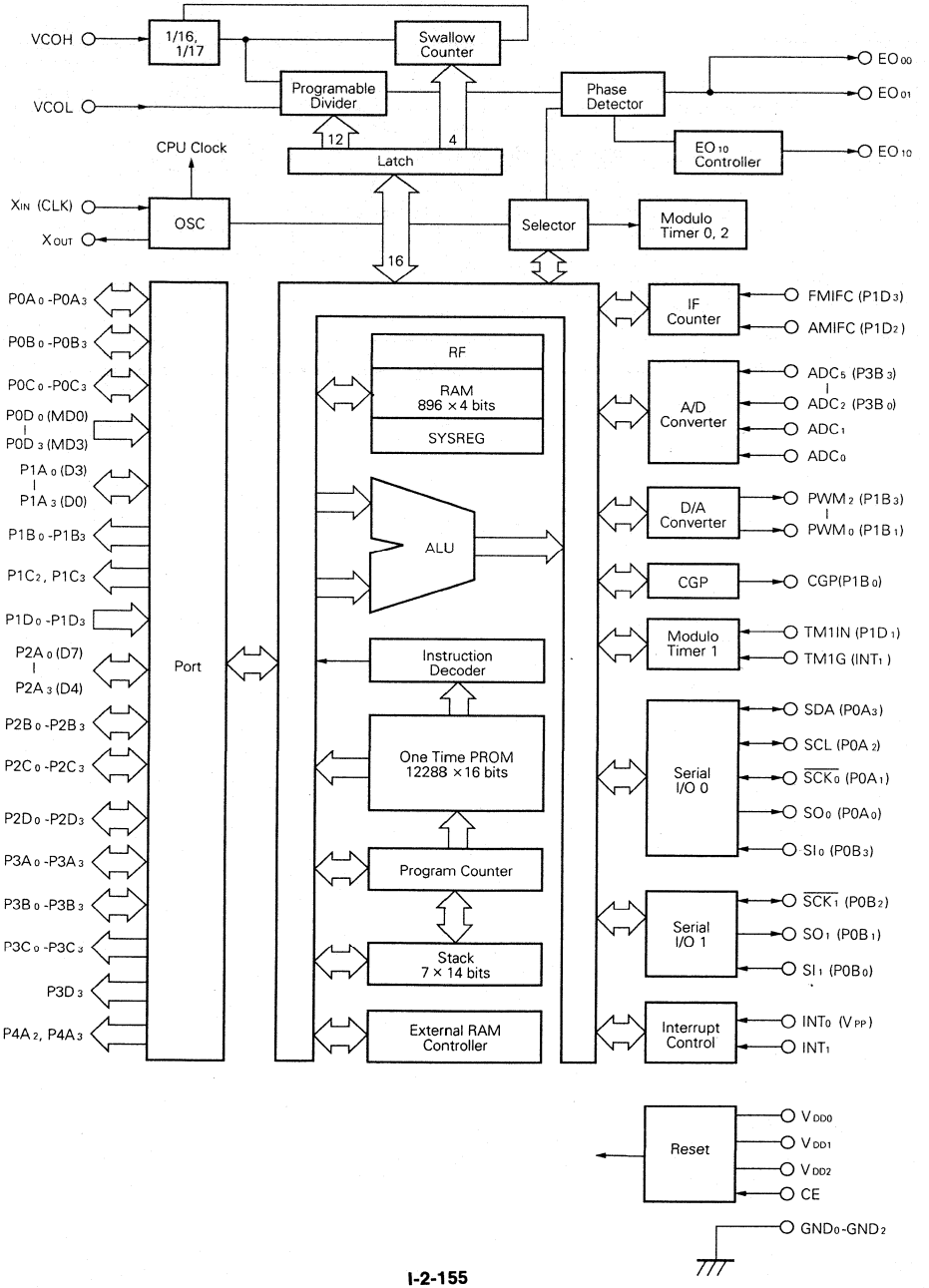
Note **Item in parentheses indicate the recommended conditions for unused pins in the PROM programming mode.**

L : Connect to GND via an individual resistor (470 Ω).

OPEN: Leave open.

$P0A_0$ to $P0A_3$	: Input /output port	AMIFC	: Frequency counter input
$P0B_0$ to $P0B_3$	: Input /output port	TM1IN	: Event counter input
$P0C_0$ to $P0C_3$	: Input /output port	TM1G	: External gate counter input
$P0D_0$ to $P0D_3$	: Input port	FCG	: External gate counter input
$P1A_0$ to $P1A_3$	: Input /output port	CGP	: Clock generator port
$P1B_0$ to $P1B_3$	: Output port	VCOL	: Local oscillation low input
$P1C_2$, $P1C_3$	: Output port	VCOH	: Local osillation high input
$P1D_0$ to $P1D_3$	: Input port	EO_{10}	: Error out output
$P2A_0$ to $P2A_3$	: Input /output port	EO_{00}, EO_{01}	: Error output
$P2B_0$ to $P2B_3$	: Input /output port	INT_0, INT_1	: External interrupt request signal inputs
$P2C_0$ to $P2C_3$	: Input /output port		
$P2D_0$ to $P2D_3$	: Input /output port	CE	: Chip enable input
$P3A_0$ to $P3A_3$	: Input /output port	X_{IN}, X_{OUT}	: Main clock oscillator
$P3B_0$ to $P3B_3$	: Input /output port	CKOUT	: Clock output
$P3C_0$ to $P3C_3$	: Output port	$RAMA_0$ to $RAMA_8$	: External SRAM address outputs
$P3D_3$	: Output port	$RAMD_0$ to $RAMD_7$	: External SRAM data input/outputs
$P4A_2$, $P4A_3$	: Output port	RAMOE	: External SRAM read signal output
ADC_0 to ADC_5	: A/D converter inputs	RAMWE	: External SRAM write signal output
PWM_0 to PWM_2	: D/A converter outputs	CLK	: PROM clock input
SDA	: Serial data input/output	MD0 to MD3	: PROM mode selection inputs
SCL	: Serial clock input /output	D_0 to D_7	: PROM data input /outputs
$\overline{SCK_0}$, $\overline{SCK_1}$	: Serial clock input /outputs	V_{PP}	: PROM power supply
SO_0, SO_1	: Serial data outputs	V_{DD0} to V_{DD2}	: Power supply
SI_0, SI_1	: Serial data inputs	GND_0 to GND_2	: Ground
FMIFC	: Frequency counter input		

BLOCK DIAGRAM



Differences between μPD17P006 and μPD17006

(T_a = 25 °C)

Parameter			μPD17P006		μPD17006	
			TYP.	MAX.	TYP.	MAX.
Supply current [mA]	IDD1	CPU and PLL in operation X_{IN} pin sine-wave input f_{IN} = 4.5 MHz, V_{IN} = V_{DD}	3.0	6.0	1.2	2.4
	IDD2	CPU in operation, PLL stopped, HALT instruction used 20 instructions executed per ms X_{IN} pin sine-wave input f_{IN} = 4.5 MHz, V_{IN} = V_{DD}	2.5	5.0	0.5	0.9
Data retention current [μA]	IDDR2	Crystal oscillation stopped	2	7	2	5

Remarks Note that PLL analog characteristics also differ to some extent in addition to the above characteristics.

1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET

1 to 4	$P3B_3/ADC_5$ to $P3B_0/ADC_2$	Port 3B and A/D converter input/outputs
		• $P3B_3$ to $P3B_0$
		  • 4-bit CMOS input/output port
		• ADC_5 to ADC_2
		  • 8-bit resolution A/D converter inputs
			CMOS push-pull	Input ($P3B_3$ to $P3B_0$)

5 6	ADC_1 ADC_0	8-bit resolution A/D converter inputs	—	Floating

7
8
9
10
	$P1D_3$/FMIFC
	$P1D_2$/AMIFC
	$P1D_1$/TM1IN
	$P1D_0$/FCG
		Port 1D, frequency counter, RSD counter and event counter, and external gate counter inputs
		• $P1D_3$ to $P1D_0$
		  • 4-bit input port
		• FMIFC, AMIFC
		  • Frequency counter input
		• TM1IN
		  • RDS (radio data system) counter input
		  • Event counter input
		• FCG
		  • External gate counter input
			—	Floating ($P1D_3$ to $P1D_0$)

11	INT_1/TM1G	External interrupt request signal input and external gate counter input
		• INT_1
		  • External interrupt request signal input
		  • Rise or fall selectable
		• TM1G
		  • External gate counter input
			—	Input (INT_1)

12 13	$P1C_3$ $P1C_2$	2-bit CMOS output port	CMOS push-pull	Low-level output
14	V_{DD0}	Positive power supply. Applies 5 V ±10 % in normal operating mode.	—	—
15 16	VCOL VCOH	Input PLL local oscillation frequencies.	—	Input
17	GND_0	Ground	—	—
18 19 20	EO_{10} EO_{00} EO_{01}	Output PLL frequency synthesizer charge pump. Compare local oscillation frequency phases and output the result.[Note]	CMOS 3-state	Floating
21 to 24	$P3C_3$ to $P3C_0$	4-bit CMOS output port	CMOS push-pull	Low-level output

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET

25 to 27 28	$P1B_3/PWM_2$ to $P1B_1/PWM_0$ $P1B_0/CGP$	Port 1B, D/A converter, and clock generator port outputs
		• $P1B_3$ to $P1B_0$
		  • 4-bit output port
		• PWM_2 to PWM_0
		  • D/A converter outputs
		• CGP
		  • Clock generator port
			N-ch open-drain 14 V withstand voltage ($P1B_3/PWM_2$ to $P1B_1/PWM_0$)
			CMOS push-pull ($P1B_0$ to CGP)
				Output undefined data. ($P1B_3$ to $P1B_0$)

29	INT_0	External interrupt request signal input. Either rising or falling edge can be selected as valid interrupt request edge.	—	Input
30	V_{DD1}	Positive power supply. Applies 5 V ±10 % in normal operating mode.	—	—
31	CE	μPD17P006 operation selection and reset signal input.	—	Input

32	$P3D_3/RAMA_8$	Outputs address for accessing port 3D and external SRAM.
		• $P3D_3$
		  • 1-bit output port
		• $RAMA_8$
		  • External SRAM address output
			Output	Low-level output ($P3D_3$)

33	GND_1	Ground	—	—
34 35	X_{OUT} X_{IN}	System clock oscillator. A 4.5 MHz crystal resonator should be connected.	CMOS —	—
36	CKOUT	Clock output for external microcomputer. Output 4.5 MHz.	Output	Low-level output

37 to 40
41 to 44
	$P2D_3/RAMA_7$ to $P2D_0/RAMA_4$
	$P3A_3/RAMA_3$ to $P3A_3/RAMA_0$
		Address outputs for accessing port 2D, port 3A, and external SRAM
		• $P2D_3$ to $P2D_0$
		  • 4-bit CMOS input/output port
		  • Settable as input or output as a 4-bit unit
		• $P3A_3$ to $P3A_0$
		  • 4-bit CMOS input/output port
		  • Settable as input or output as a 4-bit unit
		• $RAMA_7$ to $RAMA_0$
		  • External SRAM address outputs
			CMOS	Input ($P2D_3$ to $P2D_0$, $P3A_3$ to $P3A_0$)

45 to 48
49 to 52
	$P1A_3/RAMD_7$ to $P1A_0/RAMD_4$
	$P2A_3/RAMD_3$ to $P2A_0/RAMD_0$
		Input/output for port 1A, port 2A, and external SRAM data reads/writes
		• $P1A_3$ to $P1A_0$
		  • 4-bit CMOS input/output port
		  • Settable as input or output bit-wise
		• $P2A_3$ to $P2A_0$
		  • 4-bit CMOS input/output port
		  • Settable as input or output bit-wise
		• $RAMD_7$ to $RAMD_0$
		  • External SRAM data input/outputs
			CMOS	Input ($P1A_3$ to $P1A_0$, $P2A_3$ to $P2A_0$)

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET
53 54 55 56 57 58 59 60	$P0B_0/SI_1$ $P0B_1/SO_1$ $P0B_2/\overline{SCK_1}$ $P0B_3/SI_0$ $P0A_0/SO_0$ $P0A_1/\overline{SCK_0}$ $P0A_2$/SCL $P0A_3$/SDA	P0B. P0A and serial interface input/outputs • $P0B_0$ to $P0B_3$ • 4-bit CMOS input/output port • Settable as input or output bit-wise • $P0A_0$ to $P0A_3$ • 4-bit input/output port • Settable as input or output bit-wise • SDA, SCL • SDA: Serial data input/output • SCL: Serial clock input/output • $\overline{SCK_0}$, SO_0, SI_0 • $\overline{SCK_0}$: Serial clock input/output • SO_0: Serial data output • SI_0: Serial data input • $\overline{SCK_1}$ SO_1, SI_1 • $\overline{SCK_1}$: Serial clock input/output • SO_1: Serial data output • SI_1: Serial data input	CMOS push-pull ($P0B_0$, $P0B_1/SO_1$, $P0B_2/\overline{SCK_1}$, $P0B_3$, $P0A_0/SO_0$, $P0A_1/\overline{SCK_0}$) N-ch open-drain $P0A_2$/SCL, $P0A_3$/SDA	Input ($P0B_0$ to $P0B_3$, $P0A_0$ to $P0A_3$)
61	GND_2	Ground	—	—
62 63	$P4A_2$/RAMOE $P4A_3$/RAMWE	Port 4A and external SRAM read/write signal outputs • $P4A_2$, $P4A_3$ • 2-bit CMOS output port • RAMOE, RAMWE • RAMOE: External SRAM read signal output • RAMWE: External SRAM write signal output	CMOS	Low-level output ($P4A_2$, $P4A_3$)
64	V_{DD3}	Positive power supply. Applies 5 V ±10 % in normal operating mode.	—	—
65 to 68	$P2B_3$ to $P2B_0$	4-bit CMOS input/output port Settable as input or output as a 4-bit unit	CMOS	Input
69 to 72	$P2C_3$ to $P2C_0$	4-bit CMOS input/output port Settable as input or output as a 4-bit unit	CMOS	Input
73 to 76	$P0D_3$ to $P0D_0$	4-bit input port	—	Input
77 to 80	$P0C_3$ to $P0C_0$	4-bit CMOS input/output port Settable as input or output as a 4-bit unit	CMOS	Input

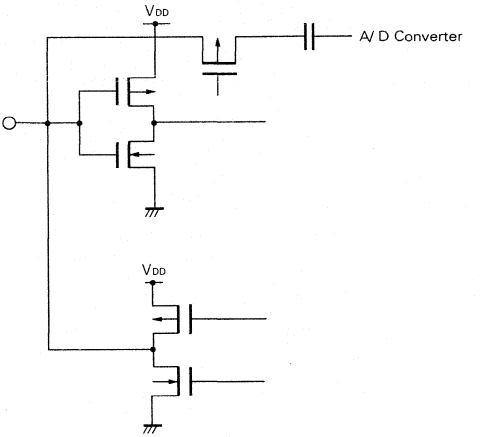
Note EO_{10} output can be controlled by the program.

1.2 PROM PROGRAMMING MODE

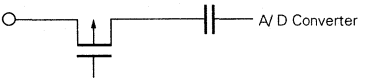
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET
14	V_{DD0}	Positive power supply. Applies 6 V in program memory write, read and verify operations.	—	—
17	GND_0	Ground	—	—
29	V_{PP}	Power supply for PROM programming. Applies 12.5 V as program voltage in program memory write, read and verify operations.	—	—
30	V_{DD1}	Positive power supply. Applies 6 V in program memory write, read and verify operations.	—	—
33	GND_1	Ground	—	—
35	CLK	PROM programming clock	—	—
45 to 52	D_0 to D_7	8-bit data input/output for PROM programming	CMOS push-pull	Input
61	GND_2	Ground	—	—
64	V_{DD2}	Positive power supply. Applies 6 V in program memory write, read and verify operations.	—	—
73 to 76	MD_3 to MD_0	Operating mode selection inputs for PROM programming	—	Input

1.3 PIN EQUIVALENT CIRCUITS

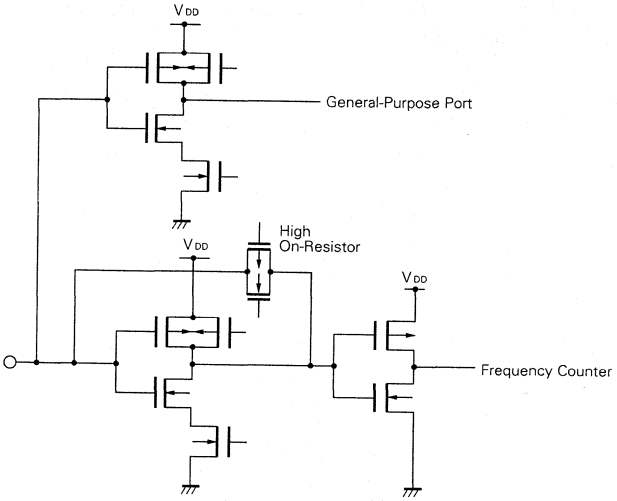
(1) P3B ($P3B_3/ADC_5$, $P3B_2/ADC_4$, $P3B_1/ADC_3$, $P3B_0/ADC_2$) (input/output)



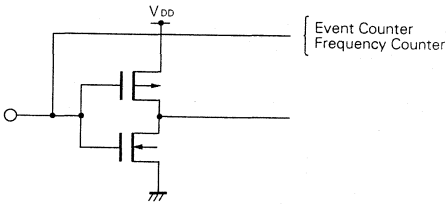
(2) ADC_1, ADC_0 (input)



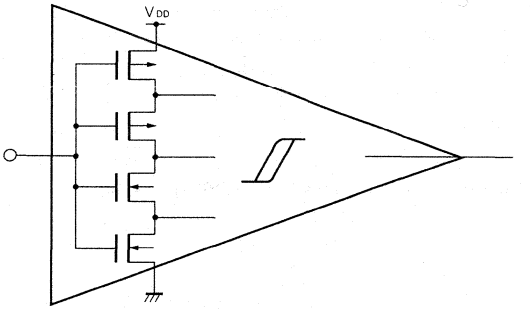
(3) P1D (P1D3/FMIFC, P1D2/AMIFC) (input)



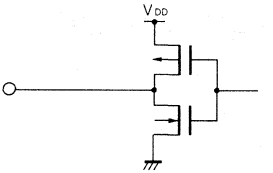
(4) P1D (P1D1/TM1IN, P1D0/FCG) (input)



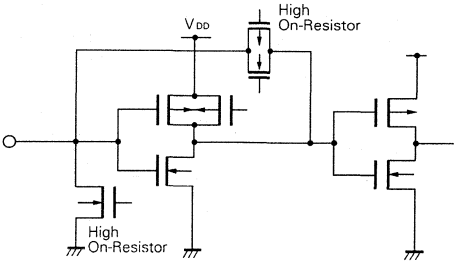
(5) CE, INT_1, INT_0 (hysteresis input)



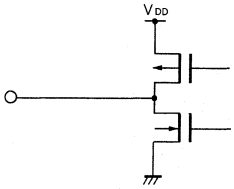
(6) P1C (P1C3, P1C2)
P3C (P3C3, P3C2, P3C1, P3C0)
P1B (P1B0/CGP)
P3D (P3D3/RAMA8)
P4A (P4A3/RAMWE, P4A2/ RAMOE) (output)



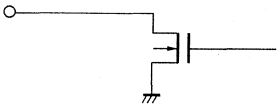
(7) VCOH, VCOL (input)



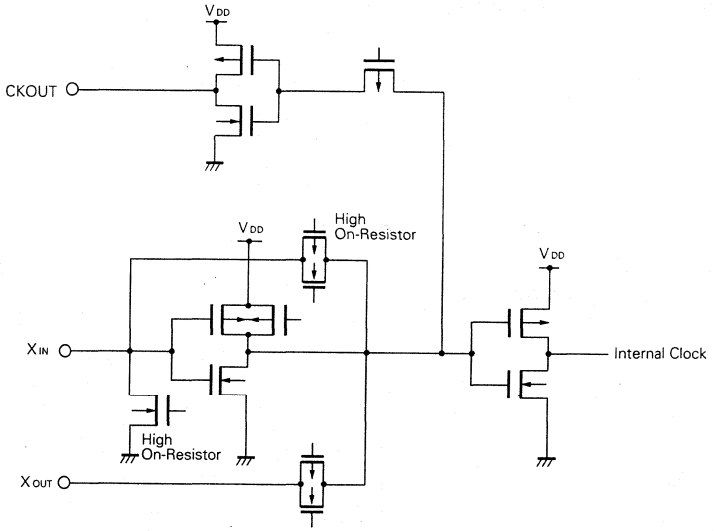
(8) EO_{10}, EO_{00}, EO_1 (output)



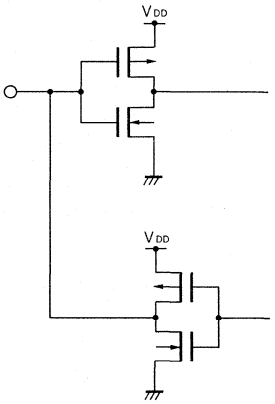
(9) P1B (P1B3/PWM2, P1B2/PWM1, P1B1/PWM0) (output)



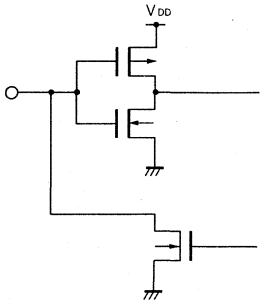
(10) X_{OUT} (output), X_{IN} (input), CKOUT (output)



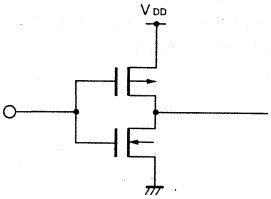
(11) P2D ($P2D_3$/$RAMA_7$, $P2D_2$/$RAMA_6$, $P2D_1$/$RAMA_5$, $P2D_0$/$RAMA_4$)
P3A ($P3A_3$/$RAMA_3$, $P3A_2$/$RAMA_2$, $P3A_1$/$RAMA_1$, $P3A_0$/$RAMA_0$)
P1A ($P1A_3$/$RAMD_7$, $P1A_2$/$RAMD_6$, $P1A_1$/$RAMD_5$, $P1A_0$/$RAMD_4$)
P2A ($P2A_3$/$RAMD_3$, $P2A_2$/ $RAMD_2$, $P2A_1$/$RAMD_1$, $P2A_0$/$RAMD_0$)
P0B ($P0B_3$/SI_0, $P0B_2$/$\overline{SCK}_1$, $P0B_1$/SO_1, $P0B_0$/SI_1)
P0A ($P0A_1$/$\overline{SCK}_0$, $P0A_0$/SO_0)
P2B ($P2B_3$, $P2B_2$, $P2B_1$, $P2B_0$)
P2C ($P2C_3$, $P2C_2$, $P2C_1$, $P2C_0$)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
} (input/output)



(12) P0A ($P0A_3$/SDA, $P0A_2$/SCL) (input/output)



(13) P0D (P0D3, P0D2, P0D1, P0D0) (input)



2. LIST OF μPD17P006 FUNCTIONS

Item		Function
PROM		12288 × 16 bits
	Table reference area	12288 × 16 bits
RAM		896 × 4 bits
	Data buffers	4 × 4 bits
	General registers	16 × 4 bits
System registers		12 × 4 bits
Register file		56 × 4 bits (control registers)
General-purpose port registers		17 × 4 bits
Instruction execution time		1.78 μs (using 4.5 MHz crystal resonator)
Stack levels		7 levels (stack manipulation capability)
General-purpose ports	Input/output port	40
	Input port	8
	Output	13
Clock generator port		1
Serial interface		• 2 systems, 3 channels Serial interface 0 (2-wire, 3-wire) Serial interface 1 (3-wire)
D/A converter		• 9 bits × 3 (PWM output, output withstand Voltage: 14 V MAX.) • Usable as modulo timer
A/D converter		• 8 bits × 6 (successive approximation by hardware and software)
Interrupts		• 8 channels (maskable interrupts) External interrupts : 2 channels (INT_0 pin, INT_1 pin) Internal interrupts : 4 channels (modulo timer × 3, serial interface 0) Dual-function interrupts: 2 channels D/A converter and serial interface 1, frequency counter and A/D converter and timer overflow)
Timer		• 4 systems 12-bit modulo (Remote control: 10/50 μs) 8-bit modulo (RDS clock cycle: 10/100 μs) 8-bit modulo (general-purpose: 10/100/500/1000 μs) Timer carry FF (100 ms)
Reset functions		• Power-on reset (when powered is turned on) • Reset via CE pin (CE pin: low → high) • Power failure detection function
PLL Frequency synthesizer	Frequency division method	• 2 methods Direct division method (VCOL pin 30 MHz MAX.) Pulse swallow method (VCOL pin 40 MHz MAX.) (VCOH pin 150 MHz MAX.)
	Reference frequency	• 12 frequencies selectable by program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50 100 kHz
	Charge pump	• 2 independent error out output systems (EO_{00}/EO_{01} system and EO_{10} system) • Output controllable by program (EO_{10} pin)
	Phase comparator	• Unlock detection possible by program Selectable unlock FF delay time

Item	Function
Frequency counter	• Frequency measurement P1D3/FMIFC pin 5 to 15 MHz P1D2/AMIFC pin 0.1 to 1 MHz • External gate width measurement P1D0/FCG pin
Supply voltage	• V_{DD} = 4.5 to 5.5 V (PLL and CPU operating) • V_{DD} = 3.5 to 5.5 V (PLL stopped, CPU operating) • V_{DD} = 2.2 to 5.5 V (Crystal oscillation stopped)
Package	80-pin plastic QFP (14 × 20 mm)

3. ONE-TIME PROM (PROGRAM MEMORY) WRITE, READ AND VERIFY OPERATIONS

The program memory incorporated in the μPD17P006 is 24576×8-bit electrically programmable one-time PROM. In normal operation, this PROM is accessed in a 16-bit word mode, but in program memory write, read and verify operations the memory is accessed in 8-bit word mode. In this case, the upper 8 bits of the 16-bit word are allocated to an even address, and the lower 8 bits to an odd address.

For PROM write, read, and verify operations, the PROM mode is set and the pins shown in Table 3-1 are used.

Address updating is performed by means of clock input from the CLK pin rather than by address input.

Table 3-1 Pins Used in Program Memory Write, Read and Verify Operations

Pin Name	Function
V_{PP}	Program voltage (12.5 V) application
CLK	Address update clock input
MD0 to MD3	Operating mode selection
D0 to D7	8-bit data input/output
V_{DD0} to V_{DD2}	Supply voltage (6 V) application

Writing to the on-chip PROM is performed using a PROM programmer and dedicated program adapter. The following types of PROM programmer and program adapter should be used:

PROM programmer	AF-9703	(Manufactured by Ando Electric Co., Ltd.)
	AF-9704	(Manufactured by Ando Electric Co., Ltd.)
Program adapter	AF-9808E	(Manufactured by Ando Electric Co., Ltd.)

3.1 PROGRAM MEMORY WRITE/READ/VERIFY OPERATING MODES

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD17P006 enters a program memory write/read/verify mode.

This mode is one of the operating modes shown in Table 3-2 according to the setting of pins MD0 to MD3.

Pins not used in the program memory write/read verify mode should be left open or connected to ground via a pull-down resistor (470 Ω) (see **"Pin Configuration (2) PROM Programming Mode"**).

Table 3-2 Program Memory Write/Read/Verify Operating Modes

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	X	H	H	Program inhibit mode

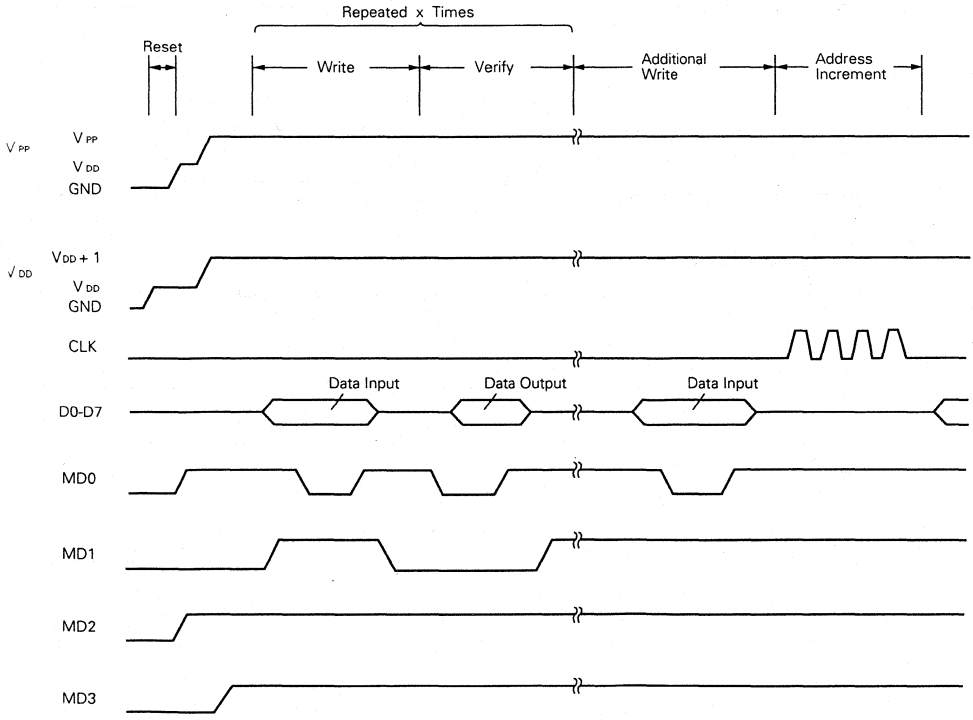
Remarks X: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The procedure for writing to program memory is as shown below, allowing high-speed writing

(1) Unused pins are connected to GND with a pull-down resistor. The CLK pin is driven low.
(2) 5 V is supplied to the V_{DD} pin. The V_{PP} pin is driven low.
(3) 5 V is supplied to the V_{PP} pin after a 10 μs wait.
(4) The mode setting pin is set to the program memory address zero-clear mode.
(5) 6 V is supplied to V_{DD} 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Data is written in 1 ms write mode.
(8) Program inhibit mode.
(9) Verify mode. If write is successful go to (10), otherwise repeat (7) through (9).
(10) (Number of times written in (7) to (9): X) × 1 ms additional writes.
(11) Program inhibit mode
(12) Program memory address is updated (+1) by inputting 4 pulses to the CLK pin.
(13) Steps (7) to (12) are repeated until the last address.
(14) Program memory address zero-clear mode.
(15) V_{DD}/ V_{PP} pin voltage is changed to 5 V.
(16) Power-off.

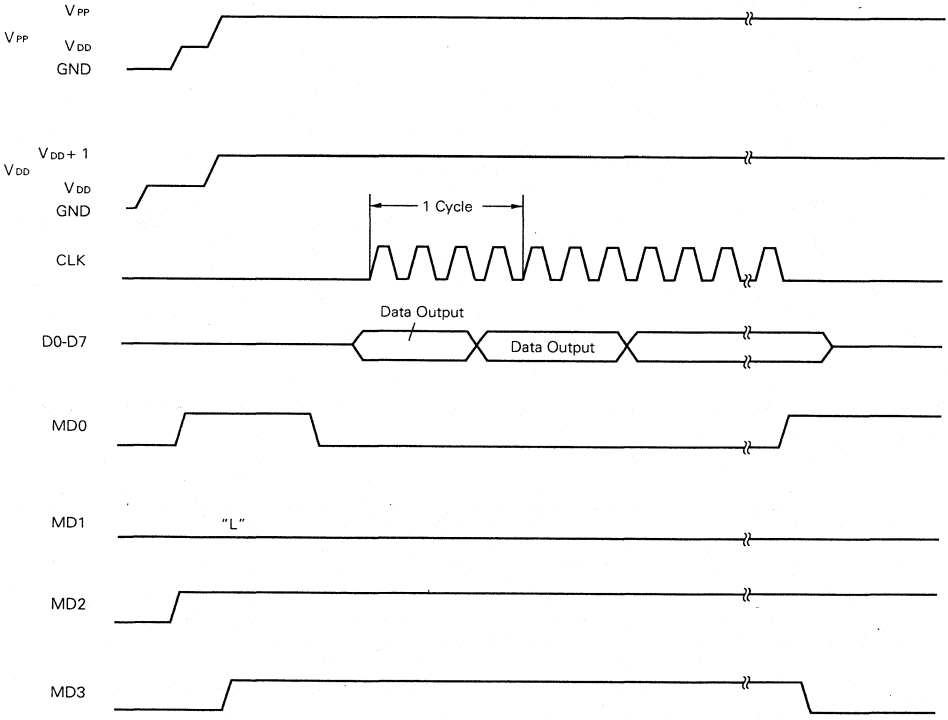
Steps (2) to (12) of the this procedure are shown in the following figure.



3.3 PROGRAM MEMORY READ PROCEDURE

(1) Unused pins are connected to GND with a pull-down resistor. The CLK pin is driven low.
(2) 5 V is supplied to the V_{DD} pin. The V_{PP} pin is driven low.
(3) 5 V is supplied to the V_{PP} pin after a 10 μs wait.
(4) The mode setting pin is set to the program memory address zero-clear mode.
(5) 6 V is supplied to V_{DD}, 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Verify mode. When clock pulses are input to the CLK pin, data is output sequentially, one address per 4-clock cycle.
(8) Program inhibit mode.
(9) Program memory address zero-clear mode.
(10) V_{DD}/ V_{PP} pin voltage is changed to 5 V.
(11) Power-off

Steps (2) to (9) of this Procedure are shown in the following figure.



4. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		−0.3 to +6.0	V
PROM Supply Voltage	V_{PP}		−0.3 to +13.5	V
Input Voltage	V_I		−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	Except $P0A_2$, $P0A_3$, $P1B_1$, to $P1B_3$	−0.3 to V_{DD} +0.3	V
Output Withstand Voltage	V_{BDS1}	$P1B_1$ to $P1B_3$	16.0	V
Output Withstand Voltage	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} +0.3	V
Output Current High	I_{OH}	1 pin	−10.0	mA
		Total, all output pins	−20.0	mA
Output Current Low	I_{OL}	1 pin	10.0	mA
		Total, all output pins	20.0	mA
Total Power Consumption	P_t		450	mW
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL operating
	V_{DD2}	3.5	5.0	5.5	V	CPU operating, PLL stopped
Data Retention Time	V_{DDR}	2.2		5.5	V	Crystal osillation stopped
Supply Voltage Rise Time	t_{RISE}			500	ms	V_{DD} = 0 → 4.5 V
Input Amplitude	V_{IN1}	0.5		V_{DD}	V_{p-p}	VC0H, VC0L
	V_{IN2}	0.5		V_{DD}	V_{p-p}	AMIFC, FMIFC
Output Withstand Voltage	V_{BDS}			14.0	V	$P1B_1$ to $P1B_3$
Operating Temperature	T_{opt}	−40		+85	°C	

DC Characteristics (Ta = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL operating
	V_{DD2}	3.5	5.0	5.5	V	CPU operating, PLL stopped
Supply Current	I_{DD1}		3.0	6.0	mA	CPU operating, PLL stopped X_{IN} pin sine wave input f_{IN} = 4.5 MHz, V_{IN} = V_{DD}, T_a = 25 °C
	I_{DD2}		2.5	5.0	mA	CPU operating, PLL stopped, HALT instruction used 20 instructions executed per ms X_{IN} pin sine wave input f_{IN} = 4.5 MHz, V_{IN} = V_{DD}, T_a = 25 °C
Data Retention Voltage	V_{DDR1}	3.5		5.5	V	Using power failure detection by timer FF - crystal oscillation
	V_{DDR2}	2.2		5.5	V	Using power failure detection by timer FF- crystal oscillation stopped
	V_{DDR3}	2.0		5.5	V	Data memory (RAM) retention
Data Retention Current	I_{DDR1}		2	3	μA	Crystal oscillation stopped V_{DD} = 5.0 V, T_a = 25 °C
	I_{DDR2}		2	7	μA	Crystal oscillation stopped T_a = 25 °C
Input Voltage High	V_{IH1}	0.8 V_{DD}		V_{DD}	V	**Note1**
Input Voltage Low	V_{IL1}	0		0.2 V_{DD}	V	**Note1**
Output Current High	I_{OH1}	−1.0	−5.0		mA	**Note2** V_{OH} = V_{DD} −1 V
	I_{OH2}	−1.0	−4.0		mA	EO_{10}, EO_{00}, EO_{01} V_{OH} = V_{DD} −1 V
Output Current Low	I_{OL1}	1.0	7.0		mA	**Note2** V_{OL} = 1 V
	I_{OL2}	1.0	3.5		mA	EO_{10}, EO_{00}, EO_{01} V_{OL} = 1 V
	I_{OL3}	1.0	2.0		mA	$P1B_1$ to $P1B_3$ V_{OL} = 1 V
	I_{OL4}	1.0	10.0		mA	$P0A_2$, $P0A_3$ V_{OL} = 1 V
Input Current High	I_{IH1}	0.1	0.8		mA	VCOH pulled low V_{IH} = V_{DD}
	I_{IH2}	0.1	0.8		mA	VCOL pulled low V_{IH} = V_{DD}
	I_{IH3}	0.1	1.3		mA	X_{IN} pulled low V_{IH} = V_{DD}
Output off Leak Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ V_{OH} = V_{DD}
	I_{L2}			500	nA	$P1B_1$ to $P1B_3$ V_{OH} = 14 V
	I_{L3}			±100	nA	EO_{10}, EO_{00}, EO_{01} V_{OH} = V_{DD}, V_{OL} = 0 V

Note1 $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$, $P1D_0$ to $P1D_3$, $P2A_0$ to $P2A_3$, $P2B_0$ to $P2B_3$, $P2C_0$ to $P2C_3$, $P2D_0$ to $P2D_3$, $P3A_0$ to $P3A_3$, $P3B_0$ to $P3B_3$, CE, INT_0, INT_1

2 $P0A_0$, $P0A_1$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_0$ to $P1A_3$, $P1B_0$, $P1C_2$, $P2A_0$, to $P2A_3$, $P2B_0$ to $P2B_3$, $P2C_0$ to $P2C_3$, $P2D_0$ to $P2D_3$, $P3A_0$ to $P3A_3$, $P3B_0$ to $P3B_3$, $P3C_0$ to $P3C_3$, $P3D_3$, $P4A_2$, $P4A_3$

AC CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{IN1}	0.5		30	MHz	VCOL MF mode sine-wave input V_{IN} = 0.3 V_{p-p}
	f_{IN2}	5		40	MHz	VCOL HF mode sine-wave input V_{IN} = 0.3 V_{p-p}
	f_{IN3}			150	MHz	VCOH sine-wave input V_{IN} = 0.3 V_{p-p}
	f_{IN4}	0.1		1	MHz	AMIFC sine-wave input V_{IN} = 0.5 V_{p-p}
	f_{IN5}	0.44		0.46	MHz	AMIFC sine-wave input V_{IN} = 0.05 V_{p-p}
	f_{IN6}	5		15	MHz	FMIFC sine-wave input V_{IN} = 0.5 V_{p-p}
	f_{IN7}	10.5		10.9	MHz	FMIFC sine-wave input V_{IN} = 0.06 V_{p-p}
A/D Conversion Resolution				6	bit	
A/D Conversion Total Error			±1.5		LSB	T_a = −10 to +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply Current	I_{DD3}		15		mA	CPU and PLL operating VCOH sine-wave input f_{IN} = 150 MHz, V_{IN} = 0.3 V_{p-p} V_{DD} = 5 V, T_a = 25 °C

DC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CLK
	V_{IH2}	V_{DD} −0.5		V_{DD}	V	CLK
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			1.0	V	I_{OL} = 1 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note1 Ensure that V_{PP} does not exceed +13.5 V including overshoot.

2 Ensure that V_{DD} is applied before V_{PP} and cut off after V_{PP}.

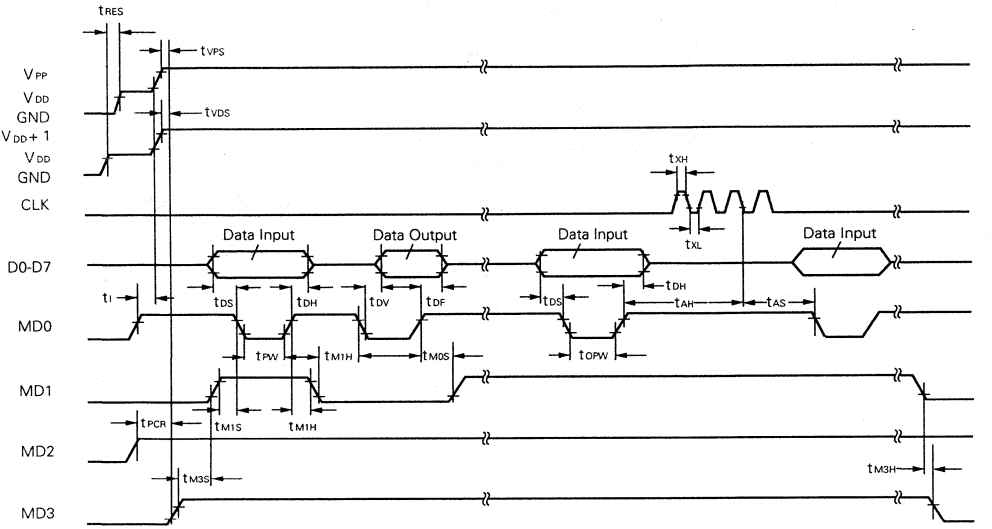
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V V_{pp} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	Note1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Set-Up Time[Note2] (to MD0↓)	t_{AS}	t_{AS}	2			μs	
MD1 Set-Up Timer (to MD0↓)	t_{M1S}	t_{OES}	2			μs	
Data Set-Up Time (to MD0↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time[Note2] (from MD0↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (from MD0↑)	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑	t_{DF}	t_{DF}	0		130	ns	
V_{pp} Set-Up Time (to MD3↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Set-Up Time (to MD3↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Set-Up Time (to MD1↑)	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (from MD0↑)	T_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recovery Time (from MD0↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	—	10			μs	
CLK Input High-/Low-Level Width	t_{XH}, t_{XL}	—	0.125			μs	
CLK Input Frequency	f_X	—			4.19	MHz	
Initial Mode Setting Time	t_I	—	2				
MD3 Set-Up Time (to MD1↑)	t_{M3S}	—	2			μs	
MD3 Hold Time (from MD1↓)	t_{M3H}	—	2			μs	
MD3 Set-Up Time (to MD0↓)	t_{M3SR}	—	2			μs	For program memory read
Data Output Delay Time from Address[Note2]	t_{DAD}	t_{ACC}	2			μs	For program memory read
Data Output Hold Time from Address[Note2]	t_{HAD}	t_{OH}	0		130	ns	For program memory read
MD3 Hold Time (from MD0↑)	t_{M3HR}	—	2			μs	For program memory read
Data Output Float Delay Time from MD3↓	t_{DFR}	—	2			μs	For program memory read
Read Set-up Time	t_{RES}		10			μs	

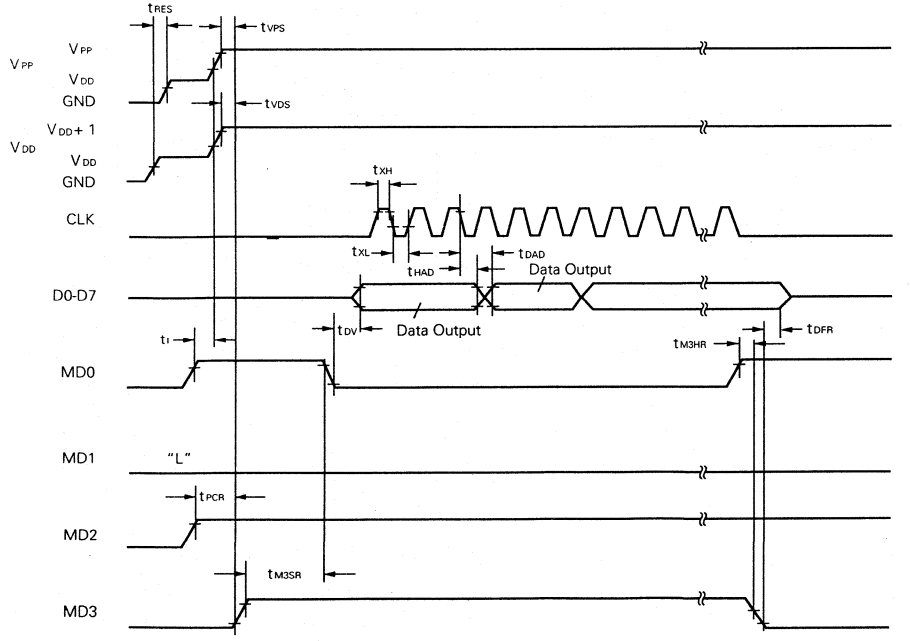
Note1 Corresponding μPD27C256 symbol.

2 Internal address incrementing (+1) is performed on the 3rd fall of CLK with 4 clock pulses (CLK) as one cycle.
Internal addresses are not connected to pins.

Program Memory Write Timing

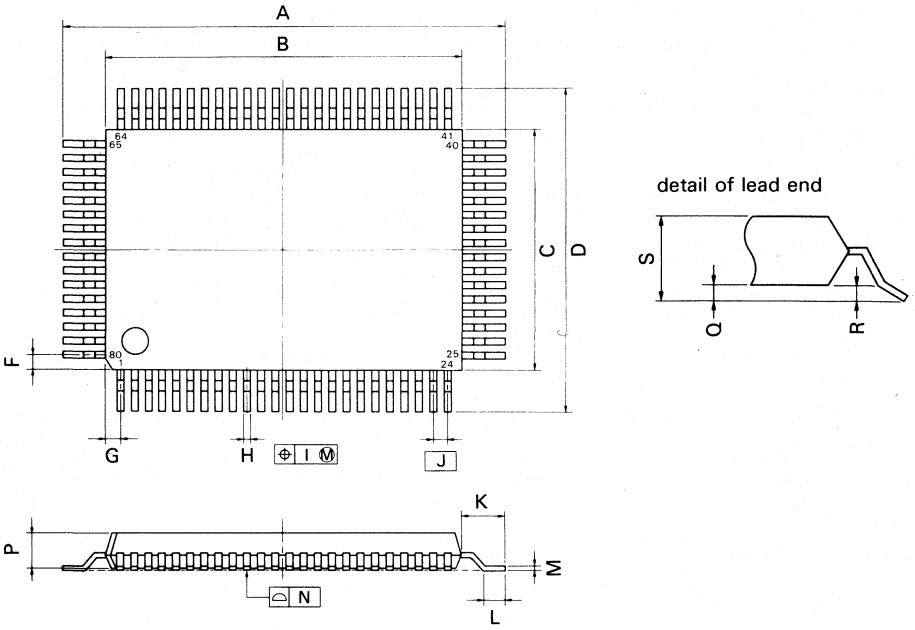


Program Memory Read Timing



5. PACKAGE DIMENSION

80 PIN PLASTIC QFP (14×20)



S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{+0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{+0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{+0.4}$	$0.677^{+0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{+0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{+0.2}$	$0.063^{+0.008}$
L	$0.8^{+0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{+0.1}$	$0.004^{+0.004}$
R	$0.1^{+0.1}$	$0.004^{+0.004}$
S	3.0 MAX.	0.119 MAX.

DIGITAL TUNING SYSTEM HARDWARE BUILT-IN 4-BIT SINGLE CHIP MICRO CONTROLLER

μPD17010 is a 4-bit single chip CMOS micro controller which contains digital tuning system hardware.

17K architecture is used for CPU, data and memory manipulations and various types of operations, and peripheral hardware control can be performed directly by one instruction.

Peripheral hardware devices include a prescaler which operates up to 250 MHz, PLL frequency synthesizer, LPF (Low Pass Filter) amplifier, and frequency counter for digital tuning in addition to various types of input/output ports, LCD controller/driver, 12 bit modulo timer, A/D converter, D/A converter (PWM output), and clock generator ports.

Consequently, a high performance digital system with a variety of functions can be constructed using only one chip. One-time PROM version μPD17P010 is available as μPD17010 and μPD17P010 can be used for program evaluation and small lot production of μPD17010.

FEATURES

- Using 17K architecture
- Program memory (ROM)
  7932 × 16 bits
- General purpose data memory (RAM)
  432 × 4 bits
- Instruction execution time
  4.44 μs (using 4.5 MHz quarts oscillator)
- Decimal operation enabled
- Table reference enabled
- Built-in PLL frequency synthesizer hardware
  Dual modules prescaler (150 MHz Max.), programmable divider, phase comparator, charge pump, and LPF amplifier
- Various types of peripheral hardware
  General purpose input/output ports, LCD controller/driver, serial interface, 12 bit modulo timer, A/D converter, D/A converter (PWM output), clock generator port and frequency counter.
- Various types of interrupt
  External interrupt: 2 channels
  Internal interrupt : 4 channels
- Power On Reset, resetting by a CE pin, and built-in blackout detection circuit
- CMOS low power consumption
- Power supply voltage 5 V ± 10 %

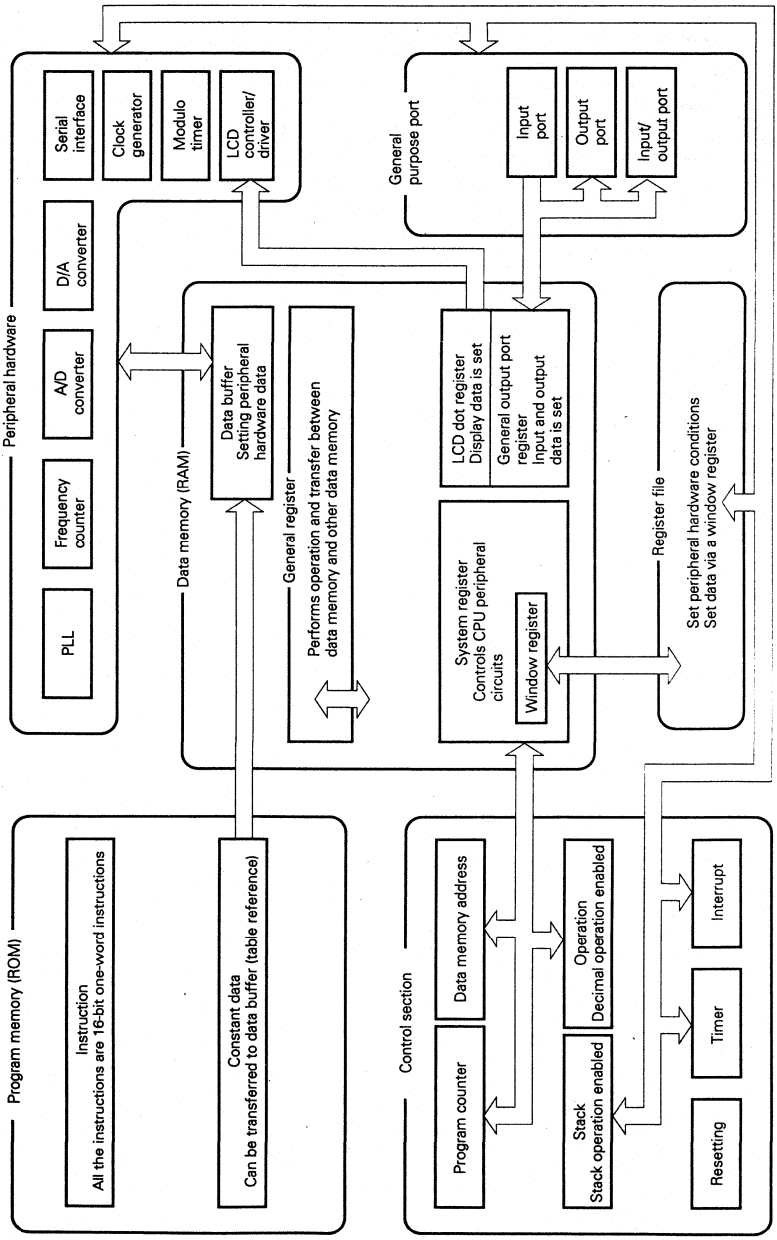
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17010GF-×××-3B9	80-pin plastic QFP (14 × 20)	Standard

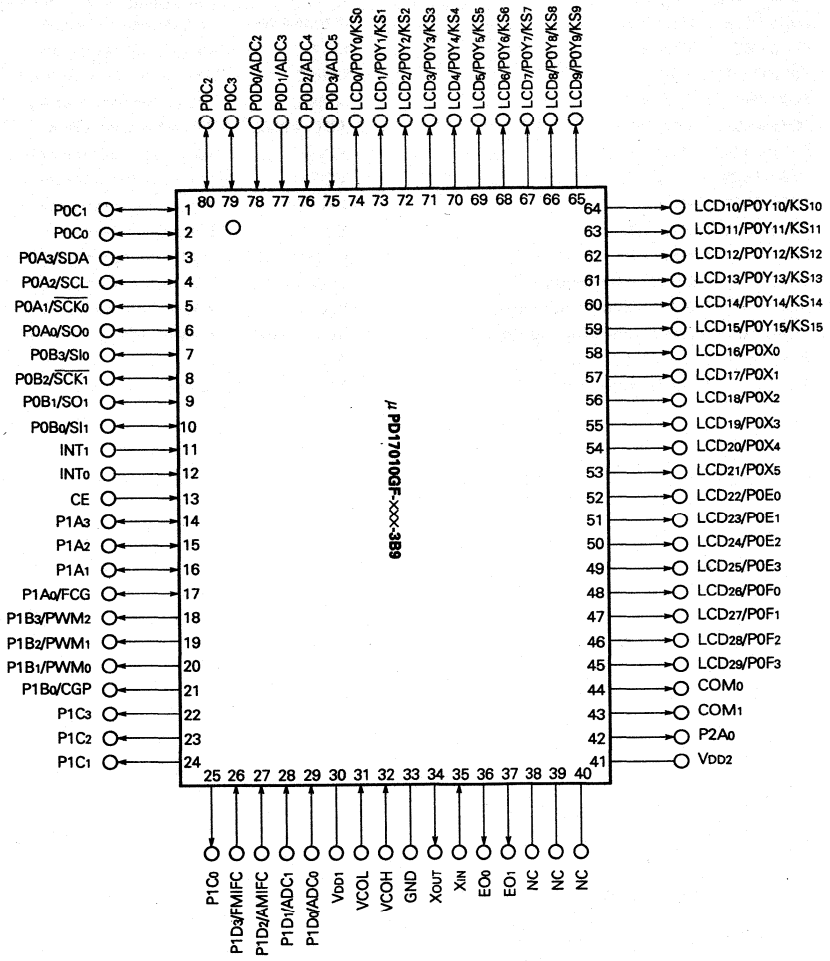
Item	Function
Program memory (ROM)	• 7932 × 16 bits The entire internal ROM area can be table referenced.
General data memory (RAM)	• 432 × 4 bits Data buffer : 4 × 4 bits General register : 16 × 4 bits
System register	• 12 × 4 bits
Register file	• 41 × 4 bits (control register)
General port register (including LCD dot data register)	• 24 × 4 bits
Instruction execution time	• 4.44 μs (using 4.5 MHz quarts oscillator)
Stack level	• 9 levels (stack operation enabled)
General purpose port	• Input/output port : 16 • Input ports : 8 • Output ports : 9 (+30: LCD segment pin)
Clock generator port (CGP)	• 1 VDP (Variable Duty Pulse) and SG (Signal Generator) functions
LCD controller/driver	• 30 segments, 2 common 1/2 duty, 1/2 bias, frame frequency 250 Hz, driving voltage V_{DD}, segment pin used also for key source: 16 ports All of the 30 ports can be used as output ports. (4 ports, 4 ports, 6 ports, and 16 ports can be set independently)
Serial interface	• Two types (3 channels) Serial interface 0 (2-wire system, 3-wire system) Serial interface 1 (3-wire system)
D/A converter	• 8 bits × 3 (PWM output and output resisting pressure 16 V Max.)
A/D converter	• 6 bits × 6 (consecutive comparison method by software)
Interrupt	• 6 channels (maskable interrupt) External interrupt : 2 channels (INT_0 pin and INT_1 pin) However, INT_1 can perform interrupts and switching when timer overflow occurs. Internal interrupt : 4 channels (timer 2, serial interface 0, and frequency counter)
Timer	• Three types 12-bit modulo timer Basic timer carry FF (1, 5, 100, 250 ms) Basic timer interrupt (1, 5, 100, 250 ms)
Reset	• Power On Reset (at power supply connection) • Resetting by CE pin (CE pin Low → High) • Blackout detection function

Item		Function
PLL frequency synthesizer	Division method	• 2 types Direct division method (VCOL pin 20 MHz Max.) Pulse swallow method (VCOL pin 40 MHz Max.) (VCOH pin 150 MHz Max.)
	Reference frequency	• 12 types are selected by the program 1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50, 100 kHz
	Charge pump	• Two independent error output
	Phase comparator	• Unlocking can be detected by a program Unlocking FF delay time can be selected
	LPF amplifier	• CMOS operation amplifier output resisting pressure 16 V Max.
Frequency counter		• Frequency test $P1D_3$/FMIFC pin 5-15 MHz $P1D_2$/AMIFC pin 0.1-1 MHz • External gate width test $P1A_0$/FCG pin
Power supply voltage		5 V ±10 %
Package		80-pin plastic QFP (14 × 20 mm)

CONCEPT OF μPD17010



PIN CONFIGURATION (Top View)



P0A0-P0A3 : Port 0A
P0B0-P0B3 : Port 0B
P0C0-P0C3 : Port 0C
P0D0-P0D3 : Port 0D
P0E0-P0E3 : Port 0E
P0F0-P0F3 : Port 0F
P0X0-P0X5 : Port 0X
P0Y0-P0Y15 : Port 0Y
P1A0-P1A3 : Port 1A
P1B0-P1B3 : Port 1B
P1C0-P1C3 : Port 1C
P1D0-P1D3 : Port 1D
P2A0 : Port 2A
SDA : Serial data input/output
SCL : Serial clock input/output
$\overline{SCK_0}$ $\overline{SCK_1}$: Serial clock input/output
SO0, SO1 : Serial data output
SI0, SI1 : Serial data input

INT0, INT1 : External interrupt input
CE : Chip enable input
FCG : External gate counter input
PWM0-PWM2 : D/A converter output
CGP : Clock generator port
FMIFC : Frequency counter input
AMIFC : Frequency counter input
ADC0-ADC5 : A/D converter input
VCOL : Local oscillation low input
VCOH : Local oscillation high input
XIN, XOUT : Quarts resonator connector pins
EO0, EO1 : Error out output
COM0, COM1 : LCD common signal output
LCD0-LCD29 : LCD segment signal output
KS0-KS15 : Key source signal output
VDD1, VDD2 : Power supply
GND : Ground
NC : No connection

1. PIN FUNCTIONS

1.1 EXPLANATION ON EACH PIN FUNCTION

PIN NO.	SYMBOL	FUNCTIONS	OUTPUT TYPE	POWER ON RESET
79 80 1 2	$P0C_3$ $P0C_2$ $P0C_1$ $P0C_0$	4-bit input/output port. Can be specified as an input/output port in 4-bit units	CMOS Push-Pull	Input
3 4 5 6 7 8 9 10	$P0A_3$/SDA* $P0A_2$/SCL* $P0A_1/\overline{SCK_0}$ $P0A_0/SO_0$ $P0B_3/SI_0$ $P0B_2/\overline{SCK_1}$ $P0B_1/SO_1$ $P0B_0/SI_1$	Port 0A, port 0B and serial interface input/output • $P0A_3$-$P0A_0$ · 4-bit input/output port · Can be specified as an input/output port in 1-bit units. • $P0B_3$-$P0B_0$ · 4-bit CMOS input/output port · Can be specified as an input/output port in 1-bit units. • SDA, SCL · SDA : Serial data input/output · SCL : Serial clock input/output • $\overline{SCK_0}$, SO_0, SI_0 · $\overline{SCK_0}$: Serial clock input/output · SO_0 : Serial data output · SI_0 : Serial data input (SDA and SCL cannot be used simultaneously with $\overline{SCK_0}$, SI_0 and SO_0) • $\overline{SCK_1}$, SO_1, SI_1 outputs · $\overline{SCK_1}$: Serial clock input/output · SO_1 : Serial data output · SI_1 : Serial data input SDA, SCL, $\overline{SCK_0}$, SI_0, $\overline{SCK_1}$ and SI_1 are Schmitt trigger inputs with hysteresis characteristics.	N-ch open drain 5 V resisting pressure ($P0A_3$/SDA, $S0A_2$/SCL) CMOS Push-Pull ($P0A_1/\overline{SCK_0}$, $P0A_0/SO_0$, $P0B_3$, $P0B_2/\overline{SCK_1}$, $P0B_1/SO_1$, $P0B_0$)	Input ($P0A_3$-$P0A_0$, $P0B_3$-$P0B_0$)
11 12	$\overline{INT_1}$ INT_0	Edge detector interrupt input. It can be set to falling edge or rising edge detection. This pin is a Schmitt trigger input with hysteresis characteristics.	–	Input

* Since pins $P0A_3$/SDA, $P0A_2$/SCL are N-ch open drain outputs, an external pull-up resistor is required.

PIN NO.	SYMBOL	FUNCTIONS	OUTPUT TYPE	POWER ON RESET
13	CE	The operation selection and reset signal inputs of the μPD17010 is described below. (1) Device operation selection The PLL frequency synthesizer section can be operated when the CE pin is high. When the CE pin is low, the PLL frequency synthesizer section is automatically set to a disabled state (operation disabled) in the device internal section. (2) Reset signal input When the CE pin goes from low to high, the device is reset by synchronizing with the timer carry FF of the internal section (CE Reset). This pin does not accept a low or high level of less than 110-165 μs to prevent operation errors due to noise. The CEJDG register (address 07H) of the register file makes it possible to detect the input signal level of the pin. Also at this time, the content of the CEJDG register does not change at a low or high level of less than 110-165 μs. This pin is a Schmitt trigger input with hysteresis characteristics. Note that a voltage higher than that of the V_{DD} pin must not be supplied at power connection. These pins are inputs/outputs for port 1A and inputs for the external gate counter.	–	Input
14 I 16 17	$P1A_3$ I $P1A_1$ $P1A_0$/FCG	These pins are input/output for port 1A and input for the external gate counter. • $P1A_3$-$P1A_0$ · 4-bit CMOS input/output port · Can be specified as an input/output port in 1-bit units. • FCG · External gate counter input	CMOS Push-Pull ($P1A_3$-$P1A_0$)	Input ($P1A_3$-$P1A_0$)
18 19 20 21	$P1B_3$/PWM_2* $P1B_2$/PWM_1* $P1B_1$/PWM_0 $P1B_0$/CGP	These pins are outputs for port 1B, D/A converter and the clock generator port. • $P1B_3$-$P1B_0$ · 4-bit output ports • PWM_2-PWM_0 · 8-bit resolution D/A converter output • CGP · Clock generator port output	N-ch open drain 16 V resisting pressure ($P1B_3$/PWM_2 to $P1B_1$/PWM_0) CMOS Push-Pull ($P1B_0$/CGP)	Outputs undefined data ($P1B_3$-$P1B_0$)
22 I 25	$P1C_3$ I $P1C_0$	4-bit CMOS output ports	CMOS Push-Pull	Outputs undefined data

* Since pins $P1B_3$/PWM_2-$P1B_1$/PWM_0 are N-ch open drain outputs, an external pull-up resistor is required.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>FUNCTIONS</th><th>OUTPUT TYPE</th><th>POWER ON RESET</th></tr>
<tr><td>26
27
28
29</td><td>P1D3/FMIFC
P1D2/AMIFC
P1D1/ADC1
P1D0/ADC0</td><td>These pins are port ID, frequency counter and A/D converter inputs.
• P1D3-P1D0
· 4-bit input ports
• FMIFC, AMIFC
· Frequency counter inputs
The following frequencies can be tested.
<table><tr><th>Input pin</th><th>Input frequency (MHz)</th><th>Input oscillation (V_{P-P})</th></tr><tr><td rowspan="2">P1D3/FMIFC</td><td>5 - 15</td><td>0.3</td></tr><tr><td>10.5 - 10.9</td><td>0.06</td></tr><tr><td rowspan="2">P1D2/AMIFC</td><td>0.1 - 1</td><td>0.3</td></tr><tr><td>0.44 - 0.46</td><td>0.05</td></tr></table>Since an AC amplifier is used for the input of these pins, the DC components in the input signal must be removed with a capacitor.
• ADC1, ADC0
· Analog input a 6-bit resolution A/D converter</td><td>–</td><td>Input
(P1D3-P1D0)</td></tr>
<tr><td>30
41</td><td>VDD1
VDD2</td><td>These are device power supply pins. A 5 V ± 10 % voltage is supplied to the CPU or peripheral devices when they are in operation. During a clock stop a voltage of 2.2 V will maintain data. When VDD starts operating, the μPD17010 is reset by the internal power-on reset circuit. All pins other than the VDD pins (VDD1 and VDD2) must not be supplied with voltages that exceed that of the VDD pin. Special care must be taken when the VDD and CE pins are started simultaneously as a latch-up could occur.
The VDD1 and the VDD2 pins must be connected to the same electric potential.
The VDD2 pin is used to supply power to the quartz oscillation circuit (pins XIN and XOUT), error-out circuits (pins EO0 and EO1). The VDD1 pin provides the other sections with power.</td><td>–</td><td>–</td></tr>
</table>

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>FUNCTIONS</th><th>OUTPUT TYPE</th><th>POWER ON RESET</th></tr>
<tr><td>31
32</td><td>VCOL
VCOH</td><td>These pins are used for inputting the local oscillation frequency of PLL. Two methods are available: a direct division method (MF mode) and a pulse swallow method (HF and VHF modes).

<table><tr><th>Division method</th><th>Input pin</th><th>Input frequency (MHz)</th><th>Input voltage (V_{p-p})</th></tr><tr><td>Direct division (MF)</td><td>VCOL</td><td>0.5 - 30</td><td>0.3</td></tr><tr><td>Pulse swallow (HF)</td><td>VCOL</td><td>5 - 40</td><td>0.3</td></tr><tr><td>Pulse swallow (VHF)</td><td>VCOH</td><td>9 - 150</td><td>0.3</td></tr></table>
Since an AC amplifier is used for the input of these pins, the DC components in the input signal must be removed with a capacitor.</td><td>–</td><td>Input</td></tr>
<tr><td>33</td><td>GND</td><td>Ground pin of the device</td><td>–</td><td>–</td></tr>
<tr><td>34
35</td><td>X_{OUT}*
X_{IN}*</td><td>Quartz oscillator connection pin.
A 4.5 MHz quartzcrystal is connected.</td><td>CMOS Push-Pull
–</td><td>–</td></tr>
<tr><td>36
37</td><td>EO_0
EO_1</td><td>These are charge pump output pins of a PLL frequency synthesizer.
When the frequency produced by dividing the local oscillation (VCO) frequency input to the VCOL pin (pin number 31) or the VCOH (pin number 32) is higher than the reference frequency, the output at pins EO_0 and EO_1 is high. When the produced frequency is lower than the reference frequency, the output at these pins is low and when the produced frequency is equal to the reference frequency, floating occurs. Either of the EO_0 or the EO_1 pins can be used since they output the same type of signal.</td><td>CMOS 3-state</td><td>High impedance</td></tr>
<tr><td>38
I
40</td><td>NC</td><td>A non connection</td><td>–</td><td>–</td></tr>
<tr><td>42</td><td>$P2A_0$</td><td>A 1-bit CMOS output port</td><td>CMOS Push-Pull</td><td>Undefined data output</td></tr>
<tr><td>43
44</td><td>COM_1
COM_0</td><td>These pins output the common signal of the LCD controller/driver.
The output from these pins is low during the display-off mode, a power on reset or the execution of clock stop instruction.</td><td>CMOS 3-volume output</td><td>Low output</td></tr>
</table>

* Refer to **APPENDIX A CAUTIONS TO BE TAKEN WHEN CONNECTING THE QUARTZ OSCILLATOR.**

PIN NO.	SYMBOL	FUNCTIONS	OUTPUT TYPE	POWER ON RESET
45 I 48 49 I 52 53 I 58 59 I 74	$LCD_{29}/P0F_3$ I $LCD_{26}/P0F_0$ $LCD_{25}/P0E_3$ I $LCD_{22}/P0E_0$ $LCD_{21}/P0X_5$ I $LCD_{16}/P0X_0$ $LCD_{15}/P0Y_{15}/KS_{15}$ I $LCD_0/P0Y_0/KS_0$	These pins are used for outputting the segment signals of ports 0F, 0E, 0X and 0Y and LCD controller/driver as well as source signals of the key matrix. • $P0F_3$-$P0F_0$ · 4-bit CMOS output port • $P0E_3$-$P0E_0$ · 4-bit CMOS output port • $P0X_5$-$P0X_0$ · 6-bit CMOS output port • $P0Y_{15}$-$P0Y_0$ · 16-bit CMOS output port • LCD_{29}-LCD_0 · Segment signal output of the LCD controller/driver • KS_{15}-KS_0 · Key source signals of the key matrix	CMOS Push-Pull	Low output (LCD_{29}-LCD_0)
75 I 78	$P0D_3$-ADC_5 I $P0D_0/ADC_2$	Analog input to port 0D and A/D converter and key source signal return input for LCD segments. • $P0D_3$-$P0D_0$ · 4-bit input port · The internal pull-down resistor must be on at all times. • ADC_5-ADC_2 · Analog input to 6-bit resolution A/D converter · The internal pull-down resistor must be off. • Return input of key source signal · When an LCD segment pin is used in the key source, the internal pull-down resistor must be on only during key source output (220 μs) and off during LCD segment signal output.	–	Input with pull-down resistor ($P0D_3$-$P0D_0$)

1.2 NOTES ON USING A GENERAL PURPOSE PORT

1.2.1 Port Register Data Set

The port registers (registers P0A to P2A) on data memory are used for reading input data or setting output data of each of the ports, Port 0A, Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A.

In this case, the $P0A_3$ pin of Port 0A corresponds to the highest bit of port register P0A and the $P0A_0$ pin corresponds to the lowest bit.

These apply also to Port 0B, Port 0C, Port 0D, Port 1A, Port 1B, Port 1C, Port 1D, and Port 2A. Output data of Port 0E, Port 0F, Port 0X, and Port 0Y is set by the LCD group register via the LCD dot register or a data buffer on the data memory.

1.2.2 Input/output Ports (Port 0A, Port 0B, Port 0C, and Port 1A)

(1) When each port is specified as an input port

By executing an instruction (the address of the port register is specified for m of SKT m, #i, or ADD r, m) for reading the contents of each port register in the data memory, the status of each port pin is used as the value of the port register.

When an instruction (specified for r of MOV m, #i or ADD r, m) for writing data to each port register is executed, the value is written to the output data latch circuit.

(2) When each port is specified as an output port

When an instruction for writing data to each port register is executed, the value is written to the output data latch circuit and is output from each pin.

When an instruction for reading the contents of each port register is executed, the contents of output data latch are used as the value of the port register. However, for pins $P0A_3$/SDA and $P0A_2$/SCL, the pin status is read as it is when the contents of the port register are read and the status may be different from the output data.

At Power On Reset, CE Reset, or execution of a Clock Stop instruction, all of these pins are set for input ports.

Since the contents of the output data latch circuit are undefined at Power On Reset, a Write instruction must be executed for the port register before setting data to the output port. Otherwise, undefined data is output. At CE Reset or execution of a Clock Stop instruction, the contents of the output data latch circuit do not change.

1.2.3 Output Ports (Port 1B, Port 1C, Port 0F, Port 0E, Port 0X, and Port 0Y)

An output port is used for writing the value of the port register to the output data latch circuit by executing an instruction for writing data in a port register and outputting data from each pin.

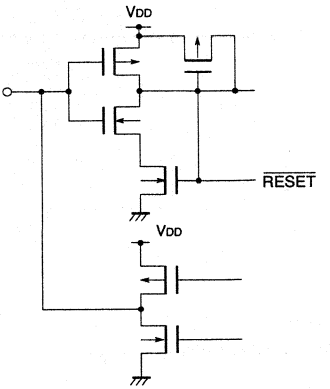
When a Read instruction is executed for a port register value, the port register value is set as the status of the output data latch circuit.

At Power On Reset, undefined data is output.

At CE Reset, the previous output data is kept at execution of a Clock Stop instruction. However, Port 0E, Port 0F, Port 0X, and Port 0Y output a Low level automatically at Power On Reset and at execution of a Clock Stop instruction.

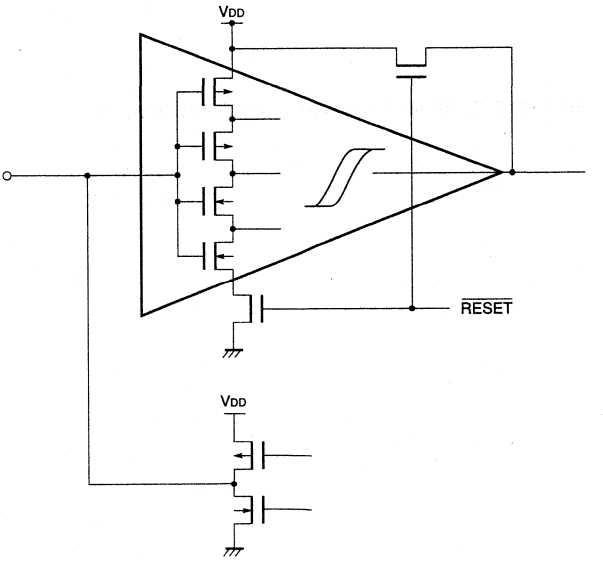
1.3 PIN EQUIVALENT CIRCUITS

(1) P0A ($P0A_0/SO_0$)
P0B ($P0B_1/SO_1$)
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$) *1
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
} (Input/output)

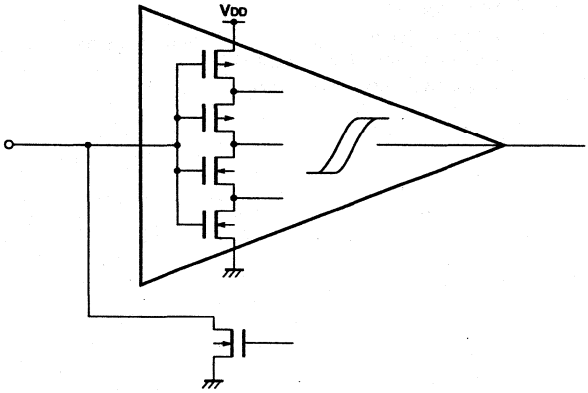


*1 The $\overline{RESET}$ signal is not provided to P0C.

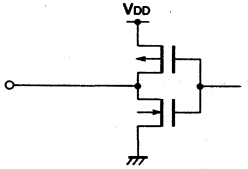
(2) P0A ($P0A_1/\overline{SCK_0}$)
P0B ($P0B_3/SI_0$, $P0B_2/\overline{SCK_1}$, $P0B_0/SI_1$)
} (Hysteresis input or output)



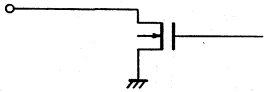
(3) P0A (P0A3/SDA, P0A2/SCL) (Hysteresis input or output)



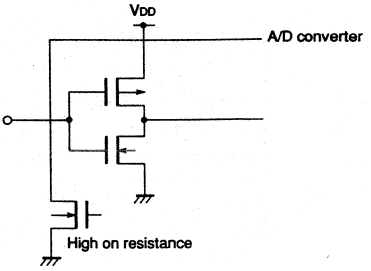
(4) P1B (P1B0/CGP)
P1C (P1C3, P1C2, P1C1, P1C0)
P2A (P2A0)
LCD0/P0Y0/KS0-LCD29/P0F3 } **(Output)**



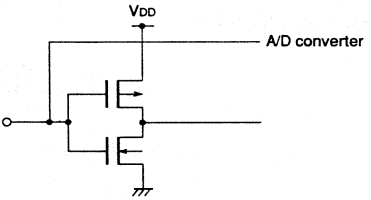
(5) P1B (P1B3/PWM2, P1B2/PWM1, P1B1/PWM0) (Output)



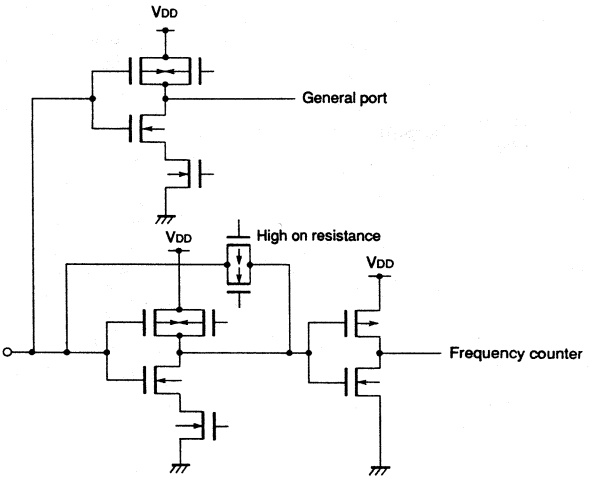
(6) P0D (P0D3/ADC5, P0D2/ADC4, P0D1/ADC3, P0D0/ADC2) (Input)



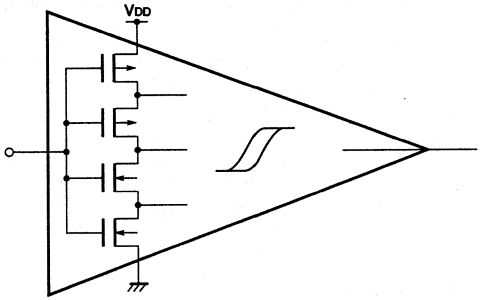
(7) P1D (P1D1/ADC1, P1D0/ADC0) (Input)



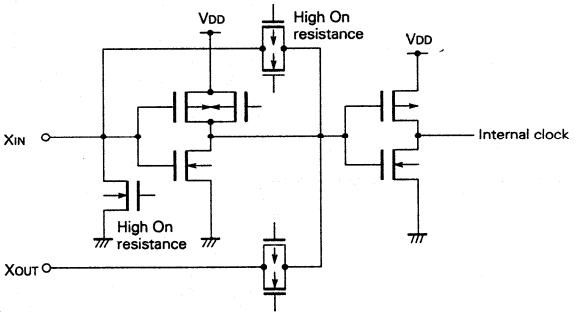
(8) P1D (P1D3/FMIFC, P1D2/AMIFC) (Input)



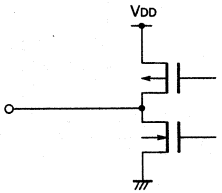
(9) CE, INT1, INT0 } **(Schmitt trigger input)**



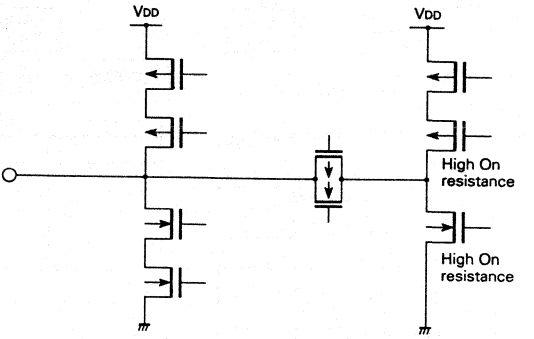
(10) XOUT (Output) and XIN (Input)



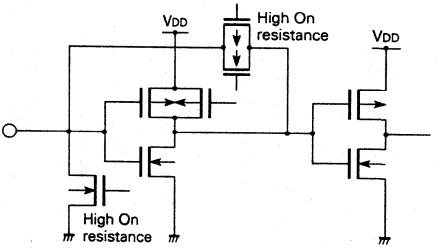
(11) EO1, EO0 } **(Output)**



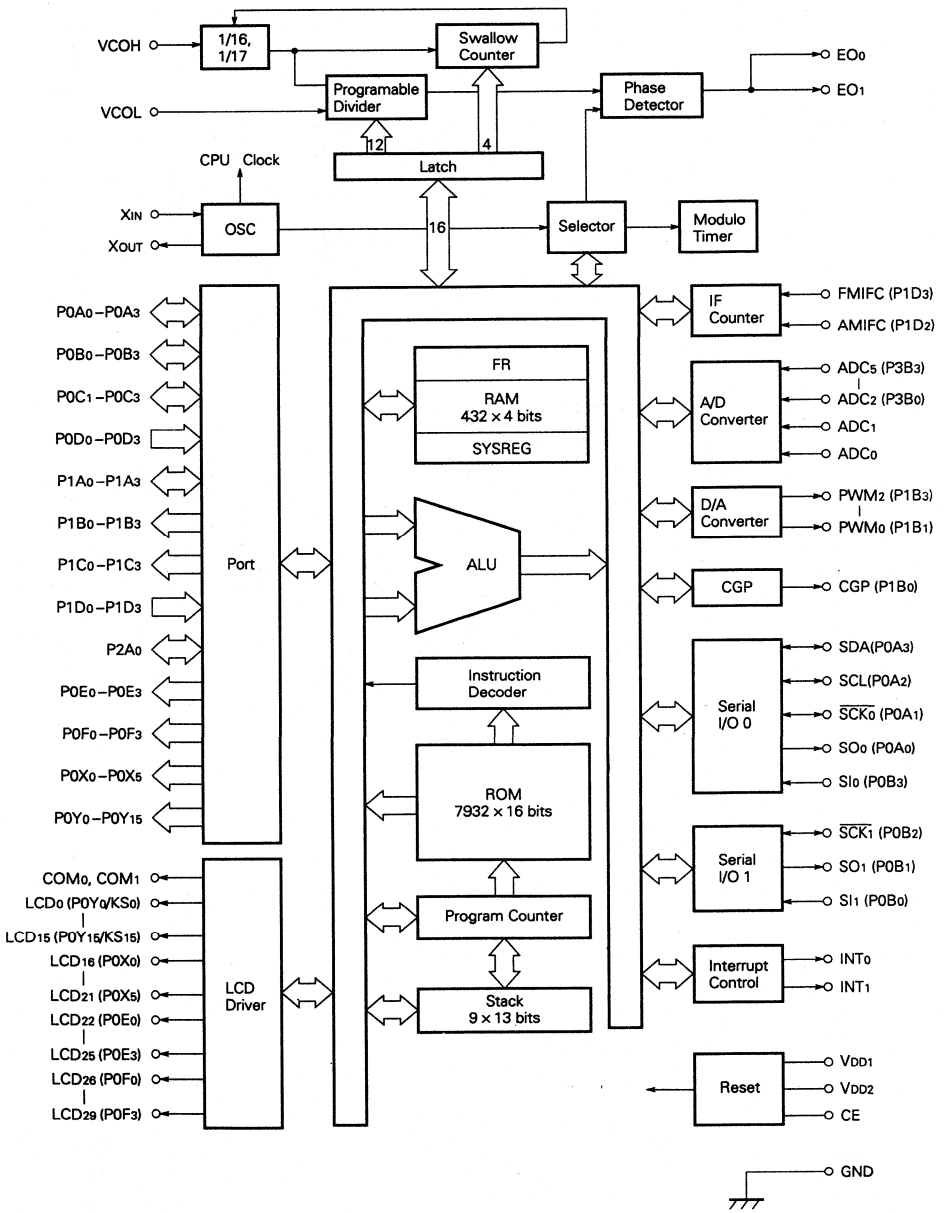
(12) COM1
COM0
} (Output)



(13) VCOH
VCOL
} (Input)



2. BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T_a = 25 ±2 °C)

Source Voltage	V_{DD}		−0.3 - +6.0	V
Input Voltage	V_I		−0.3 - V_{DD} + 0.3	V
Output Voltage	V_O	$P1B_1$ - $P1B_3$, $P0A_2$, $P0A_3$	−0.3 - V_{DD} + 0.3	V
Output Withstand Voltage	V_{BDS1}	$P1B_1$ - $P1B_3$	18.0	V
	V_{BDS2}	$P0A_2$, $P0A_3$	V_{DD} + 0.3	V
High Level Output Current	I_{OH}	1 pin	−12	mA
		$P2A_0$, LCD_0 - LCD_{29} pins combined	−25	mA
		All pins other than the above	−40	mA
Low Level Output Current	I_{OL}	Any of $P0A_0$ - $P0A_3$, $P1A_1$ - $P1A_3$, $P2A_0$	15	mA
		Any pin other than the above	10	mA
		$P0A_0$ - $P0A_3$, $P1A_1$ - $P1A_3$, $P2A_0$ pins combined	50	mA
		All pins other than the above	20	mA
Total Loss **Note**	Pt		450	mW
Operating Temperature	T_{opt}		−40 - +85	°C
Storage Temperature	T_{stg}		−55 - +125	°C

Note See next section, "Calculating total loss" for details.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Source Voltage	V_{DD1}	4.5	5.0	5.5	V	PLL and CPU are operating
	V_{DD2}	3.5	5.0	5.5	V	PLL is OFF and CPU is operating
Data Holding Voltage	V_{DDR}	2.2		5.5	V	Quartz oscillator OFF
Source Voltage Rise Time	t_{rise}			500	ms	V_{DD} = 0 → 4.5 V
Input Amplitude	V_{IN1}	0.5		V_{DD}	V_{P-P}	VCOL, VCOH
	V_{IN2}	0.5		V_{DD}	V_{P-P}	AMIFC, FMIFC
Output Withstand Voltage	V_{BDS}			16.0	V	$P1B_1$ - $P1B_3$
Operating Temperature	T_{opt}	−40		+85	°C	

Calculation total loss

The μPD17010 has three types of power consumption and the chip must be designed so that the sum of these figures is less than total Pt (80 % of rating is recommended).

① CPU loss : Calculated as V_{DD} (MAX.) × I_{DD} (MAX.)
② Output pin loss : Loss calculated when each output pin outputs maximum current
③ Pull down resistor loss: Power loss due to internal pulldown resistance

Example Assuming that the following power is output from the output pins.

• High output	:	$P2A_0$ pin	12 mA
		LCD_0 pin	12 mA
		LCD_1 pin	1 mA
		$P0B_0$-$P0B_2$ pins	12 mA
		$P0B_3$ pin	4 mA
• Low output	:	$P0A_0$-$P0A_2$ pins	15 mA
		$P0A_3$ pin	5 mA
		$P0C_0$, $P0C_1$ pins	10 mA

The $P0D_0$ to $P0D_3$ pins are supplied with a 0.3 mA current when the internal pull-down resistor is on.

① CPU loss	:	5.5 V × 15 mA = 82.5 mW		
② Output pin loss	:	$P2A_0$ pin	···2.4 V × 12 mA	= 28.8 mW
		LCD_0 pin	···3 V × 12 mA	= 36 mW
		LCD_1 pin	···1 V × 1 mA	= 1 mW
		$P0B_0$-$P0B_2$ pins combined	···2.4 V × 12 mA × 3	= 86.4 mW
		$P0B_3$ pin	···1 V × 4 mA	= 4 mW
		$P0A_0$-$P0A_2$ pins combined	···2 V × 15 mA × 3	= 90 mW
		$P0A_3$ pin	···2 V × 5 mA	= 10 mA
		$P0C_0$, $P0C_1$ pins combined	···2 V × 10 mA × 2	= 40 mW
③ Pull-down resistor loss:		$P0D_0$-$P0D_3$ pins combined	···5.5 V × 0.3 mA	= 1.7 mW

Pt = ① + ② + ③ = 82.5 + (28.8 + 36 + 1 + 86.4 + 4 + 90 + 10 + 40) + 1.7 = 380.4 mW

Since the absolute maximum rating of the total loss is 450 mW, the figures in the above example do not exceed the rating. These values should be taken into account in the design.

DC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and PLL are operating
	V_{DD2}	3.5	5.0	5.5	V	CPU is operating and PLL is OFF
Source Current	I_{DD1}		1.2	2.4	mA	CPU is operating and PLL is OFF. X_{IN} pin Sine wave input (f_{IN} = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C
	I_{DD2}		0.45	0.90	mA	CPU is operating, PLL is OFF, and HALT instruction is used (20 instructions executed per 1 ms). X_{IN} pin Sine wave input (f_{IN} = 4.5 MHz, V_{IN} = V_{DD}), T_a = 25 °C
Data Holding Voltage	V_{DDR1}	3.5		5.5	V	Power failure detection by timer FF, quartz oscillator oscillating
	V_{DDR2}	2.2		5.5	V	Power failure detection by timer FF, quartz oscillator not oscillating
	V_{DDR3}	2.0		5.5	V	Data memory (RAM) holding
Data Holding Current	I_{DDR1}		2	5	μA	Quartz oscillator not oscillating T_a = 25 °C
	I_{DDR2}		2	3	μA	Quartz oscillator not oscillating V_{DD} = 5.0 V, T_a = 25 °C
Intermediate Level Output Voltage	V_{OM1}	2.3	2.5	2.7	V	COM_0, COM_1 V_{DD} = 5 V
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P1A_0$ - $P1A_3$, $P1D_0$ - $P1D_3$, CE, INT_0, INT_1
	V_{IH2}	0.6 V_{DD}		V_{DD}	V	$P0D_0$ - $P0D_3$
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD}	V	$P0A_0$ - $P0A_3$, $P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P0D_0$ - $P0D_3$, $P1A_0$ - $P1A_3$, $P1D_0$ - $P1D_3$, CE, INT_0, INT_1
High Level Output Current	I_{OH1}	−2.0	−10.0		mA	$P0A_0$, $P0A_1$, $P1A_1$ - $P1A_3$, $P2A_0$ V_{OH} = V_{DD} −2 V, V_{DD} = 5 V, T_a = 25 °C
	I_{OH2}	−1.0	−5.0		mA	$P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P1A_0$, $P1B_0$, $P1C_0$ - $P1C_3$ V_{OH} = V_{DD} −1 V
	I_{OH3}	−1.0	−4.0		mA	LCD_0 - LCD_{29}, EO_0, EO_1 V_{OH} = V_{DD} − 1 V

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Low Level Output Current	I_{OL1}	5.0	15.0		mA	$P0A_0$ - $P0A_3$, $P1A_1$ - $P1A_3$, $P2A_0$ V_{OL} = 2 V, V_{DD} = 5 V, T_a = 25 °C
	I_{OL2}	1.0	7.0		mA	$P0B_0$ - $P0B_3$, $P0C_0$ - $P0C_3$, $P1B_0$, $P1C_0$ - $P1C_3$ V_{OL} = 1 V
	I_{OL3}	1.0	3.5		mA	LCD_0 - LCD_{29}, EO_0, EO_1 V_{OL} = 1 V
	I_{OL4}	1.0	2.0		mA	$P1B_1$ - $P1B_3$ V_{OL} = 1 V
High Level Input Current	I_{IH1}	0.1	0.8		mA	VCOH pull-down V_{IH} = V_{DD}
	I_{IH2}	0.1	0.8		mA	VCOL pull-down V_{IH} = V_{DD}
	I_{IH3}	0.1	1.3		mA	X_{IN} pull-down V_{IH} = V_{DD}
	I_{IH4}	0.05	0.13	0.30	mA	$P0D_0$ - $P0D_3$ pull-down V_{IH} = V_{DD}
Output Off Leak Current	I_{L1}			500	nA	$P0A_2$, $P0A_3$ V_{OH} = V_{DD}
	I_{L2}			500	nA	$P1B_1$ - $P1B_3$ V_{OH} = 16 V
	I_{L3}			±100	nA	EO_0, EO_1 V_{OH} = V_{DD}, V_{OL} = 0 V

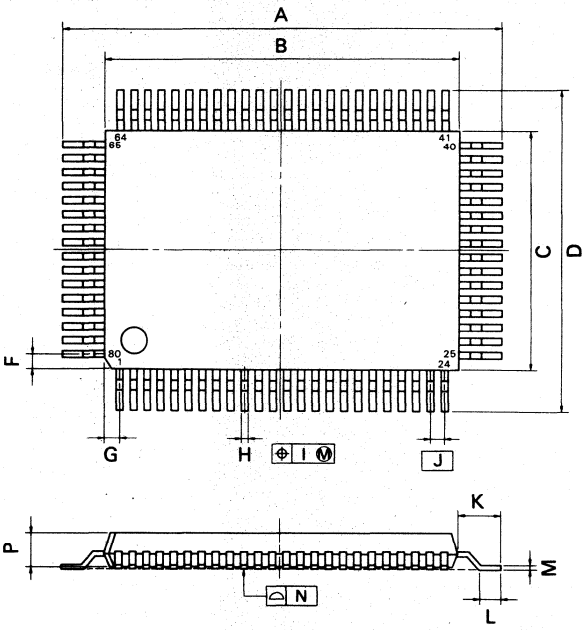
AC CHARACTERISTICS (Unless otherwise specified, T_a = −40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

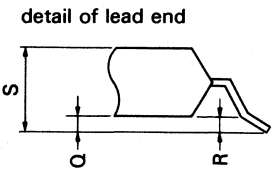
CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{IN1}	0.5		30	MHz	VCOL MF mode, sine wave input V_{IN} = 0.3 V_{P-P}
	f_{IN2}	5		40	MHz	VCOL HF mode, sine wave input V_{IN} = 0.3 V_{P-P}
	f_{IN3}	9		150	MHz	VCOH, sine wave input V_{IN} = 0.3 V_{P-P}
	f_{IN4}	0.1		1	MHz	AMIFC, sine wave input V_{IN} = 0.5 V_{P-P}
	f_{IN5}	0.44		0.46	MHz	AMIFC, sine wave input V_{IN} = 0.05 V_{P-P}
	f_{IN6}	5		15	MHz	FMIFC, sine wave input V_{IN} = 0.5 V_{P-P}
	f_{IN7}	10.5		10.9	MHz	FMIFC, sine wave input V_{IN} = 0.06 V_{P-P}
AD Converting Resolution				6	bit	
Total Error of AD Conversion			±1	±1.5	LSB	T_a = −10 to +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITION
		MIN.	TYP.	MAX.	UNIT	
Source Current	I_{DD3}		15		mA	CPU and PLL are operating VCOH sine wave input f_{IN} = 150 MHz, V_{IN} = 0.3 V_{P-P} V_{DD} = 5 V, T_a = 25 °C
High Level Output Current	I_{OH4}		−0.2		mA	COM_0, COM_1 V_{OH} = V_{DD} − 1 V
Intermediate Level Output Current	I_{OM1}		−20		μA	COM_0, COM_1 V_{OM} = V_{DD} − 1 V
	I_{OM2}		20		μA	COM_0, COM_1 V_{OM} = 1 V
Low Level Output Current	I_{OL5}		0.2		mA	COM_0, COM_1 V_{OL} = 1 V

PACKAGE DIMENSION
80 PIN PLASTIC QFP (14×20)





S80GF-80-3B9

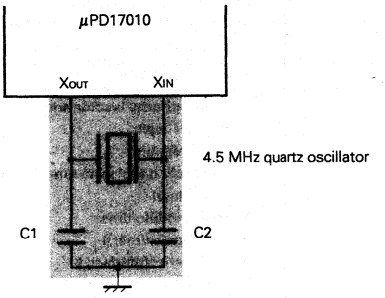
NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

APPENDIX A CAUTIONS TO BE TAKEN WHEN CONNECTING THE QUARTZ OSCILLATOR

The marked gray area in the figure must be handled as described below to prevent affecting wire capacity when using a system clock.

- Make the wires as short as possible.
- If C1 and C2 are made too large, the oscillator start characteristics deteriorate and power consumption increases.
- The oscillator wave adjustment trimmer capacitor should normally be connected to the XIN pin. However, the oscillation stability varies with the quartz oscillator. Test the oscillator before connecting it.
- Connecting an emulation probe to the XOUT and XIN pins may often not provide an accurate adjustment due to probe capacity. Use an LCD drive waveform (125 Hz) or a VCO oscillator frequency for measurement.



APPENDIX B DIFFERENCES BETWEEN μPD17010 and μPD17005

(1) Hardware

Item	μPD17010	μPD17005
ROM	7932 × 16 bits	
RAM	432 × 4 bits	
System Register	41 × 4 bits	33 × 4 bits
General Register Pointer	5 bits	4 bits
Stack Levels	9 levels	7 levels
Serial Interface	• SIO0 clock 37.5, 75, 112.5, 225 kHz • SIO1 clock External, 37.5, 75, 450 kHz • SCL, SDA, $\overline{SCK_0}$, $\overline{SCK_1}$, SI_0 and SI_1 pins have hysteresis characteristics	• SIO1 clock 75, 150, 225, 450 kHz • SIO2 clock External, 75, 150, 450 kHz
D/A Converter	Frequency: 4394.5 kHz	Frequency: 878.9 kHz
Interrupts	• Interrupt priority (vector address) 1. (6H) INT_0 pin 2. (5H) INT_1 pin (This pin doubles as timer count overflow) 3. (4H) modulo timer 4. (3H) basic timer 1 5. (2H) serial interface 0 6. (1H) frequency counter • Automatic backup of system registers (3 levels) (WR, BANK, RP, PSWORD) • Change address of IRQxxx flag	• Interrupt priority (vector address) 1. (5H) INT_0 pin 2. (4H) INT_1 pin 3. (3H) timer 4. (2H) serial interface 1 5. (1H) frequency counter • Automatic backup of system registers (4 levels) (BANK and IXE)
Timers	• Basic timer 0 carry • Basic timer 1 interrupt (Clock: 4, 10, 200 and 1000 Hz) • Modulo timer (Clock: 1, 3, 90 and 100 kHz)	• Timer carry • Timer interrupt (Clock: 4, 10, 200 and 1000 kHz)
PLL Frequency Synthesizer	• No LPF (Low pass filter)	• Internal LPF operational amplifier

(2) Software

Item	μPD17010	μPD17005
Interrupt Request Flag	A write instruction (POKE) or a macro instruction with a built-in flag operation can be used.	An error occurs during assembling when a write (POKE) instruction or a macro instruction with a built-in flag operation is used. The following is a list of relevant flags. • IRQIFC • IRQSIO1 • IRQTM • IRQ1 • IRQ0
IF Counter Control Register	A read instruction (PEEK) can be used. At this time "0" is read. The SETn instruction can also be used.	An error occurs during assembling when a read (PEEK) instruction is used. Consequently, macro instructions that generate PEEK instruction objects cannot be used when the SETn instruction is in use. • IFCRES • IFCSTRT

(3) Development tool

Item		μPD17010	μPD17005
Hardware	SE Board	SE-17010	SE-17005
	Emulation Probe	EP-17003GF	
Software	Device File	AS17010	AS17005
	Macrolibrary	No	• IFCSET.LIB • IRQ.MAC

(4) Cautions related to reserved word names

The reserved words of the μPD17010 control register differ slightly from those of μPD17005. The following is a list of reserved words that differ from those of the μPD17005.

Item	μPD17010	μPD17005
Timer	BTM1CK1	TMMD3
	BTM1CK0	TMMD2
	BTM0CK1	TMMD1
	BTM0CK0	TMMD0
	BTM0CY	TMCY
	TMCK3	
	TMCK2	
	TMCK1	
	TMCK0	
	TMOVF	
	TMRPT	
	TMRES	
	TMEN	
PLL frequency synthesizer	PLULSEN3	PLULDLY3
	PLULSEN2	PLULDLY2
	PLULSEN1	PLULDLY1
	PLULSEN0	PLULDLY0
	PLLRFCK3	PLLRFMD3
	PLLRFCK2	PLLRFMD2
	PLLRFCK1	PLLRFMD1
	PLLRFCK0	PLLRFMD0
D/A converter	PWM2SEL	PWM2ON
	PWM1SEL	PWM1ON
	PWM0SEL	PWM0ON
	CGPSEL	CGON
LCD driver	P0YSEL	P0YON
	P0XSEL	P0XON
	P0ESEL	P0EON
	P0FSEL	P0FON
IF	IFCGOSTT	IFCG

Item	μPD17010	μPD17005
Serial interface	SIO1TS	SIO2TS
	SIO1HIZ	SIO2HIZ
	SIO1CK1	SIO2CK1
	SIO1CK0	SIO2CK0
	SIO0CH	SIO1CH
	SIO0MS	SIO1MS
	SIO0TX	SIO1TX
	SIO0NWT	SIO1NWT
	SIO0WRQ1	SIO1WRQ1
	SIO0WRQ0	SIO1WRQ0
	SIO0WSTT	
	SIO0SF8	SIO1SF8
	SIO0SF9	SIO1SF9
	SIO0IMD3	SIO1IMD3
	SIO0IMD2	SIO1IMD2
	SIO0IMD1	SIO1IMD1
	SIO0IMD0	SIO1IMD0
	SIO0CK3	SIO1CK3
	SIO0CK2	SIO1CK2
	SIO0CK1	SIO1CK1
	SIO0CK0	SIO1CK0
Interrupts	IGRPSL	
	IPSIO0	IPSIO1
	IPBTM1	IPTM
	IPGRP	IP1
	IPTM	
	IRQSIO0	IRQSIO1
	IRQBTM1	IRQTM
	IRQTM	
	IRQGRP	IRQ1

4-BIT SINGLE-CHIP MICROCONTROLLER

μPD17P010 is the 4-bit single-chip microcontroller for digital tuning system which incorporates the prescaler operational up to 150 MHz, PLL frequency synthesizer, LCD driver, and IF counter.

Since the CPU has no any accumulator and adopts 17K architecture which can control the data memory directly, you can perform very efficient programming. It is necessary to be noted that any instruction is 16-bit length 1 word.

PLL frequency synthesizer can operate in pulse swallow system and select such high frequency as 50 or 100 kHz, which makes it much easier to configure a high performance tuner. Since it also incorporates 16-bit frequency counter, you can use it for the detection of broadcast by counting the intermediate frequency of a tuner.

IE-17K (incircuit emulator) and AS17K (assembler) are available, which are easy-to-use as the tools of μPD17P010 system development.

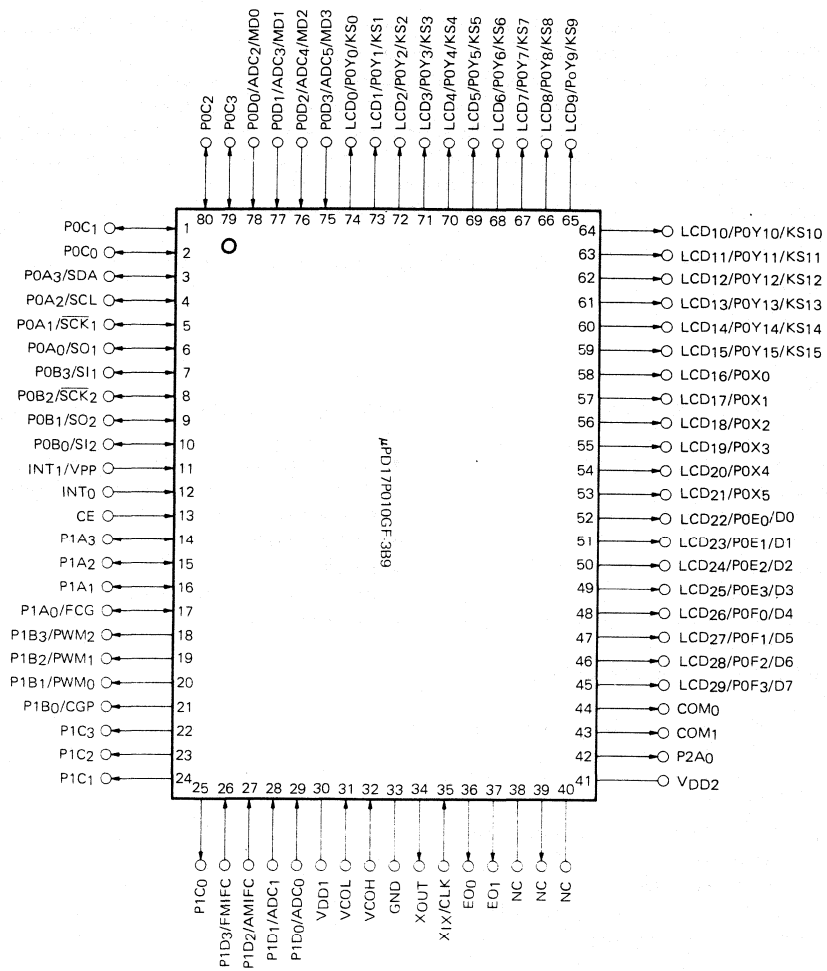
Since it incorporates One-Time PROM, it is useful for the system evaluation when developing the system of μPD17010*, and for small production.

* : Under development.

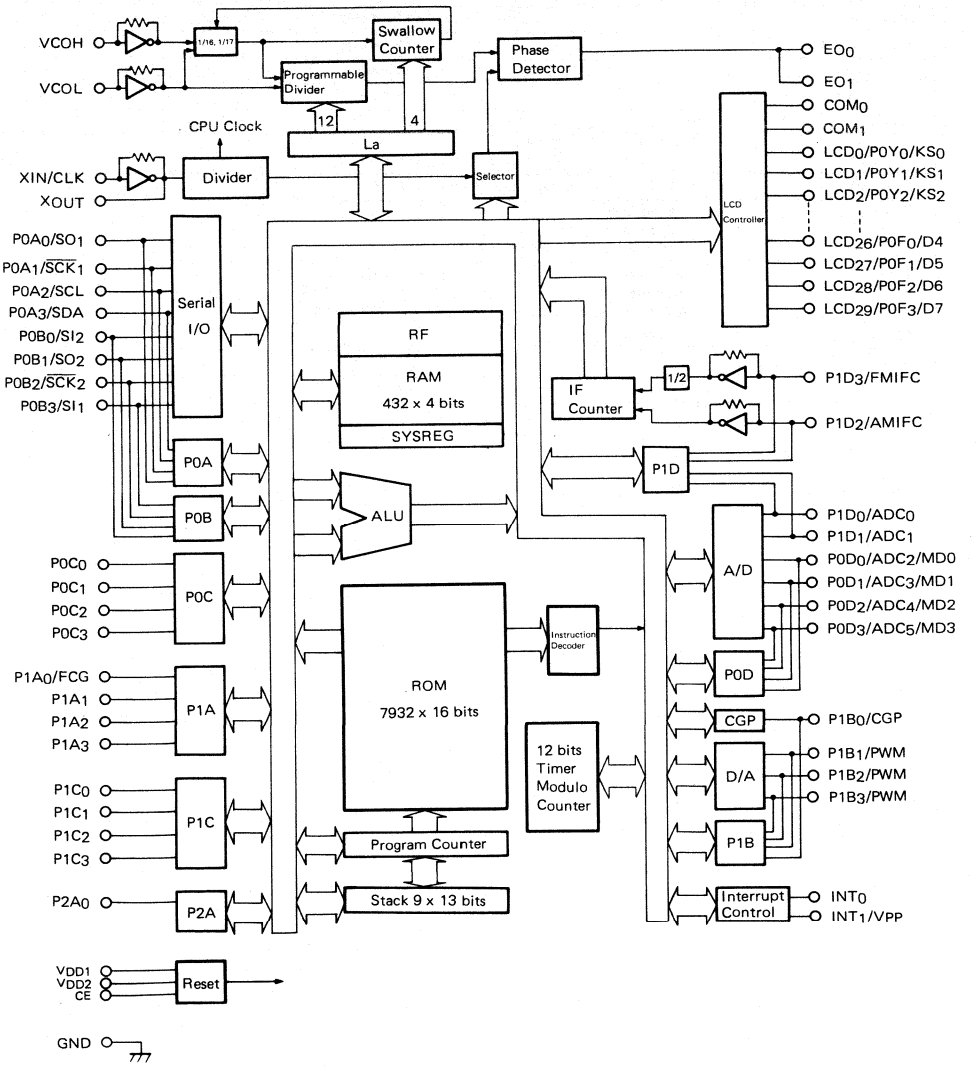
FEATURES

- 4-bit single chip microcontroller for digital tuning system
- Program memory (One-Time PROM): 7932 x 16 bits
- Data memory (RAM): 432 x 16 bits
- Stack level: 9
- Perceptible 35 types of instruction set
- Decimal operational
- Instruction execution time: 4.44 μs (when connecting a 4.5 MHz crystal resonator)
- On-chip PLL frequency synthesizer and 150 MHz prescaler
- 12 types of reference frequency selectable by program
- On-chip LCD driver (1/2 bias, 1/2 duty, frame frequency: 250 MHz)
- On-chip 8-bit serial interface (2 systems 3 channels: 3-wire and 2-wire)
- 12-bit timer modulo counter
- On-chip 8-bit D/A converter: 3 outputs (PWM)
- On-chip 6-bit A/D converter: 6 inputs
- On-chip service interruption detector and power-on reset circuit
- Interrupt (external: 2 systems, internal: 4 systems)
- Various I/O ports available (33 ports (+30 ports: Segment pins))
- On-chip CGP (Clock Generator Port)
- 5 V ±10 %
- CMOS low power consumption
- 80-pin plastic QFP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM

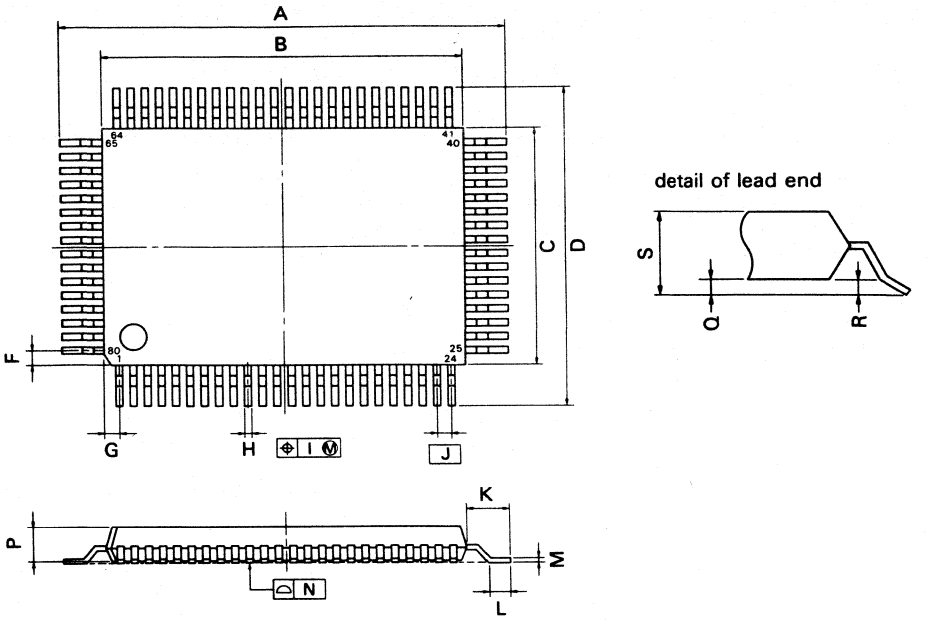


FUNCTION LIST

Product Name	μPD17010	μPD17P010
ROM	7932 x 16 bits	
RAM	432 x 4 bits	
System register	12 x 4 bits	
Register file	41 x 4 bits	
Port register	7 x 4 bits	
Port	Input/output port : 16 ports Input port : 8 ports Output port : 9 ports (+30 ports: Segment pins)	
Serial interface	• 2 systems, 3 channels 8 bits, 3-wire and 2-wire	
Interrupt	• 6 channels External interrupt : 2 channels Internal interrupt : 4 channels	
Timer	Timer carry (1 ms, 5 ms, 100 ms, 250 ms) Timer interrupt (1 ms, 5 ms, 100 ms, 250 ms) 12-bit timer modulo counter (10 μs, 11.1 μs, 333.3 μs, 1 ms)	
Standby function	• STOP, HALT	
Power supply voltage	V_{DD} = 5 V ±10 %	
Package	80-pin plastic QFP	

PACKAGE DIMENSION

80 PIN PLASTIC QFP (14×20)



S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

SINGLE CHIP MICROCOMPUTER FOR PLL FREQUENCY SYNTHESIZER BUILT-IN IMAGE DISPLAY CONTROLLER

μPD17002 is a 4 bits CMOS microcomputer for digital tuning system in single chip incorporating an Image Display Controller with various kinds of display capability and a PLL frequency synthesizer.

CPU has 4-bit parallel addition and substruction instructions, logical operation instructions, bit test instructions, carry F/F set and reset instructions, interrupt function, and timer function. Built-in user programable IDC (Image Display Controller) controls various kinds of display with easy program. This IC is made of 48 pin plastic shrink DIP (Dual In-Line Package) provided with plentiful I/O (Input/Output) ports controlled by effective input/output instructions, serial interface function, 4 bits A/D converter and 6 bits PWM output.

FEATURES

- 4 bits microcomputer for digital tuning system
- built-in PLL frequency synthesizer using prescaler: μPB568
- single power supply (5 V ±10 %)
- CMOS with low power consumption
- program memory (ROM): 8 K byte (16 bits x 3 968 steps)
- data memory (RAM): 4 bits x 336 words
- stack level: 6
- 35 types of understandable instruction
- capable of decimal arithmetic
- instruction execution time: 2 μs (with 8 MHz crystal connected)
- IDC (Image Display controller) built-in (user programable)
  - number of display character : 97 characters (max. in one screen)
  - display location : 12 lines x 16 columns
  - number of character types : 120 types
  - character format : 10 x 15 dots (capable of fringe function)
  - character color : 8 colors
  - character size : 4 types of setting is available independently both for line and column (14, 28, 42, 56H)
- built-in 8 bits serial interface (1 system 2 channel: 3 wire and 2 wire system)
- built-in D/A converter: 6 bits x 4 (PWM output)
- built-in A/D converter: 4 bits x 6
- built-in H. Sync. signal counter
- built-in commercial power supply frequency counter
- built-in power-up detection circuit and power-on-reset circuit
- interrupt input for remote control signal (with noise canceller)
- plentiful I/O ports
  - input output port : 15
  - input port : 4
  - output port : 8

ORDERING INFORMATION

Order Code	Package
μPD17002CU-XXX	48-pin plastic shrink DIP (600 mil)

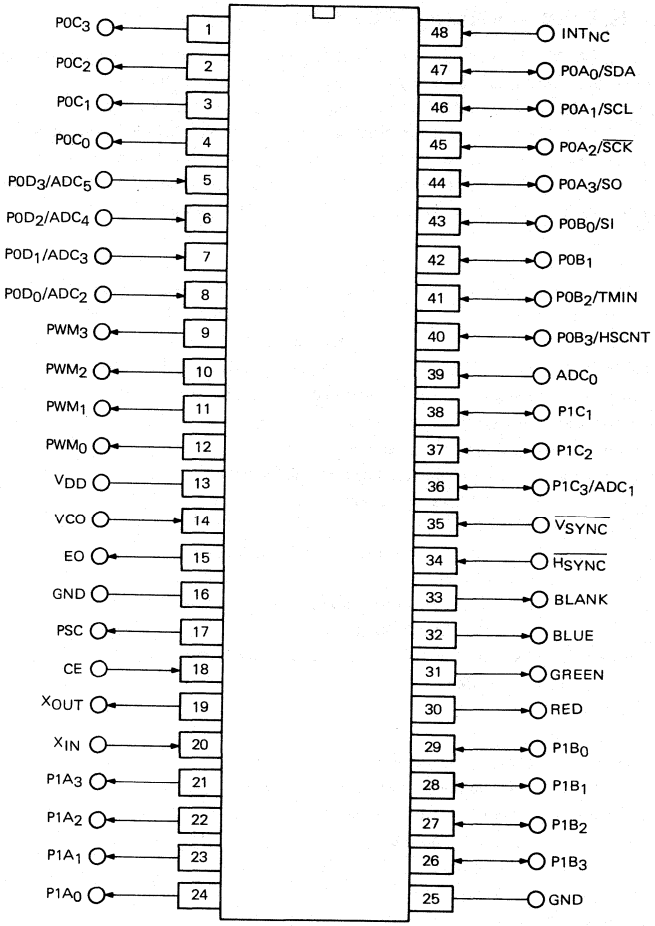
Notes on Serial Interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

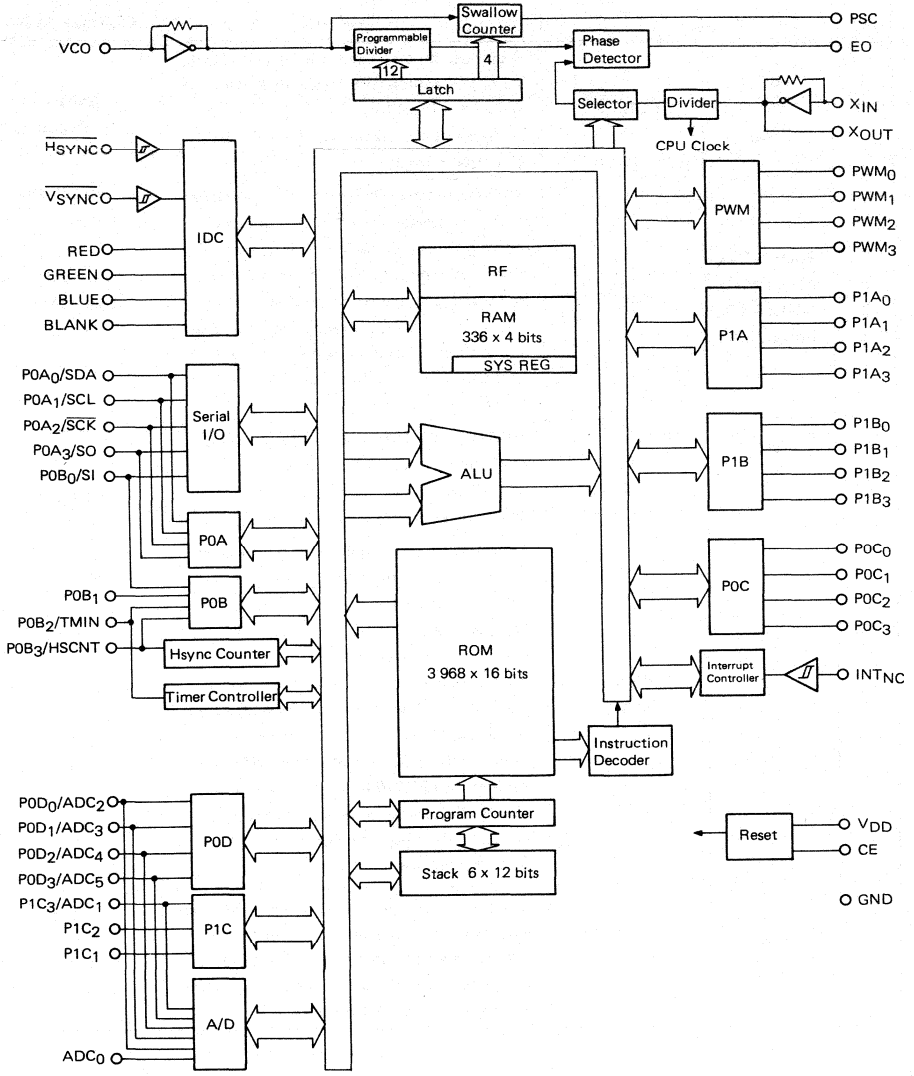
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONNECTION (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
1 to 4	$P0C_3$ to $P0C_0$	PORT 0C	4 bit output port. Latch for Port 0C is located at 72H address of BANK 0 or BANK 2 of data memory (RAM). Output status is unconstant at the initial power-on (V_{DD}).	CMOS push-pull
5 6 7 8	$P0D_3/ADC_5$ $P0D_2/ADC_4$ $P0D_1/ADC_3$ $P0D_0/ADC_2$	Port 0D	4 bit input port. These ports can be used also as A/D converter. When used as port, pull-down resistor (100 kΩ TYP.) is connected. The built-in 4-bit A/D converters employ the successive approximation method. The A/D converter reference voltage is V_{DD}. Latch for Port 0D is located at 73H address of BANK 0 or BANK 2 of data memory (RAM).	Input with pull-down resister
9 to 12	PWM_3 to PWM_0	D/A converter	VDP (Variable Duty Port) or output port. VDP function is to output the pulse of 15.625 kHz frequency sequently. The pulse duty is variable by 66-step program.	N-ch open-drain
13	V_{DD}	Power Supply	Device power supply pin. This pin supplies 5 V ±10 % while the device is operating with full functions. When only CPU operates (PLL and IDC stop), 4.0 to 5.5 V is supplied. This voltage can be dropped to 2.5 V to hold the internal data memory (RAM) with a STOP instruction. When the voltage applied to this pin changes from 0 to 4.0 V, the device is reset and the program starts from address 0 because the μPD17002 has a power-on reset circuit. To operate power-on reset circuit normally, the rising time (0→4.0 V) should be within 500 ms.	–
14	VCO	Local Oscillator Signal Input	Input the output of VCO (Voltage Controlled Oscillator) after frequency division by the μPB568 prescaler, that is the output of the prescaler. μPB568 is a Two-Modulus prescaler with division ratio (1 GHz MAX.).	Input (self-bias)

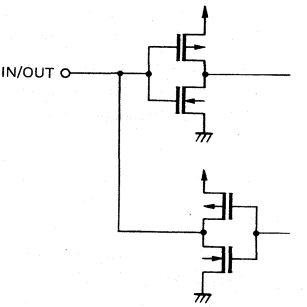
PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
15	EO	Error Output	PLL error output pin. If the frequency obtained by dividing the oscillation output of VCO is higher than the reference frequency, high level is output from this pin. Otherwise, low level is output. A floating condition results if the two frequencies are identical. The output is supplied through the LPF (Low Pass Filter) to the varacter diodes that form the VCO (Voltage Controlled Oscillator) as a tuning voltage.	CMOS 3-state
16 25	GND	Ground	Device ground pin. Both pins should be connected to the ground.	–
17	PSC	Pulse Swallowing Control Output	Pin used to output a frequency division ratio switching signal to the μPD568. Connected directly to the PSC pin of the μPB568. The ratios are 1/128 and 1/136 (or 1/64 and 1/68).	CMOS push-pull
18	CE	Chip Enable	Device selection signal input pin. This pin must be high level to enable the device and low level to disable the device. When a STOP instruction in the program is executed while the CE pin is low level, the internal clock generator and CPU stop, and the memory can enter the hold state requiring low power consumption. STOP instruction is effective only when CE pin is low level, and when high level, works as same as NOP instruction. When CE pin goes to the high level from the low level, the device is reset and the program starts from 0 address. When the device is reset, BANK turns 0 and I/O port enters the input mode.	Input
19 20	X_{OUT} X_{IN}	X'tal	Crystal oscillator connector pin. Connect a 8 MHz crystal resonator to this pin.	CMOS push-pull (X_{OUT}) Input (X_{IN})
21 to 24	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. Latch for this port is located at 70H address of e BANK 1 in the data memory (RAM). This pin is N-channel open drain type. (Breakdown Voltage: 12.5 V) (Sink Current: 20 mA TYP.)	N-ch open-drain

PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
26 to 29	$P1B_3$ to $P1B_0$	Port 1B	4-bit input output port. The input or output state of each bit can be specified in these ports. The input and output are set by the P1BBIO word (35H) in the resistor file. Latch for these ports are located at 71H address of BANK 1 in the data memory (RAM).	CMOS push-pull (I/O)
30 31 32	RED GREEN BLUE	Character Signal Output	Character data output pins for R. G. B. Active high output	CMOS push-pull
33	BLANK	Blanking Signal Output	Blanking signal output pin to cut video signal. (Active high output)	CMOS push-pull
34	$\overline{H_{SYNC}}$	H. Sync Signal Input	H. Sync. signal input pin for IDC (Active low input)	Input
35	$\overline{V_{SYNC}}$	V. Sync. Signal Input	V. Sync. signal input pin for IDC (Active low input). This signal can be used for interruption.	Input
36 37 38	$P1C_3/ADC_1$ $P1C_2$ $P1C_1$	Port 1C	3-bit input output port or A/D converter pin. The input or output state of each 3-bit can be set in these ports. The input and output are specified by the P1CGIO bit (#0 bit of 27H) in the resistor file. When used as A/D converter, input should be specified. Latch for this port is allocated at 72H address of BANK 1 in the data memory (RAM). Port 1C enters into input at initial power-on (V_{DD}), or at clock stop time or at reset time. (CE pin: Low→High)	CMOS push-pull (I/O)
39	ADC_0	AD Conversion	The A/D converter input pin. The built-in 4-bit A/D converters employ the successive approximation method. The A/D converter reference voltage is V_{DD}.	Input
40 41 42 43	$P0B_3$/HSCNT $P0B_2$/TMIN $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input output ports. The input or output state of each bit can be specified in these ports. The input and output are set by the P0BBIO word (36H) in the resistor file. Latch for these ports are located at 71H address of BANK 0 or BANK 2 in the data memory (RAM). $P0B_2$/TMIN can be used also as an external timer input. Interruption starts by the 1/5 or 1/6 of the frequency input to this pin.	CMOS push-pull (I/O) However $P0B_3$/HSCNT is self biased at input.

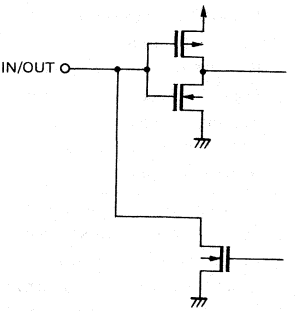
PIN No.	SYMBOL	PIN NAME	FUNCTION	OUTPUT TYPE
40 41 42 43	$P0B_3$/HSCNT $P0B_2$/TMIN $P0B_1$ $P0B_0$/SI	Port 0B	Usually commercial power supply frequency is input to this pin, and used as reference clock for timer. $P0B_0$/SI pin can be used also as a serial interface (μCOM standard mode) data input pin. $P0B_3$/HSCNT pin can be used also as a H. sync. signal counter input pin. Therefore this pin is self biased ($V_{DD}/2$) at any time. Port 0B turns input at the initial power-on (V_{DD}) or at clock stop time or at reset time (CE pin: Low→High).	CMOS push-pull (I/O) However $P0B_3$/HSCNT is self biased at input.
44 45 46 47	$P0A_3$/SO $P0A_2/\overline{SCK}$ $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input output port. The input or output state of each bit can be specified in these ports. The input and output are set by the P0ABIO word (37H) in the resistor file. Latch for these ports are located at 70H address of BANK 0 or BANK 2 in the data-memory (RAM). $P0A_3$/SO pin can be used also as a serial interface (μCOM standard mode) data output pin. $P0A_2/\overline{SCK}$ pin can be used also as a shift clock input output pin. $P0A_0$/SDA pin can be used as a serial interface (two wire mode and μCOM standard mode) data input output pin. $P0A_1$/SCL pin can be used as a shift clock input output pin.	$P0A_3$/SO $P0A_2/\overline{SCK}$ CMOS push-pull (I/O) P0A1/SCL $P0A_0$/SDA N-ch open-drain (I/O)
48	INT_{NC}	Interrupt Request Signal Input	Interrupt request signal input pin with noise canceller. This pin makes programming easy for a noisy signal such as a remote control signal. Program decides if interruption starts at rising time or at falling time of input signal into this pin. IEDG1 flag reset enters into interruption at rising time. IEDG1 flag set enters into interruption at falling time. At reset time (CE pin: Low→High), IEDG1 flag is reset and interruption starts at the rising edge.	Input

INPUT/OUTPUT CIRCUITS

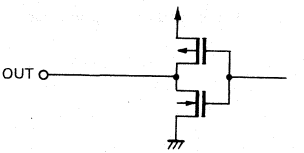
P0A ($P0A_3$/SO, $P0A_2$/$\overline{SCK}$)
P0B ($P0B_1$, $P0B_0$/SI)
P1B ($P1B_3$, $P1B_2$, $P1B_1$, $P1B_0$)
P1C ($P1C_3$/ADC_1, $P1C_2$, $P1C_1$)



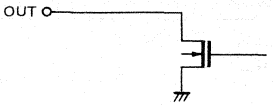
P0A ($P0A_1$/SCL, $P0A_0$/SDA)



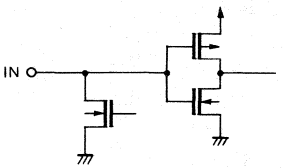
P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
RED, GREEN, BLUE, BLANK, PSC



PWM (PWM_3, PWM_2, PWM_1, PWM_0)
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)

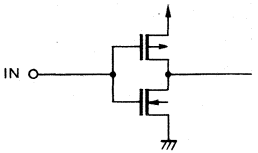


P0D ($P0D_3/ADC_5$, $P0D_2/ADC_4$, $P0D_1/ADC_3$, $P0D_0/ADC_2$)

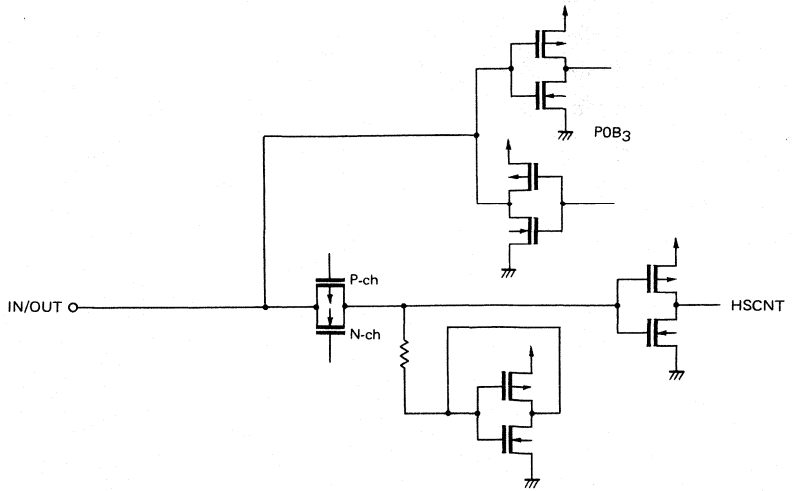


(High ON Register)

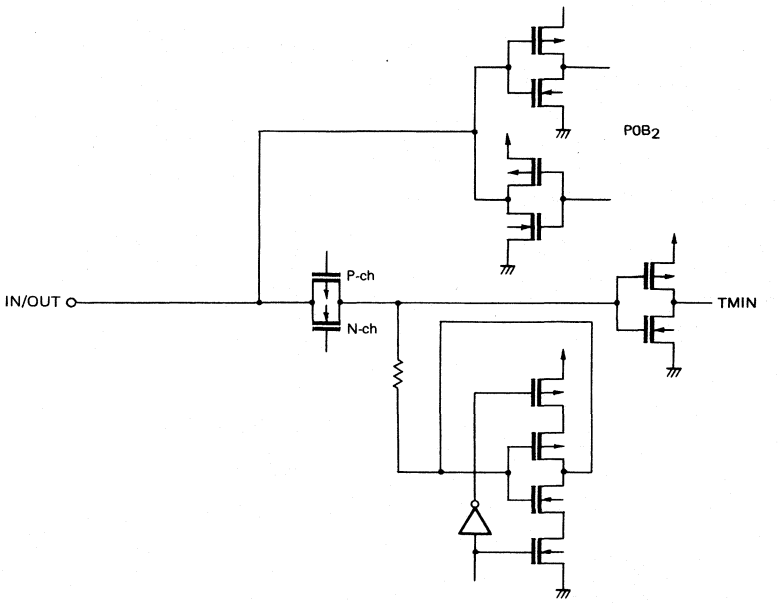
AD_0



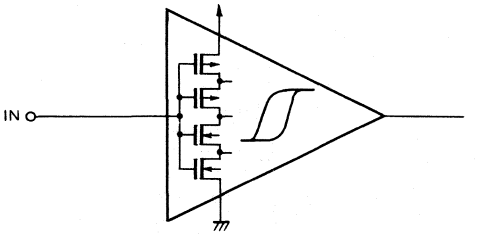
$P0B_3$/HSCNT



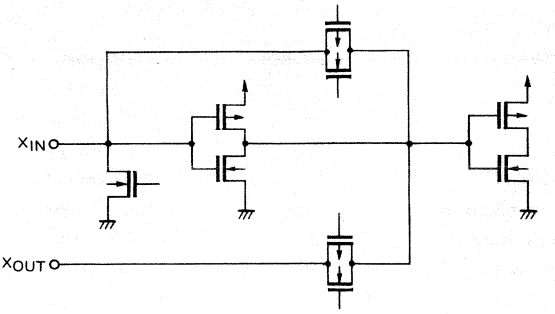
$P0B_2$/TMIN



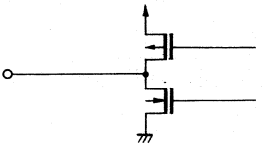
$\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, INT_{NC}, CE



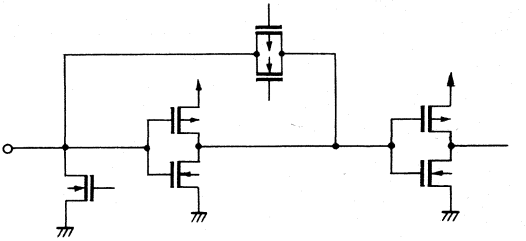
X_{OUT}, X_{IN}



EO



VCO



ELECTRICAL CHARACTERISTICS (TARGET SPEC)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Sink Current	I_O	10 (except P1A)	mA
Output Breakdown Voltage	V_{BDS}	13 (P1A, PWM)	V
Operating Temperature	T_a	−20 to +70	°C
Storage Temperature	V_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All functions operate (CPU, PLL, IDC)
Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only CPU operates
Data Retention Voltage	V_{DR}	3.0		5.5	V	Crystal oscillation stopped
Output Breakdown Voltage	V_{BDS}			12.5	V	P1A, PWM
Supply Voltage Rising Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{DD1}		8		mA	(T_a=25 °C)
Supply Current	I_{DD2}		1		mA	Only CPU operates (T_a=25 °C)
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	P0A, P0B, P0D, P1B, P1C
High Level Input Voltage	V_{IH2}	0.8 V_{DD}			V	CE, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Low Level Input Voltage	V_{IL2}			0.2 V_{DD}	V	CE, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
High Level Output Current	I_{OH}		–2	–1	mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, RED, GREEN, BLUE, BLANK $V_{OH}=V_{DD}-1$ V
Low Level Output Current	I_{OL1}	1	2		mA	P0A, P0B, P0C, P1B, P1C, RED, GREEN, BLUE, BLANK, PWM V_{OL}=1 V
Low Level Output Current	I_{OL2}	15	20		mA	P1A, V_{OL}=1 V
High Level Input Current	I_{IH}	100			μA	VCO, X_{IN}, $V_I=V_{DD}$=4.5 V
Data Retention Current	I_{DR}			10	μA	Crystal oscillation stopped (T_a=25 °C)
Output Leakage Current	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, PWM, EO, V_{IH}=5 V

AC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

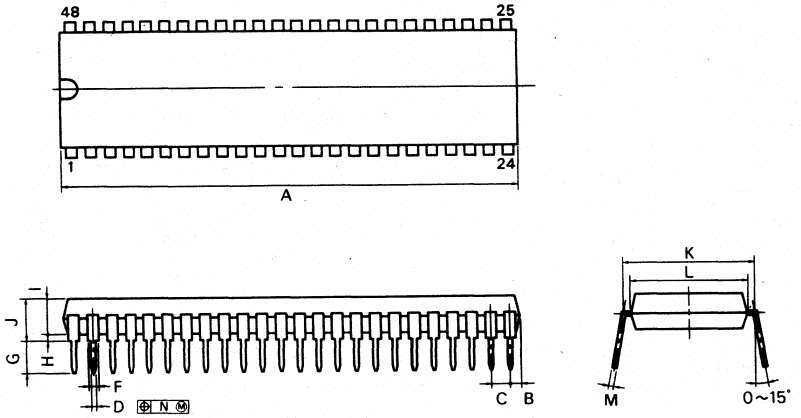
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Frequency	f_{TMR}	50		60	Hz	POB_2/TMIN
Input Frequency	f_{HS}	10		20	kHz	POB_3/HSCNT
IDC Jitter	IDC_G		4	6	ns	
IDC H. SYNC Start Position	IDC_{HP}		16.25		μs	from last edge of H. SYNC
IDC I. SYNC Start Position	IDC_{VP}		17		H	from last edge of V. SYNC
Operating Frequency	f_{in}			15	MHz	VCO (V_I=0.6 V_{P-P}, SIN WAVE)

A/D CONVERTER CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
A/D Conversion Absolute Accuracy		±1/2		±1	LSB	T_a=–10 to +50 °C
Input Impedance		1			MΩ	

PACKAGE DIMENTION

48PIN PLASTIC SHRINK DIP (600 mil)



P48C-70-600B

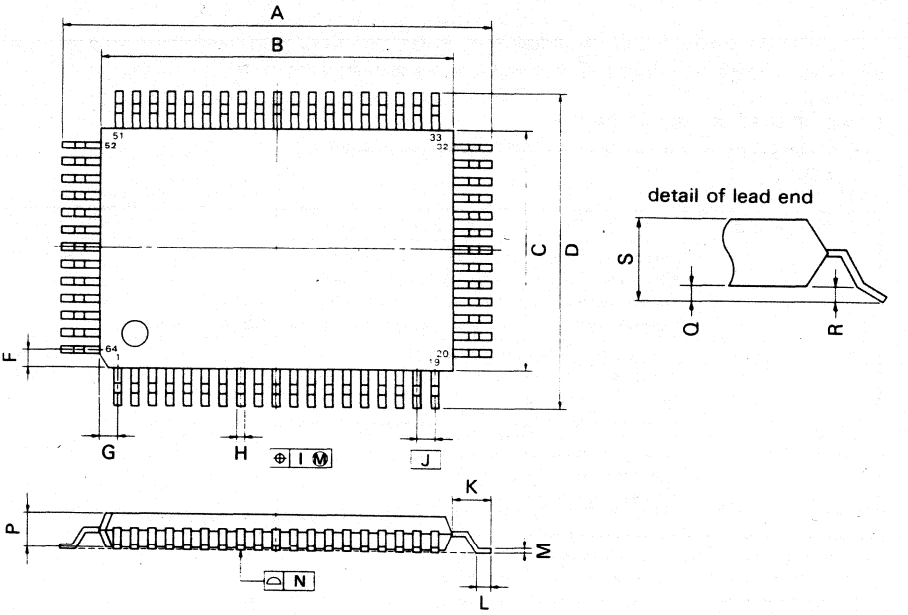
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	44.46 MAX.	1.751 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64 PIN PLASTIC QFP (14×20)



S64GF-100-3B8,3BE

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

RECOMMENDEDLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to out document "SMT MANUAL" (IEI-1207).

μPD17002

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 220 °C or below, Reflow time: 30 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	IR20–162
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	VPI5–162
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: 2 days (16 hours pre-backing is required at 125 °C afterwards)	WS60–162

*: Exposure limit before soldering after dry-pack package is opend.
Storage conditions: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "partial heating method".

BUILT-IN IMAGE DISPLAY CONTROLLER

The μPD17P008 is a 4 bits CMOS microcontroller incorporating One Time PROM, 2K bits EEPROM, Image Display Controller (IDC) and PLL frequency synthesizer into one chip for digital tuning of PLL frequency synthesizer system of TV.

Image Display Controller has various display function showing not only letters but also drawings.

Fonts of IDC are selected by user's program and effective debugging can be realized by actual indications from the beginning of software development.

In addition, Hsync. counter for station detection and serial interface for communication with other peripheral devices are incorporated, also 4 bits A/D converter 8 bits D/A converter (PWM output) and 6 bits D/A converter (PWM output) are incorporated.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instructions consist of 16 bits one word.

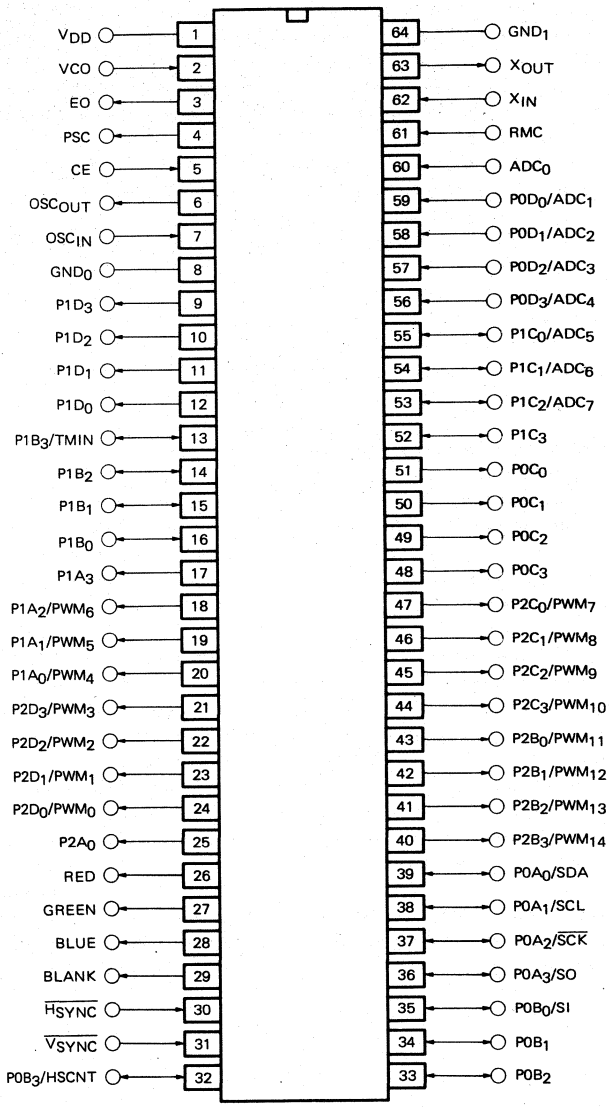
One Time PROM makes it perfect for system evaluation or small lot production of the mask ROM products μPD17008.

Package type is 64-pin plastic shrink DIP (Dual In-Line Package).

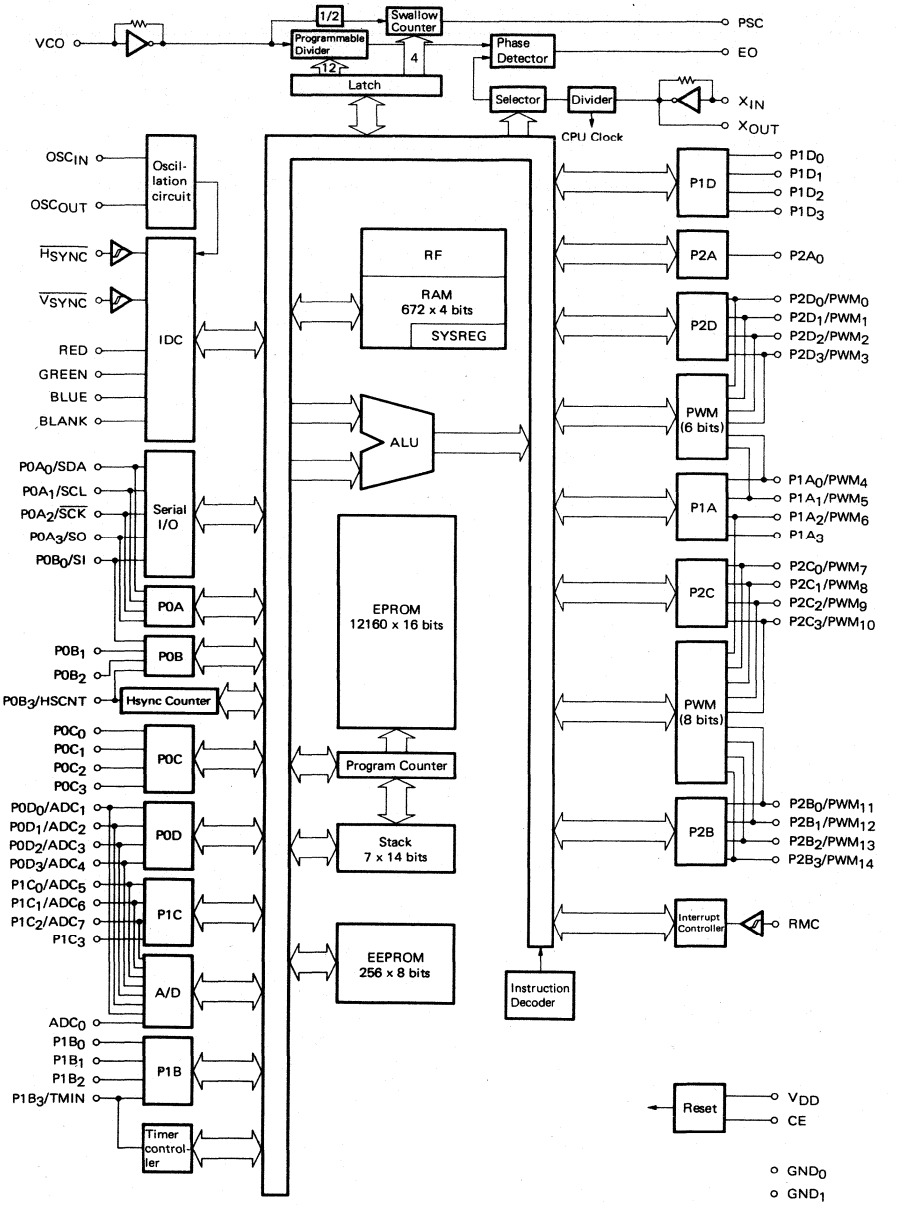
FEATURES

- 4 bits microcontroller for digital tuning system
- program memory (ROM):
  32K byte (16.256 steps x 16 bits)
- data memory (RAM): 672 words x 4 bits
- stack level: 7
- 36 types of understandable instruction
- capable of decimal arithmetic
- instruction execution time:
  2 μs (with 8 MHz crystal connected)
- built-in PLL frequency synthesizer
  using 1 GHz prescaler: μPB568
- IDC (Image Display Controller) built-in
  (user programmable)
  - number of display character:
    200 characters (max. in one screen)
  - display location: 14 lines x 19 columns
  - number of character types: 248 types
  - character format:
    10 x 15 dots (capable of fringe function)
    2-dot space between characters can be set.
  - character color: 8 colors
  - character size:
    4 types of setting is available independently both for line and column (14, 28, 42, 56H)
- built-in circuit to prevent 1-dot vertical flicker.
- built-in 8 bits serial interface:
  (1 system 2 channels: 3 wire and 2 wire systems)
- built-in D/A converter: 6 bits x 6 ch (PWM output)
  : 8 bits x 9 ch (PWM output)
- built-in A/D converter: 4 bits x 8 ch
- built-in H. Sync. signal counter
- built-in commercial power supply freq. counter
- built-in power-up detection circuit and power-on reset circuit.
- interrupt input for remote control signal
  (with noise canceller)
- plentiful I/O ports: input output port: 16
  input port : 4
  output port : 25
- single power supply (5 V ± 10 %)
- CMOS with low power consumption
- 64-pin plastic shrink DIP (600 mil)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



SINGLE-CHIP MICROCONTROLLER FOR VOLTAGE SYNTHESIZER WITH ON-CHIP IMAGE DISPLAY CONTROLLER

The μPD17051 is a 4-bit CMOS microcontroller for digital tuning systems with an on-chip image display controller (IDC) allowing various kinds of display and 14-bit D/A converter for voltage synthesizer use.

The CPU features include 4-bit parallel addition, logical operations, multiple bit testing, carry flag setting/resetting, powerful interrupt functions and timer functions.

The on-chip user-programmable image display controller for on-screen enables easy program control of various kinds of display.

The μPD17051 comes in 48-pin plastic shrink DIP form, and has a wide range of I/O port and serial interface functions controlled by powerful input/output instructions, plus a 4-bit A/D converter and 6-bit PWM output.

FEATURES

- 4-bit microcontroller for digital tuning systems
- On-chip 14-bit D/A converter for voltage synthesizer
- Programmable memory (ROM) : 16K bytes (8192 steps × 16 bits)
- Data memory (RAM) : 448 words × 4 bits
- Stack levels : 6
- 35 easy-to-understand instruction sets
- Decimal operation capability
- Instruction execution time : 2 μs (with 8 MHz oscillator connected)
- On-chip IDC (user-programmable)
  - Display capacity : Max. 97 characters per screen
  - Display positions : 14 rows × 19 columns
  - Character set : 128 characters (64 simultaneously usable per screen)
  - Character format : 10 × 15 dots (bordering capability)
  - Colors : 8
  - Character size : 4 independent vertical/horizontal settings (15, 30, 45, 60 H) (2.5, 5.0, 7.5 10 μs)
- On-chip 8-bit serial interface (1 system: 3-wire or 2-wire)
- On-chip D/A converter : 6 bits × 3 (PWM output)
- On-chip A/D converter : 4 bits × 8
- On-chip horizontal synchronization signal counter
- On-chip commercial power supply frequency counter
- On-chip power outage detection circuit and power-on reset circuit
- Remote control signal interrupt input (with noise canceler)
- Many I/O ports
  - Input/output ports : 16
  - Input ports : 5
  - Output ports : 10
- 5 V ±10 %
- Low power consumption CMOS

ORDERING INFORMATION

Order Code	Package
μPD17051CU-xxx	48-Pin Plastic Shrink DIP (600 mil)

Notes on Serial interface: **The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:**

Duties when using I2C bus system

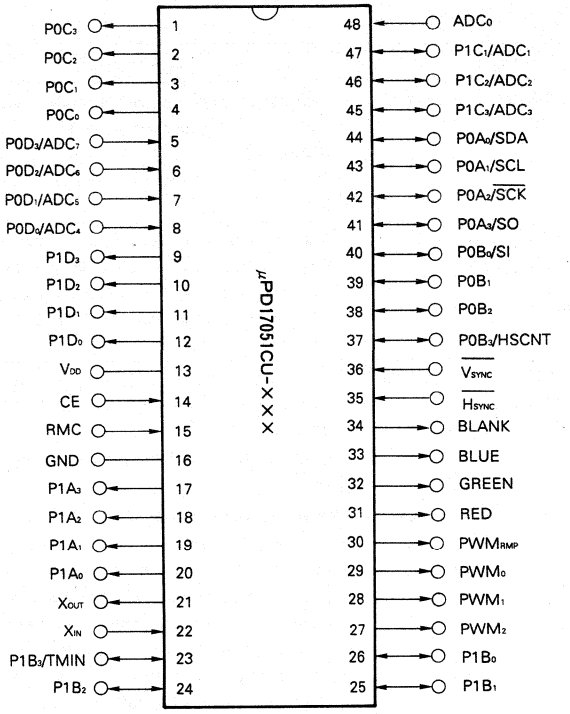
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

FUNCTIONAL OUTLINE

Item	Function
Program memory	• 16K bytes (8192 steps × 16 bits) Table reference area : 256 steps CROM dual-function area : 2048 steps
Data memory	• 448 words (448 words × 4 bits) Data buffer : 4 words General-purpose registers : 16 words VRAM dual-function area : 224 words
System registers	• 12 words
Register file	• 24 words (control registers)
Port registers	• 8 words
Instruction execution time	• 2 μs (using 8 MHz ceramic oscillator)
Stack levels	• 6 levels (stack manipulation capability)
General-purpose ports	• Input/output ports : 16 • Input ports : 5 • Output ports : 10
IDC (Image Display Controller)	• Display capacity : 97 characters per screen • Display positions : 14 rows × 19 columns • Character set : 128 characters (user-programmable) (64 different characters simultaneously displayable per screen) • Character format : 10 × 15 dots • Colors : 8 • Character size : 4 vertical (15, 30, 45, 60 H) 4 horizontal (2.5, 5.0, 7.5 10 μs) Independent vertical/horizontal setting capability
Serial interface	• 1 system (2 channels) 8-bit 3-wire: 1 channel 8-bit 2-wire: 1 channel
D/A converter	• 14-bit × 1 (PWM output, Max. 12.5 V withstand voltage) • 6-bit × 3 (PWM output, Max. 12.5 V withstand voltage)
A/D converter	• 4-bit × 8 (software-driven successive approximation method)
Interrupts	• 4 channels (maskable interrupts) External interrupts: 2 channels (RMC pin, $\overline{V_{SYNC}}$ pin) Internal interrupts: 2 channels (timer, serial interface)
Timer	• 2 systems Internal timer : 5, 20, 100 ms External timer : 1/5, 1/6 frequency input to P1B3/TMIN pin
Reset	• Power-on reset (on powering-on) • Reset by CE pin (CE pin: Low → high) • Power outage detection function
Supply voltage	5 V ± 10 %
Package	48-pin plastic shrink DIP (600 mil)

PIN CONFIGURATION (Top View)



ADC0 to ADC7	:	A/D converter inputs
CE	:	Chip enable
RMC	:	Interrupt signal input
XIN, XOUT	:	Oscillator
TMIN	:	External timer input
PWM0 to PWM2	:	D/A converter outputs
PWMRMP	:	Station selection D/A converter output
RED	:	Character signal output
GREEN	:	Character signal output
BLUE	:	Character signal output
BLANK	:	Blanking signal output
$\overline{\text{HSYNC}}$	:	Horizontal synchronization signal input
$\overline{\text{VSYNC}}$	:	Vertical synchronization signal input
HSCNT	:	Horizontal synchronization signal counter input
SI	:	Data input
SO	:	Data output
$\overline{\text{SCK}}$	:	Shift clock input/output
SCL	:	Shift clock input/output
SDA	:	Data input/output
P0A0 to P0A3	:	Port 0A
P0B0 to P0B3	:	Port 0B
P0C0 to P0C3	:	Port 0C
P0D0 to P0D3	:	Port 0D
P1A0 to P1A3	:	Port 1A
P1B0 to P1B3	:	Port 1B
P1C0 to P1C3	:	Port 1C
P1D0 to P1D3	:	Port 1D
VDD	:	Power supply
GND	:	Ground

1. PIN FUNCTIONS

1.1 SUMMARY OF PIN FUNCTIONS

PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
1 to 4	$P0C_3$ to $P0C_0$	Port 0C	4-bit output port. Port 0C latch is located in address 72H of data memory (RAM) BANK0 or BANK2. Output status is undefined after power-on reset.	CMOS push-pull
5 6 7 8	$P0D_3/ADC_7$ $P0D_2/ADC_6$ $P0D_1/ADC_5$ $P0D_0/ADC_4$	Port 0D	4-bit input port or A/D converter input pins. When used as a port, a pull-down resistor (100 kΩ TYP.) is attached. Port 0D latch is located in address 73H of data memory (RAM) BANK0 or BANK2.	Input (with pull-down resistor)
9 to 12	$P1D_3$ to $P1D_0$	Port 1D	4-bit output port. Port 1D latch is located in address 73H of data memory (RAM) BANK1 or BANK3. Output status is undefined after power-on reset.	CMOS push-pull
13	V_{DD}	Power supply	Device power supply pin. Supplies 5 V ±10 % voltage when all functions are operated. When IDC is not used, device operations on 4 to 5.5 V. When RAM data is retained (when clock oscillation is stopped) voltage can be reduced to approx. 2.2 V. As the μPD17051 incorporates a power-on reset circuit, a 0 → 4.0 V transition effects a system reset and the program starts at address 0. To ensure proper operation of the power-on reset circuit, the rise time from 0 to 4.0 V should be within 500 ms.	———
14	CE	Chip enable	Device selection signal input pin. Driven high when the device is operated normally, and low when the device is not used. When this pin is low, execution of the STOP instruction stops clock oscillation, allowing low-current-consumption backup. The STOP instruction is only effective when the CE pin is low; when high, this instruction operates identically to an NOP instruction. This pin has a dual function as a reset pin; A low-to high transition of the CE pin resets the device and	Input

PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
14	CE	Chip enable	the program starts from address 0. When the device is reset, bank 0 is selected and I/O ports are placed in input mode. Note however that a low-level signal of 188 us or less is not acknowledged.	
15	RMC	Interrupt signal input	Interrupt input pin with noise canceler. Using this pin for noisy signals such as remote control signals facilitates programming. Whether an interrupt is generated on the rise or the fall of the input signal to this pin can be specified by the program. An interrupt is generated on a rise when the IEDG1 flag is reset, and on a fall when this flag is set. In a CE reset the IEDG1 flag is rest, and an interrupt is thus generated on a rise of the signal	Input
16	GND	Ground	Device ground pin.	———
17 to 20	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. Port 1A latch is located in address 70H of data memory (RAM) BANK1 or BANK3. N-ch open-drain type (medium voltage, high current).	N-ch open-drain
21 22	X_{OUT} X_{IN}	Oscillator	Ceramic oscillator or crystal resonator connection pins. An 8 MHz oscillator/resonator should be used.	CMOS push-pull (X_{OUT}) Input (X_{IN})
23 24 25 26	$P1B_3$/TMIN $P1B_2$ $P1B_1$ $P1B_0$	Port 1B	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the P1BBIO word (35H) in the register file. The latch for this port is located in address 71H of data memory BANK1 or BANK3. $P1B_3$/TMIN can also be used as the external timer input. Interrupts can be generated at 1/5 or 1/6 the frequency input to this pin. Normally the commercial power supply frequency is input to this pin and used as the basic clock for the clock.	CMOS push-pull (I/O)

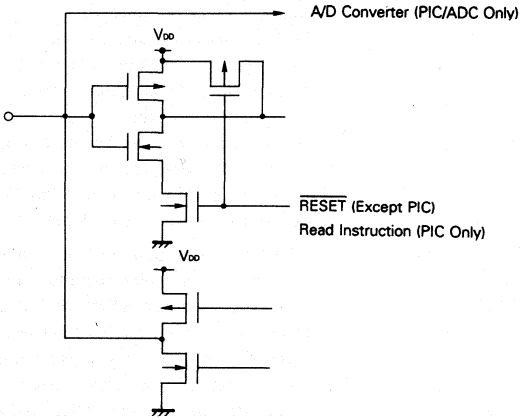
PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
27 28 29	PWM_2 PWM_1 PWM_0	D/A converter	VDP (Variable Duty Port) or 1-bit output ports. The VDP function outputs consecutive 15.625 kHz pulses, and the duty of these pulses can be varied by the program in 64 steps.	N-ch open-drain
30	PWM_{RMP}	Station selection D/A converter output	Voltage synthesizer 14-bit D/A converter output or 1-bit output port. The D/A converter outputs pulses combining 9-bit PWM and 5-bit RMP (Rate Multiplier). Therefore, D/A conversion can be performed by external connection of a simple CR filter. Outputs a low-level signal after power-on reset or when clock is stopped.	N-ch open-drain
31 32 33	RED GREEN BLUE	Character signal outputs	Output pins for character data corresponding to R, G, B. Active-high output.	CMOS push-pull
34	BLANK	Blanking signal output	Output pin for blanking signal cutting video signals. Active-high output.	CMOS push-pull
35	$\overline{H_{SYNC}}$	Horizontal synchronization signal input	Input pin for horizontal synchronization signal for IDC. Use active-low input.	Input
36	$\overline{V_{SYNC}}$	Vertical synchronization signal input	Input pin for vertical synchronization signal for IDC. Use active-low input. This pin can be used to effect interrupts.	Input
37 38 39 40	$P0B_3$/ HSCNT $P0B_2$ $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the POBBIO word (36H) in the register file. The latch for this port is located in address 71H of data memory BANK0 or BANK2. The $P0B_0$/SI pin can also be used as the serial interface (serial I/O mode) data input pin. The $P0B_3$/HSCNT pin can also be used as the horizontal synchronization signal counter input pin, in which case self-bias ($V_{DD}/2$) is applied to the HSCNT pin. Port 0B is set to input mode after a power-on reset, when the clock is stopped, or after a CE reset.	CMOS push-pull (I/O) But note that HSCNT is self-bias in input mode.

PIN No.	SIGNAL	PIN NAME	DESCRIPTION	OUTPUT TYPE
41 42 43 44	$P0A_3$/SP $P0A_2$/SCK $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input/output port. These port pins can be specified as input/output bit by bit. Input/output setting is performed by the POABIO word (37H) in the register file. The latch for this port is located in address 70H of data memory BANK0 or BANK2. The $P0A_3$/S0 pin can also be used as the serial interface (serial I/O mode) data output pin, and the $P0A_2$/SCK pin can be used as a shift clock input/output pin. The $P0A_0$/SDA pin can be used as a serial interface (2-wire mode and serial I/O mode) data input/output pin, and the $P0A_1$/SCL pin can be used as a shift clock input/output pin.	$P0A_3$/S0 $P0A_2$/SCK CMOS push-pull (I/O) $P0A_1$/SCL $P0A_0$/SDA N-ch open-drain (I/O)
45 46 47	$P1C_3$/ADC_3 $P1C_2$/ADC_2 $P1C_1$/ADC_1	Port 1C	3-bit input/output port or A/D converter input pins. Input/output setting is performed as a 3-bit unit, and is specified by the P1CGI0 bit (bit #0 or 27H) in the register file. When used as A/D converter pins, input must always be specified. The latch for this port is located in address 72H of data memory BANK1 or BANK3. Port 1C is set to input mode after a power-on reset, when the clock stopped, or after a CE reset.	CMOS push-pull (I/O)
48	ADC_0	A/D converter input	A program-driven successive approximation 4-bit A/D converter is incorporated. The A/D converter reference voltage is V_{DD}.	Input

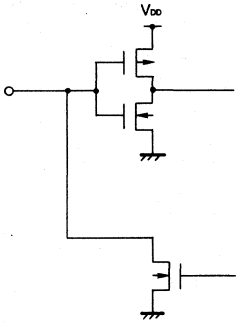
1.2 PIN EQUIVALENCE CIRCUITS

P0A ($P0A_3$/SO, $P0A_2$/$\overline{SCK}$)
P0B ($P0B_2$, $P0B_1$, $P0B_0$/SI)
P1B ($P1B_2$, $P1B_1$, $P1B_0$)
P1C ($P1C_3$/ADC_3, $P1C_2$/ADC_2, $P1C_1$/ADC_1)

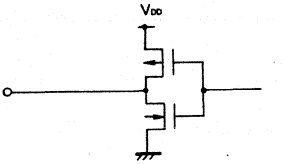
(Input/output)



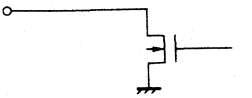
P0A ($P0A_1$/SCL, $P0A_0$/SDA): (Input/output)



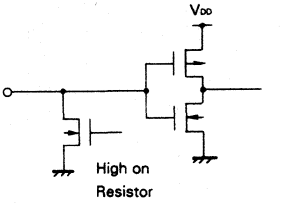
P0C (P0C3, P0C2, P0C1, P0C0)
P1D (P1D3, P1D2, P1D1, P1D0)
RED, GREEN, BLUE, BLANK
} (output)



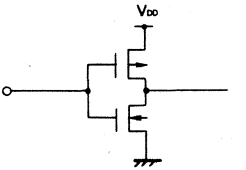
PWM (PWM2, PWM1, PWM0, PWMRMP)
P1A (P1A3, P1A2, P1A1, P1A0)
} (output)



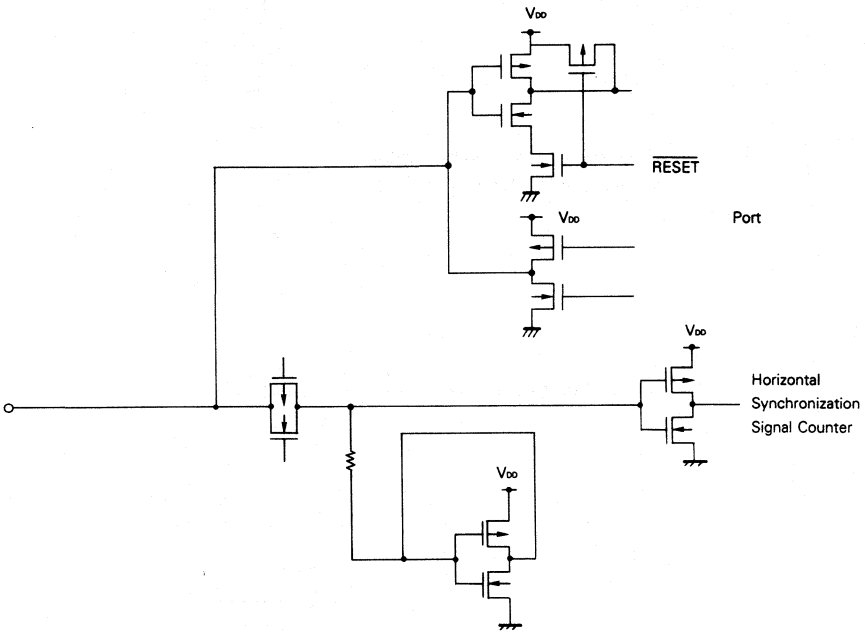
P0D (P0D3/ADC7, P0D2/ADC6, P0D1/ADC5, P0D0/ADC4): (Input)



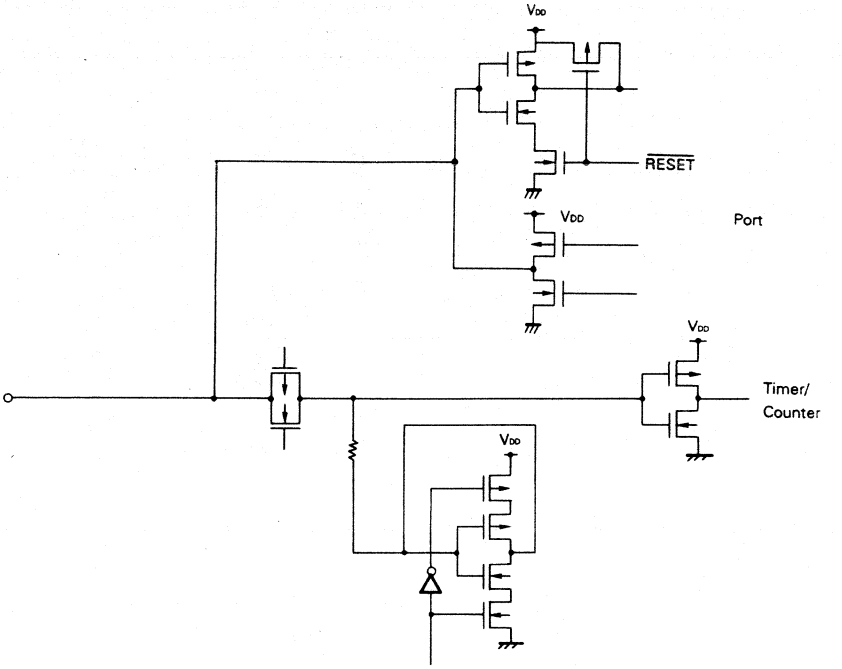
ADC0: (Input)



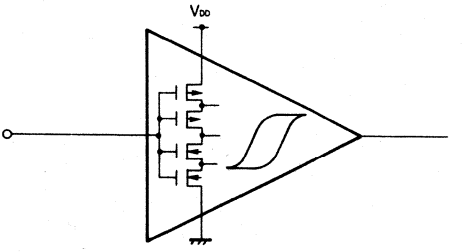
P0B3/HSCNT: (Input/output)



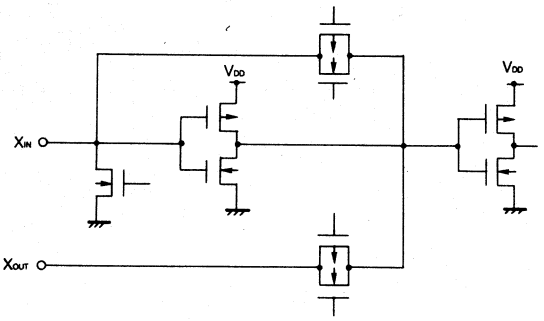
P1B3/TMIN: (Input/output)



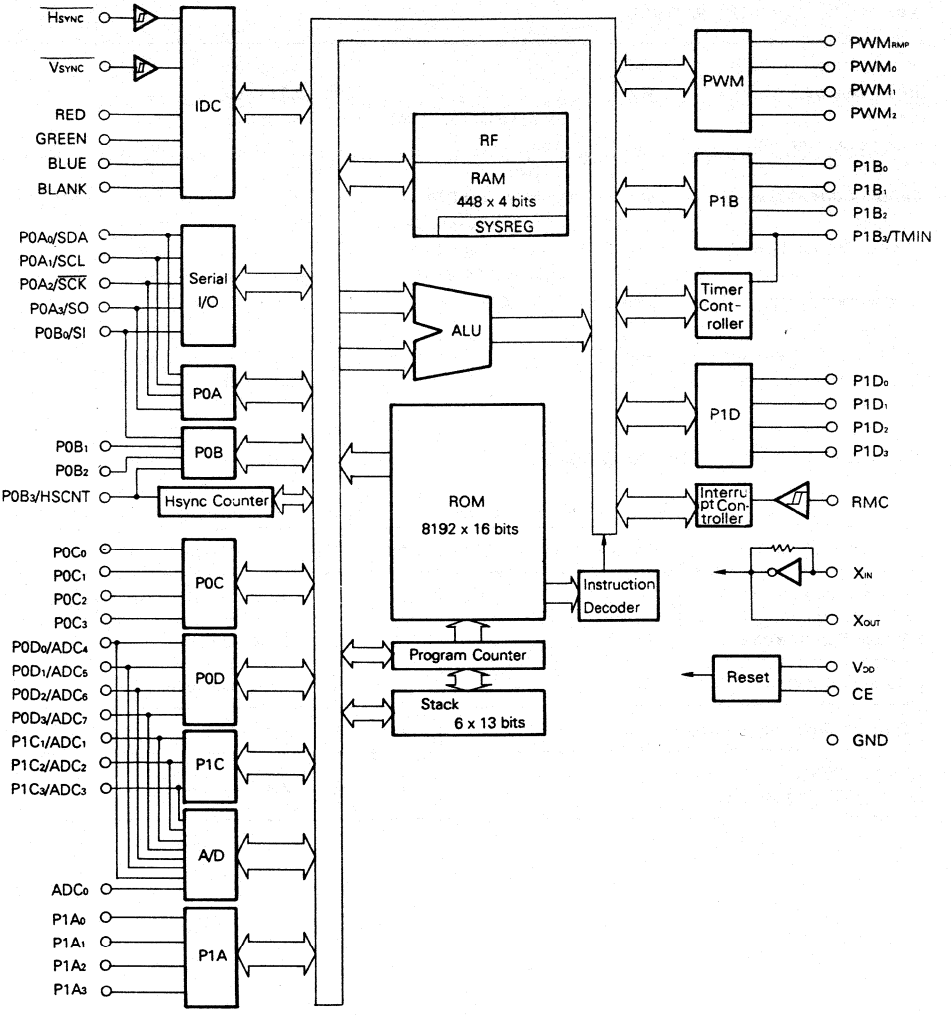
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, RMC, CE: (Schmitt triggered inputs)



X_{IN}: (Input)
X_{OUT}: (Output)



2. BLOCK DIAGRAM



24. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}		−0.3 to +6.0	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Output Voltage	V_O	Except P1A and PWM	−0.3 to V_{DD}	V
Output Current High	I_{OH}	1 pin	−12	mA
		All pins	−20	mA
Output Current Low	I_{OL1}	1 pin (except P1A)	12	mA
		All pins (except P1A)	20	mA
Output Current Low	I_{OL2}	1 pin (P1A only)	17	mA
		All pins (P1A only)	60	mA
Output Withstand Voltage	V_{BDS}	P1A, PWM	13	V
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All functions in operation
Power Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only IDC stop
Data Hold Voltage	V_{DR}	2.2		5.5	V	Clock oscillation stop
Output Withstand Voltage	V_{BDS}			12.5	V	P1A, PWM
Power Supply Voltage Rising Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Current	I_{DD1}		7	15	mA	CPU operation, IDC operation V_{DD} = 5.5 V
Power Supply Current	I_{DD2}		3.5	15	mA	CPU operation, IDC stop V_{DD} = 5.5 V
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Input Voltage High	V_{IH2}	0.8 V_{DD}		V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C
Input Voltage Low	V_{IL2}	0		0.2 V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Output Current High	I_{OH}	-1	-2		mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OH} = V_{DD} −1 V
Output Current Low	I_{OL1}	2	3		mA	P0A, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OL} = 1 V
Output Current Low	I_{OL2}	15	20		mA	P1A V_{OL} = 1 V
Output Current Low	I_{OL3}	1	2		mA	PWM V_{OL} = 1 V
Input Current High	I_{IH}		50		μA	P0D, when pulled down V_{IH} = V_{DD}
Data Hold Current	I_{DR}			10	μA	Clock oscillation stop T_a = 25 °C, V_{DD} = 5.5 V
Output Leakage	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, PWM V_{OH} = 5 V

AC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

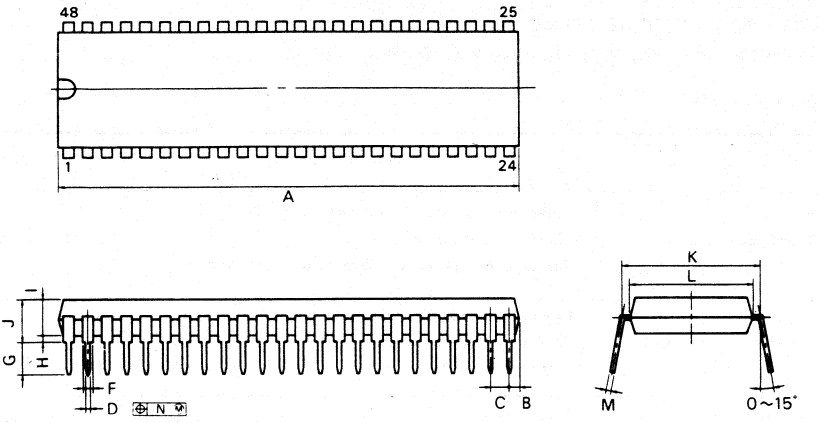
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Frequency	f_{TMIN}	50		60	Hz	P1B3/TMIN
Input Frequency	f_{HS}	10		20	kHz	P0B3/HSCNT
IDC Jitter	IDCG		3	4	ns	V_{DD} = 4.5 to 5.5 V

A/D CONVERTER CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
A/D conversion absolute accuracy		±1/2		±1	LSB	
A/D input impedance		1			MΩ	

PACKAGE DIMENSION

48PIN PLASTIC SHRINK DIP (600 mil)



P48C-70-600B

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	44.46 MAX.	1.751 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}_{-}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}_{-}$	$0.126^{+0.012}_{-}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17051CU

Soldering Process	Soldering conditions	Symbol
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300°C or below, Flow time : 10 seconds or below, Exposure limit* : None	

* : Exposure limit before soldering after dry-pack package is opened.
Storage condition: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

μPD17051CU

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below

SINGLE-CHIP MICROCOMPUTER
BUILT-IN IMAGE DISPLAY CONTROLLER FOR VOLTAGE SYNTHESIZER

The μPD17052 is a 4-bit single-chip microcomputer with a built-in display controller and 14-bit D/A converter for a digital tuning system designed for use in a voltage synthesizer TV set.

The image display controller (IDC) has a variety of image display functions. It is capable of displaying figures as well as characters. All fonts are user-programmable and can be specified as desired. Debugging can be done by actually outputting this data from the start of program development.

The microcomputer is also provided with a horizontal synchronization signal counter for detecting broadcasting stations, and a serial interface for communication with peripheral devices. Also, a 4-bit A/D converter and a 6-bit D/A converter (PWM output) are provided.

The CPU employs the μPD17000 architecture capable of handling the data memory directly without using an accumulator. This ensures highly efficient programming. All instructions comprise a single word with a length of 16 bits.

We also provide an IE-17K (In-Circuit Emulator) and an assembler as easy-to-use μPD17052 system development tools.

FEATURES

- 4-bit microcomputer for digital tuning system
- Built-in 14-bit D/A voltage synthesizer
- Program memory (ROM) : 16K bytes (16 bits x 8,192 steps)
- Data memory (RAM) : 4 bits x 448 words
- Stack levels : 6
- Easy-to-understand instructions (35)
- Decimal operations available
- Instruction execution time : 2 μs (8 MHz oscillator connected)
- Built-in IDC (Image Display Controller) (User programmable)
  - Number of display characters : Max. 99 characters per screen
  - Display position : 14 lines x 19 columns
  - Character set : 128 characters (64 different characters can be displayed in one screen simultaneously.)
  - Colors : 8 colors
  - Character size : 4 sizes can be set in vertical and/or horizontal directions (14, 28, 42, 56H)
- Built-in 8-bit serial interface (One system with two channels: three-wire and two-wire types)
- Built-in D/A converter : 6 bits x 4 (PWM output)
- Built-in A/D converter : 4 bits x 8
- Built-in horizontal synchronization signal counter
- Built-in commercial power frequency counter
- Built-in power failure detection circuit and Power On reset circuit
- Interrupt input for remote control signals (with noise canceller)
- Wealth of I/O ports
  - Input/output ports : 20
  - Input ports : 4
  - Output ports : 20
- 5 V ±10 %
- Use of low power-consumption CMOS
- 64-pin plastic shrink DIP (750 mil)

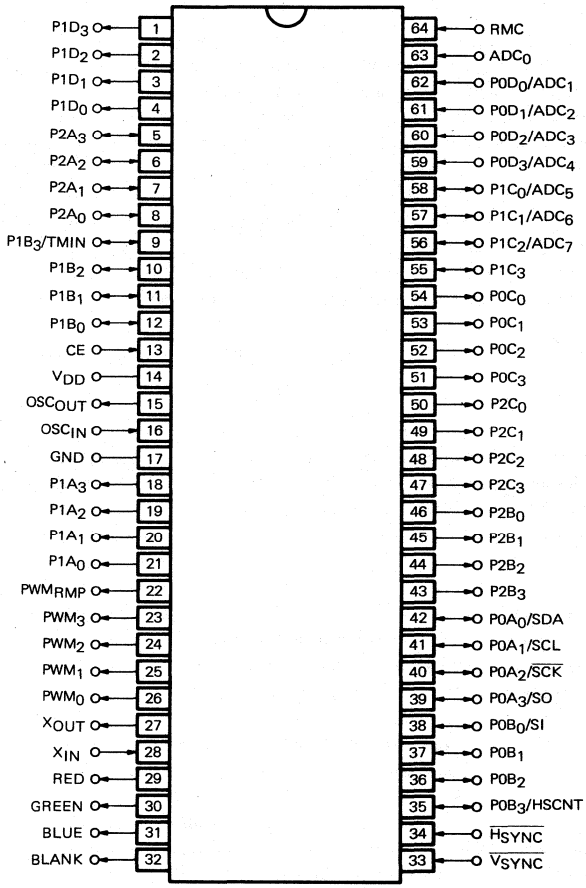
Notes on Serial interface: The 2-wire mode corresponds to the I2C-Bus specification from Philips. In case of using this interface mode note the following:

Duties when using I2C bus system

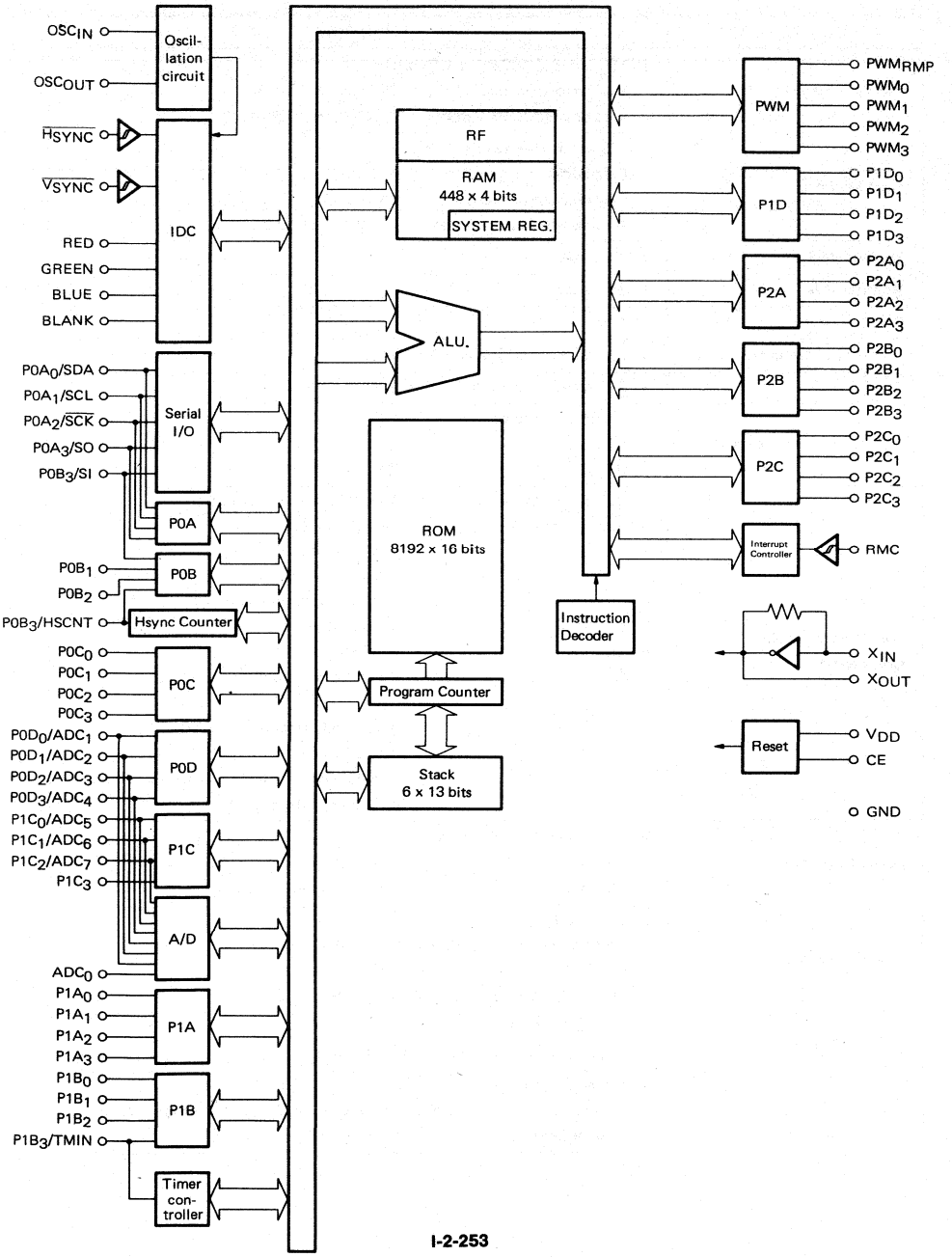
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



List of μPD17052 functions

CHARACTERISTIC	FUNCTION
Program Memory	• 16K bytes (8,192 steps x 16 bits) Table reference area : 256 steps x 16 bits Area serving also as CROM : 2,048 steps x 16bits
Data Memory	• 448 words (448 words x 4 bits) Data buffer : 4 words, General-purpose register : 16 words Area also serving as VRAM : 224 words x 4 bits
System Register	• 12 words
Register File	• 24 words
Port Register	• 11 words
Instruction Execution Time	• 2 μs, using an 8 MHz ceramic oscillator
Stack Levels	• 6 levels (stack operation available)
General-Purpose-Ports	• Input/output ports : 20 • Input ports : 4 • Output ports : 20
IDC (Image Display Controller)	• Number of display character: Max. 99 characters per screen • Display position : 14 lines x 19 columns • Character set : 128 characters (user programmable) (64 different characters can be displayed in one screen simultaneously.) • Character type : 10 x 15 dots • Colors : 8 colors • Character size : 4 sizes in vertical direction (14, 28, 42, 56H) 4 sizes in horizontal direction (2.5, 5.0, 7.5, 10.0 μs) Can be specified in vertical and horizontal directions independently.
Serial Interface	• One system (two channels) 8-bit 3-wire type : one channel 8-bit 2-wire type : one channel
D/A Converter	• 14 bits x 1 (PWM output, withstanding voltage : Max. 12.5 V) • 6 bits x 4 (PWM output, withstanding voltage : Max. 12.5 V)
A/D Converter	• 4 bits x 8 (sequential comparison by means of software)
Interruption	• 4 channels (maskable interrupt) External interrupt : 3 channels (RMC pin, $\overline{V_{SYNC}}$ pin, serial interface) Internal interrupt : One channel (timer)

CHARACTERISTIC	FUNCTION
Timer	• Two system Internal timer : 5, 20, 100 ms External timer : 1/5 and 1/6 of frequency input to PIB_3/TMIN pin
Reset	• Power ON reset (When the power is input) • Resetting by CE pin (CE pin Low → High) • Power failure detection
Power Supply Voltage	• 5 V ±10 %
Package	• 64-pin plastic shrink DIP (750 mil)

PIN DESCRIPTION

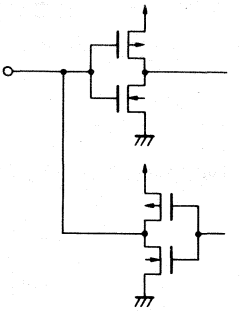
PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
1 to 4	$P1D_3$ to $P1D_0$	Port 1D	4-bit output ports. The latch of port 1D is assigned to address 73H of Bank 1 of the data memory (RAM). The output state is undefined at the time when the power (V_{DD}) is applied initially.	CMOS push-pull
5 to 8	$P2A_3$ to $P2A_0$	Port 2A	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting of input/output is performed by using the P1BBIO word (35H) on the register file. The latch of the port is assigned to address 70H of Bank 2 of the data memory (RAM).	CMOS push-pull (I/O)
9 10 11 12	$P1B_3$/TMIN $P1B_2$ $P1B_1$ $P1B_0$	Port 1B	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting of input/output is performed by using the P1BBIO word (35H) on the register file. The latch of the port is assigned to address 71H of Bank 1 of the data memory (RAM). $P1B_3$/TMIN can also be used as input to an external timer. It is possible to make an interrupt with a frequency equivalent to one-fifth or one-sixth the frequency input to this pin. Normally, the commercial power supply frequency is input to this pin for use as the reference clock.	CMOS push-pull (I/O)
13	CE	Chip enable	Device selection signal input pin. Set the pin at the high level to put the device in normal operation. Set the pin at the low level if the device is not used. When the pin is at the low level, executing the STOP instruction causes the clock oscillation to stop, making backup with a low current possible. The STOP instruction is effective only when the CE pin is at the low level. The instruction is in effect the same as the NOP instruction when the CE pin is at the high level. The pin also serves as a reset pin. Changing the CE pin from the low level to the high level causes the device to be reset and the program to start from address 0. If the device is reset, the bank is made 0 and the I/O ports are put in the input mode.	Input
14	V_{DD}	Power	Device power pin. Supply a voltage of 5 V ±10 % to when activating all functions. If the IDC is not used, apply a voltage of 4 to 5.5 V. To retain the data of RAM (when the clock oscillation is stopped), the voltage may be dropped to 2.5 V. Since the μPD17052 has a built-in power On reset circuit, if the voltage changes from 0 to 4.0 V, the system is reset and the program starts from address 0. To operate the Power On reset circuit properly, it is necessary to limit the rise time from 0 to 4.0 V to 550 ms or less.	–
15 16	OSC_{OUT} OSC_{IN}	LC oscillation	LC oscillation circuit pin for the IDC. Oscillation is made at 4 MHz.	CMOS push-pull (OSC_{OUT}) INPUT (OSC_{IN})
17	GND	Ground	Device grounding pin.	–

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
18 to 21	$P1A_3$ to $P1A_0$	Port 1A	4-bit output port. The latch of the port is assigned to address 70H of Bank 1 of the data memory (RAM). N-ch open drain type. (medium withstanding voltage, large current)	N-ch open drain
22	PWM_{RMP}	Tuning D/A converter output	Port for the output of the 14-bit D/A (Digital-to-Analog) converter for a voltage synthesizer, or port for the output of one bit. The D/A converter outputs pulses made up of a combination of 9-bit PWM (Pulse Width Modulation) and 5-bit RMP (Rate Multiplier). D/A conversion is therefore possible by connecting a simple external CR filter. The output is at the low level when Power On is reset or when the clock is stopped.	N-ch open drain
23 to 26	PWM_3 to PWM_0	D/A converter	VDP (Variable Duty Port), or port for the output one bit. The VDP function is to output pulses of a frequency of 15,625 kHz continuously. The duty of the pulse can be made variable in 64 steps by means of a program.	N-ch open drain
27 28	X_{OUT} X_{IN}	Oscillator	CPU oscillation circuit pin. Used to connect a ceramic oscillator or a crystal oscillator. Use an 8 MHz oscillator.	CMOS push-pull (XO) Input (XI)
29 30 31	RED GREEN BLUE	Character signal output	Pins to output character data corresponding to R, G and B. Output is in active High.	CMOS push-pull
32	BLANK	Blanking signal output	Pin to output blanking signals to cut image signals. Output is in active High.	CMOS push-pull
33	$\overline{V_{SYNC}}$	Vertical synchronization signal input	Pin to input vertical synchronization signals for the IDC. Input in active Low. It is possible to make an interrupt with this signal.	Input
34	$\overline{H_{SYNC}}$	Horizontal synchronization signal input	Pin to input horizontal synchronization signals for the IDC. Input in active Low.	Input
35 36 37 38	$P0B_3$/HSCNT $P0B_2$ $P0B_1$ $P0B_0$/SI	Port 0B	4-bit input/output ports. For these ports, it is possible to specify input/output on a bit by bit basis. The setting is made with the P0BBIO word (36H) on the register file. The latch of the port is assigned to address 71H of Bank 0 of the data memory (RAM). The $P0B_0$/SI pin can also serve as a data input pin of a serial interface (μCOM standard mode). The $P0B_3$/HSCNT pin can also serve as an input pin of the horizontal synchronization signal counter. This pin is always self-biased ($V_{DD}/2$). Port 0B is for input when the power (V_{DD}) is input initially, the clock stops, or resetting is done by the CE pin (Low → High).	CMOS push-pull (I/O), provided $P0B_3$/HSCNT is self-biased at the time of input.
39 40 41 42	$P0A_3$/SO $P0A_2/\overline{SCK}$ $P0A_1$/SCL $P0A_0$/SDA	Port 0A	4-bit input/output ports. These ports can be specified for input/output on a bit-by-bit basis. The setting is made with the P0ABIO word (37H) on the register file. The latch of the port is assigned to address 70H of Bank 0 of the data memory. The $P0A_3$ pin can be used as a data output pin of a serial interface (μCMOS standard mode) and the $P0A_2$/SCK pin as a shift clock input/output pin. The $P0A_0$/SDA pin can be used as a data input/output pin of a serial interface (two-wire mode and μCOM standard mode), and the $P0A_1$/SCL pin as a shift clock input/output pin.	CMOS push-pull

PIN No.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
43 to 46	$P2B_3$ to $P2B_0$	Port 2B	4-bit output port. The latch of the port is assigned to address 71H of Bank 2 of the data memory (RAM). N-ch open drain (medium withstanding voltage).	N-ch open drain
47 to 50	$P2C_3$ to $P2C_0$	Port 2C	4-bit output port. The latch of the port is assigned to address 72 of Bank 2 of the data memory (RAM). N-ch open drain. (medium withstanding voltage)	N-ch open drain
51 to 54	$P0C_3$ to $P0C_0$	Port 0C	4-bit output port. The latch of Port 0C is assigned to address 72H of Bank 0 of the data memory (RAM). The output state is indefinite when the power (V_{DD}) is input initially.	CMOS push-pull
55 56 57 58	$P1C_3$ $P1C_2/ADC_7$ $P1C_1/ADC_6$ $P1C_0/ADC_5$	Port 1C	4-bit input/output port or A/D converter pin. The setting of input/output is made every 4 bits. The P1CGIO bit (bit #0 of address 27H) on the register file is used for input/output specification. It is necessary to specify input without fail when used as an A/D converter. The latch of the port is assigned to address 72 of Bank 1 of the data memory (RAM). Port 1C is for input when the power (V_{DD}) is applied for the first time, the clock is stopped or resetting is made with the CE pin (Low → High).	CMOS push-pull (I/O)
59 60 61 62	$P0D_3/ADC_4$ $P0D_2/ADC_3$ $P0D_1/ADC_2$ $P0D_0/ADC_1$	Port 0D	4-bit input port. This port can also be used as an A/D converter. When used as a port, a pull-down resistance (100 kΩ TYP.) is attached. The latch of Port 0D is assigned to address 73H of the data memory (RAM).	Input (with pull-down resistance)
63	ADC_0	A/D converter input	A/D (Analog to Digital) converter input pin. The converter is a 4-bit built-in A/D converter employing programmed sequential comparison. The reference voltage of the A/D converter is V_{DD}.	Input
64	RMC	Interrupt signal input	Interrupt input pin with a noise canceller. Signals with a high level of noise, such as remote control signals, can be programmed easily by using this pin. It is possible to specify by means of a program whether an interrupt is made at the rise or at the fall of an input signal to this pin. Specifically, an interrupt is made at the rise or at the fall of the signal depending on whether the IEDG1 flag is reset or set, respectively. At the time of resetting (CE pin: Low → High), the IEDG1 flag is reset and an interrupt is made at the edge of the rise.	Input

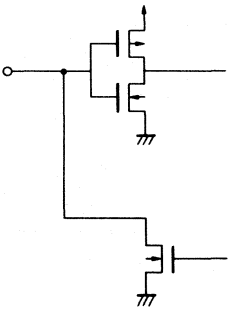
PIN EQUIVALENT CIRCUITS

P0A ($P0A_3$/SO, $P0A_2$/$\overline{SCK}$)
P0B ($P0B_2$, $P0B_1$, $P0B_0$/SI)
P1B ($P1B_2$, $P1B_1$, $P1B_0$)
P1C ($P1C_3$, $P1C_2$/ADC_7, $P1C_1$/ADC_6, $P1C_0$/ADC_5)
P2A ($P2A_3$, $P2A_2$, $P2A_1$, $P2A_0$)



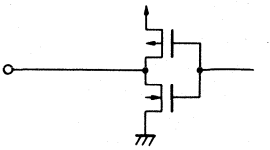
(IN/OUT)

P0A ($P0A_1$/SCL, $P0A_0$/SDA)



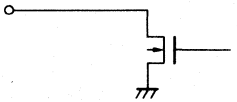
(IN/OUT)

P0C ($P0C_3$, $P0C_2$, $P0C_1$, $P0C_0$)
P1D ($P1D_3$, $P1D_2$, $P1D_1$, $P1D_0$)
RED, GREEN, BLUE, BLANK



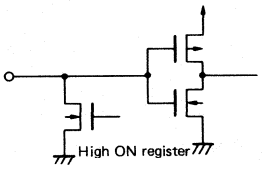
(OUT)

PWM (PWM_3, PWM_2, PWM_1, PWM_0, PWM_{RMP})
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
P2B ($P2B_3$, $P2B_2$, $P2B_1$, $P2B_0$)
P2C ($P2C_3$, $P2C_2$, $P2C_1$, $P2C_0$)



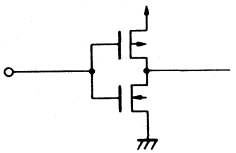
(OUT)

P0D ($P0D_3/ADC_4$, $P0D_2/ADC_3$, $P0D_1/ADC_2$, $P0D_0/ADC_1$)



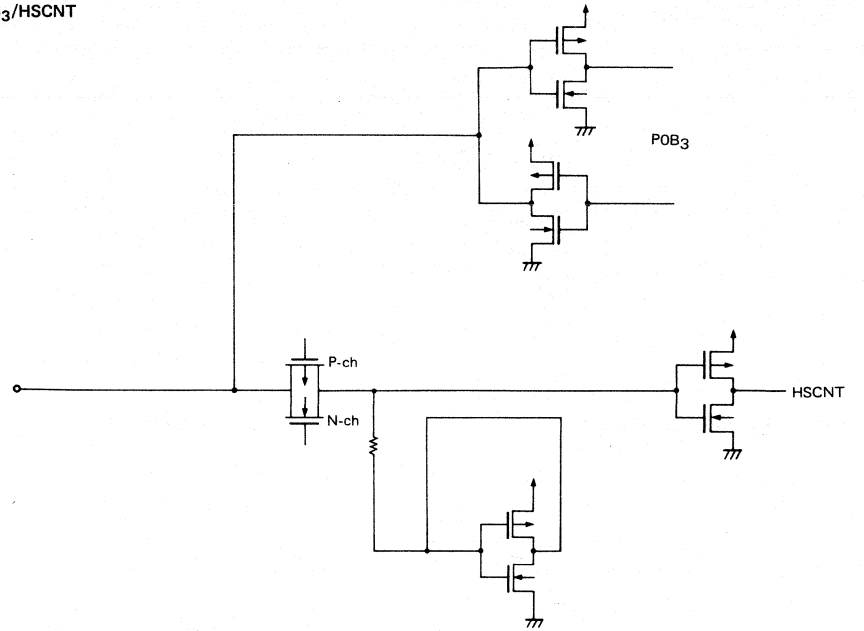
(IN)

ADC_0

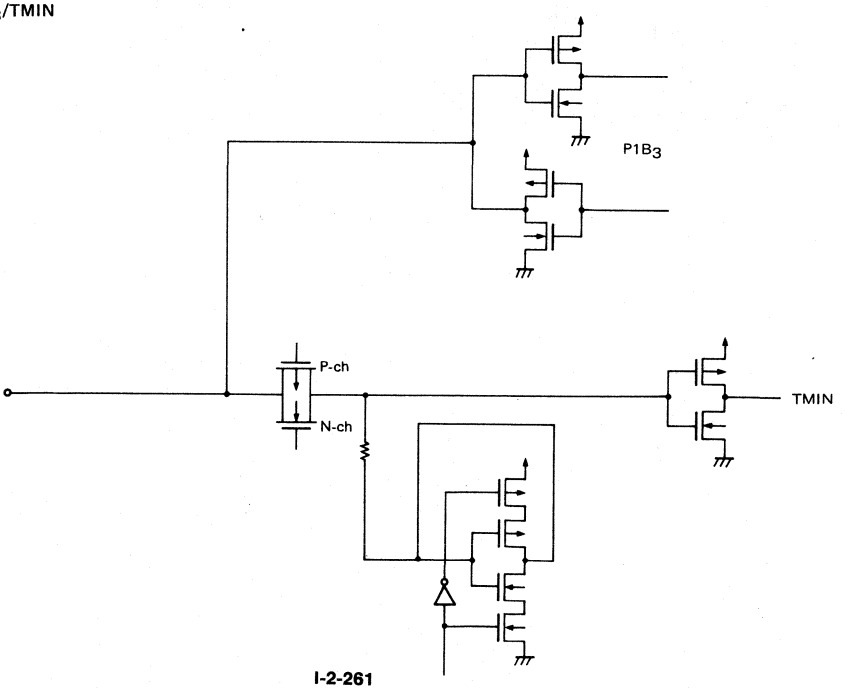


(IN)

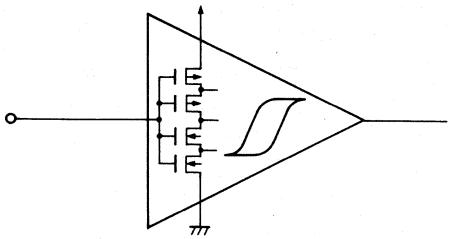
$P0B_3$/HSCNT



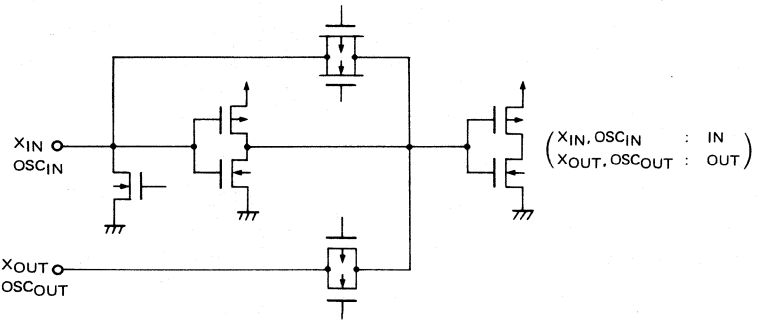
$P1B_3$/TMIN



$\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, RMC, CE



X_{OUT}, X_{IN}, OSC_{OUT}, OSC_{IN}



ELECTRIC CHARACTERISTICS (PROVISIONAL)

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}	−0.3 to +6.0	V
Input Voltage	V_I	−0.3 to V_{DD}	V
Output Voltage	V_O	−0.3 to V_{DD}	V
Output Absorption Current	I_O	10	mA
Withstanding Output Voltage	V_{BDS}	13 (P1A, P2B, P2C, PWM)	V
Operating Temperature	T_a	−20 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All function activated
Power Supply Voltage	V_{DD2}	4.0	5.0	5.5	V	Only IDC stopped
Data Storing Voltage	V_{DR}	2.5		5.5	V	Clock oscillation stopped
Withstanding Output Voltage	V_{BDS}			12.5	V	P1A, P2B, P2C, PWM
Power Supply Voltage Rise Time	t_{rise}			500	ms	V_{DD}: 0 → 4.0 V

DC CHARACTERISTICS (T_a = –20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

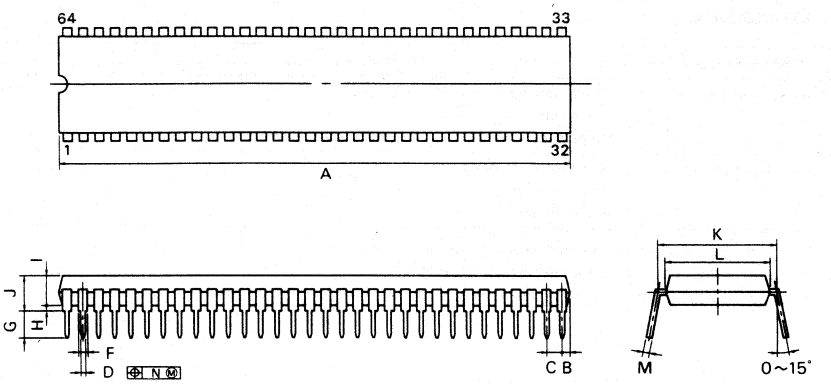
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Current	I_{DD1}		7	15	mA	CPU in operation, IDC in operation V_{DD}=5.5 V
Power Supply Current	I_{DD2}		3.5	15	mA	CPU in operation, IDC stopped V_{DD}=5.5 V
High Level Input Voltage	V_{IH1}	0.7 V_{DD}			V	P0A, P0B, P0D, P1B, P1C, P2A
High Level Input Voltage	V_{IH2}	0.8 V_{DD}			V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Low Level Input Voltage	V_{IL1}			0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C, P2A
Low Level Input Voltage	V_{IL2}			0.2 V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
High Level Output Current	I_{OH}		–2	–1	mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OH}=V_{DD}–1 V
Low Level Output Current	I_{OL1}	2	3		mA	P0A, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OL}=1 V
Low Level Output Current	I_{OL2}	15	20		mA	P1A V_{OL}=1 V
Low Level Output Current	I_{OL3}	1	2		mA	PWM, P2B, P2C V_{OL}=1 V
High Level Input Current	I_{IH}		50		μA	P0D, pull-down time
Data Storing Current	I_{DR}			10	μA	Clock oscillation stopped T_a=25 °C, V_{DD}=5.5 V
Output Leak	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, P2B, P2C, PWM V_{OH}=5 V

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Frequency	f_{TMR}	50		60	Hz	$P1B_3$/TMIN
Input Frequency	f_{HS}	10		20	kHz	$P0B_3$/HSCNT

PACKAGE DIMENSION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{-0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{-0.10}_{-0.05}$	$0.010^{-0.004}_{-0.003}$
N	0.17	0.007

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17052CW-XXX

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below, Exposure limit* : None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

BUILT-IN IMAGE DISPLAY CONTROLLER

The μPD17053 is a 4 bits CMOS microcontroller incorporating Image Display Controller (IDC) and 14 bits D/A converter into one chip for digital tuning of voltage synthesizer system of TV.

Image Display Controller has various display function showing not only letters but also drawings.

Fonts of IDC are selected by user's program and effective debugging can be realized by actual indications from the beginning of software development.

In addition, Hsync. counter for station detection and serial interface for communication with other peripheral devices are incorporated, also 4 bits A/D converter and 6 bits D/A converter (PWM output) are incorporated.

CPU applies μPD17000 architecture which operates data memory directly without accumulater, and it realizes effective programming.

All instruction consist of 16 bits one word.

As system development support tool of μPD17053, IE-17K (In Circuit Emulator) and assembler are prepared.

FEATURES

- 4 bits microcontroller for digital tuning system
- built-in 14 bits D/A converter
- single power supply (5 V ±10 %)
- CMOS with low power consumption
- program memory (ROM):
  24K byte (16 bits x 12,288 steps)
- data memory (RAM): 4 bits x 672 words
- stack level: 7 levels
- easy to understand instruction set with 36 types
- capable of decimal arithmetic
- instruction execution time:
  2 μs (with 8 MHz ceramic resonator connected)
- IDC (Image Display Controller) built-in
  (user programmable)
  - number of display character:
    199 characters (max. in one screen)
  - display location: 14 lines x 19 columns
  - number of character types: 256 types
  - character format:
    10 x 15 dots (capable of fringe function)
  - character color: 8 colors
  - character size:
    4 types of setting is available independently both for line and column, (14, 28, 42, 56H)
- built-in 8 bits serial interface:
  (1 system 2 channel: 3 wire and 2 wire system)
- built-in D/A converter: 6 bits x 4 (PWM output)
- built-in A/D converter: 4 bits x 8
- built-in H.sync. signal counter
- built-in commercial power supply freq. counter
- built-in blackout detection circuit and power-on-reset circuit.
- interrupt input for remote control signal (with noise canceler)
- plentiful I/O ports: input output port : 20
  input port : 4
  output port : 20
- 64 pin plastic shrink DIP (750 mil)

Notes on Serial interface:

The 2-wire mode corresponds to the I2C-Bus specification from Philips.

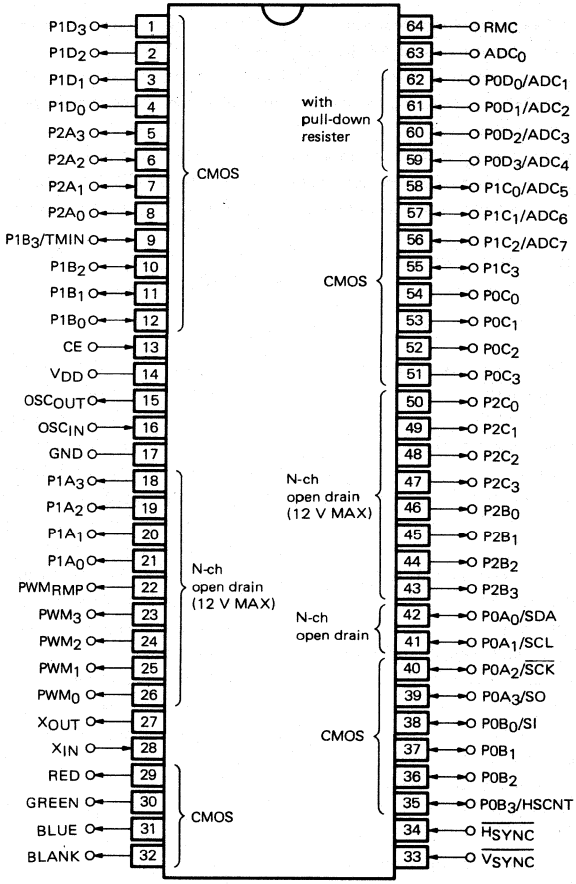
In case of using this interface mode note the following:

Duties when using I2C bus system

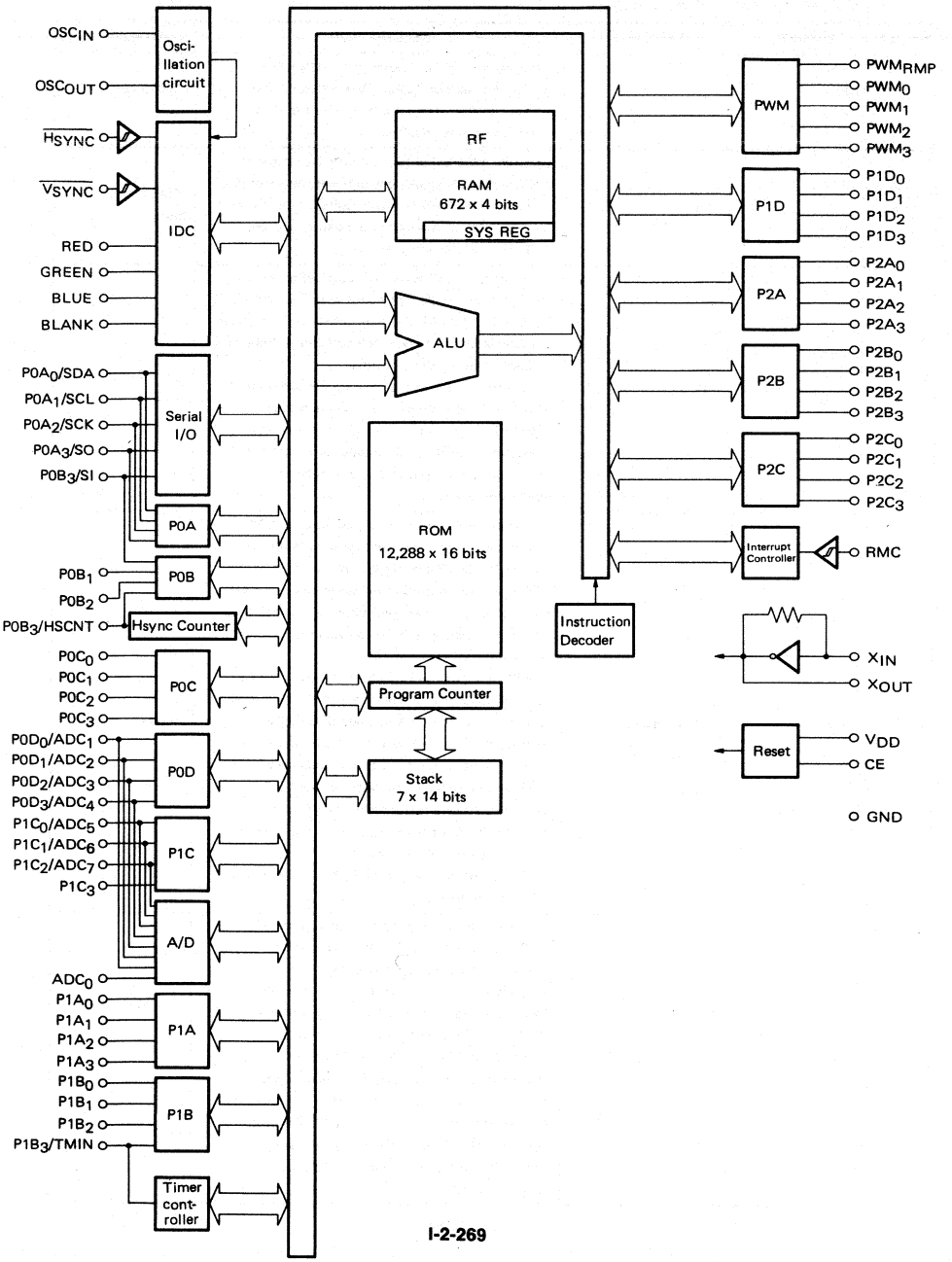
Purchase of NEC's I2C bus system hardware components conveys a license under the Philips I2C patents rights to use this components in an I2C system, provided that the system conforms the I2C standard specifications as defined by Philips.

Consequently for all ROM based components with I2C hardware circuits the user is kindly requested to notify the use of the I2C bus interface at the ROM code verification stage.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. PIN FUNCTION

1.1 DESCRIPTION OF PIN FUNCTIONS

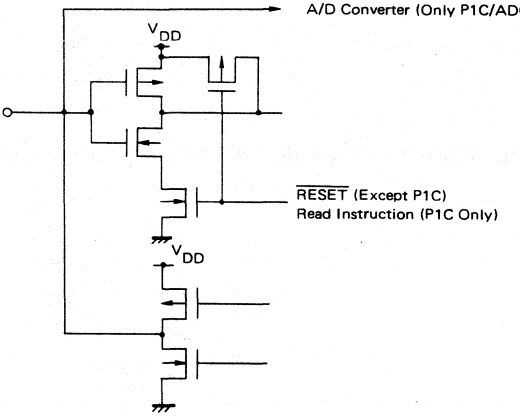
PIN NO.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
1 to 4	$P1D_3$ to $P1D_0$	Port 1D	These are 4-bit output ports. Port 1D's latch is allocated in address 73H of BANK1 of the data memory (RAM). The output state at the time of power-on reset is undefined.	CMOS push-pull
5 to 8	$P2A_3$ to $P2A_0$	Port 2A	These are 4-bit I/O ports. It is possible to specify input/output for these ports bit-wise. Input/output is set with the P2ABIO words (34H) on the register file. The latch of this port is located in address 70H of BANK2 of the data memory.	CMOS push-pull
9 10 11 12	$P1B_3$/TMIN $P1B_2$ $P1B_1$ $P1B_0$	Port 1B	These are 4-bit I/O ports. It is possible to specify input/output for these ports bit-wise. Input/output is set with the P1BBIO words (35H) on the register file. The latch of this port is located in address 71H of BANK1 of the data memory. P1B/TMIN can be used as an external timer input as well. It is possible to interrupt the frequency that is input to this pin with 1/5 or 1/6 of the frequency. Normally, the frequency of the commercial power is input to this pin to be used as a reference clock.	CMOS push-pull (I/O)
13	CE	Chip enable	This is the device selection signal input pin. The device is set to the high level for a normal operation and to the low level when not using it. If the STOP instruction is executed when this pin is at the low level, the clock oscillation is stopped thus making the backup at a low power consumption possible. The STOP instruction is valid only when the CE pin is at the low level. When it is at the high level, it functions in the same manner as the NOP instruction. This pin plays the role of a reset pin as well. Therefore, if the CE pin is changed from the low level to high, the device is reset, thus restarting the program from address 0. If the device is reset, the bank becomes 0, thus placing the I/O port in the input mode. However, the low level from 188 μs and below is not accepted.	Input
14	V_{DD}	Power input	This is the device power pin. A voltage of 5 V± 10 % is supplied to make the device operate all the functions. A voltage between 4 to 5.5 V is supplied when IDC is not used. It is possible to lower the voltage to about 2.2 V when holding the RAM data (when the clock oscillation is stopped). As μPD17053 is incorporated with the power-on reset circuit, if this is changed from 0 to 4.0 V, the system is reset thus making the program operate from address 0. Restrict the start-up time for changing from 0 to 4.0 V within 500 ms to make the power-on reset circuit operate normally.	—

PIN NO.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
15 16	OSC_{OUT} OSC_{IN}	LC oscillation	These are the LC oscillation circuit pins for IDC. They are oscillated at 4 MHz.	
17	GND	Ground	This is the ground pin of the device.	—
18 to 21	$P1A_3$ to $P1A_0$	Port 1A	These are 4-bit output ports. The latch of this port is located in address 70H of BANK1 of the data memory. The format is N-ch open-drain (middle-voltage, high current).	N-ch open-drain
22	PWM_{RMP}	Channel select D/A converter output	This is the 14-bit D/A converter output or 1-bit output port for voltage synthesizer. The D/A converter outputs the pulse which has combined the 9-bit PWM and the 5-bit RMP (Rate Multiplier). Therefore, D/A conversion can be carried out by externally connecting a simple CR filter. The low level is output for power-on reset or clock stop.	N-ch open-drain
23 to 26	PWM_3 to PWM_0	D/A converter	These are the VDP (Variable Duty Port) or 1-bit output ports. The VDP function is to output the 15.625 kHz pulse continuously and is capable of varying the duty of this pulse in 64-step programs.	N-ch open-drain
27 28	X_{OUT} X_{IN}	Clock oscillation	These are connection pins of ceramic oscillators or crystal resonators. Ensure to use 8 MHz.	CMOS push-pull (XOUT), input (X_{IN})
29 30 31	RED GREEN BLUE	Character signal output	These are the output pins of the character data corresponding to R, G and B. Output is made at active high.	CMOS push-pull
32	BLANK	Blanking signal output	This is the output pin of the blanking signal to cut image signals. Output is made at active high.	CMOS push-pull
33	$\overline{V_{SYNC}}$	Vertical synchronous signal input	This is the input pin of the vertical synchronous signal for IDC. Ensure to make the input at active low. Interrupt can be applied with this signal.	Input
34	$\overline{H_{SYNC}}$	Horizontal synchronous signal input	This is the input pin of the horizontal synchronous signal for IDC. Ensure to make the input at active low.	Input
35 36 37 38	$P0B_3$/HSCNT $P0B_2$ $P0B_1$ $P0B_0$/$\overline{SI}$	Port 0B	These are 4-bit I/O ports. It is possible to specify input/output bit-wise for these ports. This setting is made with the P0BBIO words (36H) on the register file. The latch of this port is located in address 71H of BANK0 of the data memory. Pin P0B/SI can be used as the data input pin of the serial interface (serial I/O mode) as well. Pin P0B/HSCNT can be used as the input pin of the horizontal synchronous signal counter as well. At this time, the own bias ($V_{DD}/2$) is applied to the HSCNT pin. Port 0B is ready for input in power-on reset, clock stop and CE reset.	CMOS push-pull (I/O) However, the own bias is applied to $P0B_3$/HSCNT to make the input.

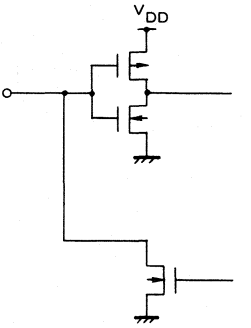
PIN NO.	SYMBOL	PIN NAME	DESCRIPTION	OUTPUT TYPE
39 40 41 42	$P0A_3$/SO $P0A_2$/$\overline{SCK}$ $P0A_1$/SCL $P0A_0$/SDA	Port 0A	These are 4-bit I/O ports. It is possible to specify input/output bit-wise for these ports. This setting is made with the P0ABIO words (37H) on the register file. The latch of this port is located in address 70H of BANK0 of the data memory. Pin $P0A_3$/SO can be used as the data output pin of the serial interface (serial I/O mode) and $P0A_2$/$\overline{SCK}$ can be used as the shift clock I/O pin. Pin P0A /SDA can be used as the data I/O pin of the serial interface (two-wire mode and serial I/O mode) and pin $P0A_1$/SCL can be used as the shift clock I/O pin.	$P0A_3$/SO $P0A_2$/$\overline{SCK}$ CMOS push-pull (I/O) $P0A_1$/SCL $P0A_0$/SDA N-ch open-drain (I/O)
43 to 46	$P2B_3$ to $P2B_0$	Port 2B	These are 4-bit output ports. The latch of this port is located in address 71H of BANK2 of the data memory. The format is N-ch open-drain (middle-voltage).	N-ch open-drain
47 to 50	$P2C_3$ to $P2C_0$	Port 2C	These are 4-bit output ports. The latch of this port is located in address 72H of BANK2 of the data memory. The format is N-ch open-drain (middle-voltage).	N-ch open-drain
51 to 54	$P0C_3$ to $P0C_0$	Port 0C	These are 4-bit output ports. The latch of this port is located in address 72H of BANK0 of the data memory. The output state is undefined in power-on reset.	CMOS push-pull
55 56 57 58	$P1C_3$ $P1C_2$/ADC_7 $P1C_1$/ADC_6 $P1C_0$/ADC_5	Port 1C	These are 4-bit I/O ports or A/D converter input pins. Input/output setting is carried every 4 bits, specifying with the P1CGIO bits (27H's #0 bit) on the register file. Ensure to specify when used as the A/D converter. The latch of this port is located in address 72H of BANK1 of the data memory. Port 1C is ready for input in power-on reset, clock stop and CE reset.	CMOS push-pull (I/O)
59 60 61 62	$P0D_3$/ADC_4 $P0D_2$/ADC_3 $P0D_1$/ADC_2 $P0D_0$/ADC_1	Port 0D	These are 4-bit input ports or A/D converter input pins. The pull-down resistor is installed (100 k TYP.) when these are used as ports. The latch of Port 0D is located in address 73H of BANK0 of the data memory.	Input (Equipped with pull-down resistor)
63	ADC_0	A/D converter input	This is the A/D converter input pin. It is incorporated with the 4-bit A/D converter of the program-based random comparison method. The reference voltage of the A/D converter is V_{DD}.	Input
64	RMC	Interrupt signal input	This is the interrupt input pin equipped with a noise canceller. If the signal is noisy such as the remote control signal, the program is made easier by using this pin. It is possible to specify in the program whether to apply an interrupt at the rise or the fall of the input signal to this pin. The interrupt is applied at the rise if the IEG flag is reset, and at the fall if the IEG flag is set. If the CE is reset, the IEG flag is reset thus applying the interrupt at the rising edge.	Input

1.2 PIN'S EQUIVALENT CIRCUIT

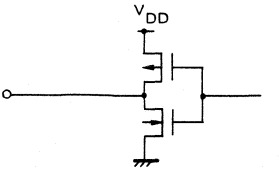
P0A (P0A$_3$/SO, P0A$_2$/$\overline{SCK}$)
P0B (P0B$_2$, P0B$_1$, P0B$_0$/SI)
P1B (P1B$_2$, P1B$_1$, P1B$_0$)
P1C (P1C$_3$, P1C$_2$/ADC$_7$, P1C$_1$/ADC$_6$, P1C$_0$/ADC$_5$)
P2A (P2A$_3$, P2A$_2$, P2A$_1$, P2A$_0$)
} (Input/output)



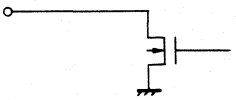
P0A (P0A$_1$/SCL, P0A$_0$/SDA): (Input/output)



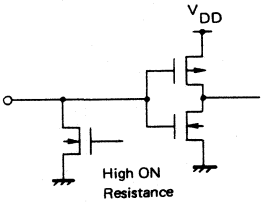
P0C (P0C$_3$, P0C$_2$, P0C$_1$, P0C$_0$)
P1D (P1D$_3$, P1D$_2$, P1D$_1$, P1D$_0$)
RED, GREEN, BLUE, BLANK
} (Output)



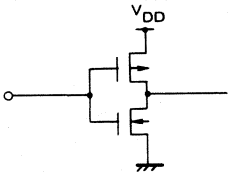
PWM (PWM_3, PWM_2, PWM_1, PWM_0, PWM_{RMP})
P1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
P2B ($P2B_3$, $P2B_2$, $P2B_1$, $P2B_0$)
P2C ($P2C_3$, $P2C_2$, $P2C_1$, $P2C_0$)
} (Output)



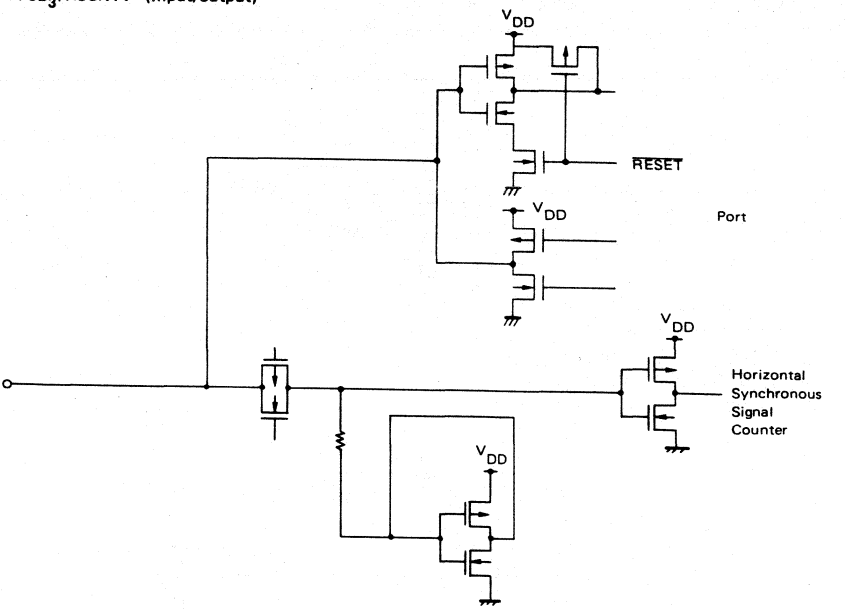
P0D ($P0D_3/ADC_7$, $P0D_2/ADC_6$, $P0D_1/ADC_5$, $P0D_0/ADC_4$): (Input)



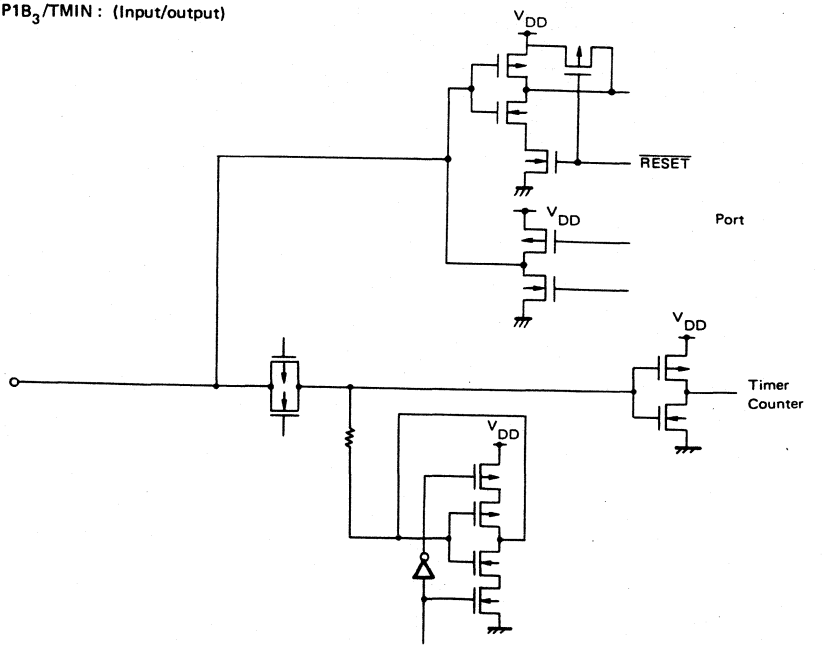
ADC_0: (Input)



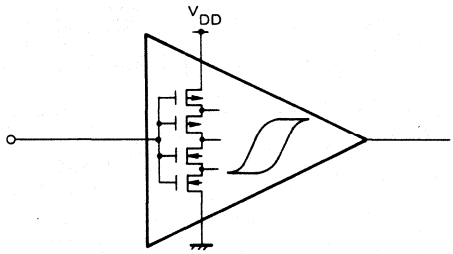
$P0B_3$/HSCNT: (Input/output)



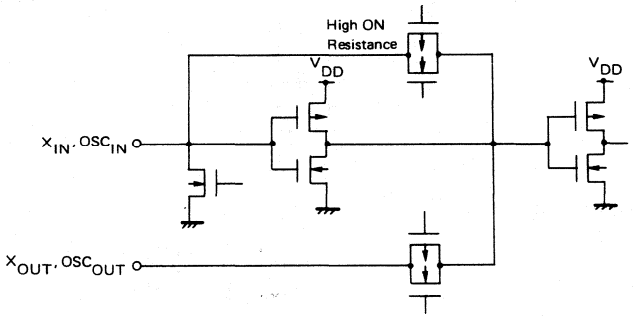
$P1B_3$/TMIN: (Input/output)



$\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$, RMC, CE : (Schmitt trigger input)



X_{IN}, OSC_{IN} : (Input)
X_{OUT}, OSC_{OUT} : (Output)



ELECTRICAL SPECIFICATIONS

ABSOLTE MAXIMUM RATINGS

Power Supply Voltage	V_{DD}		-0.3 to +6.0	V
Input Voltage	V_I		-0.3 to V_{DD}	V
Output Voltage	V_O	Except P1A, P2B, P2C and PWM	-0.3 to V_{DD}	V
Output Current High	I_{OH}	1 pin	-12	mA
		All pins	-20	mA
Output Current Low	I_{OL1}	1 pin (except P1A)	12	mA
		All pins (except P1A)	20	mA
Output Current Low	I_{OL2}	1 pin (P1A only)	17	mA
		All pins (P1A only)	60	mA
Output Withstand Voltage	V_{BDS}	P1A, P2B, P2C, PWM	13	V
Operating Temperature	T_{opt}		-20 to +70	°C
Storage Temperature	T_{stg}		-55 to +125	°C

RECOMMENDED OPERATING CONDITION

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	All functional operations
Power Supply Voltage	VDD2	4.0	5.0	5.5	V	Only IDC stop
Data Hold Voltage	V_{DR}	2.2		5.5	V	Clock oscillation stop
Output Withstand Voltage	V_{BDS}			12.5	V	P1A, P2B, P2C, PWM
Power Supply Voltage Rise Time	t_{rise}			500	ms	V_{DD}: 0 4.0 V

DC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	I_{DD1}		7	15	mA	CPU and IDC operations V_{DD} = 5.5 V
Supply Current	I_{DD2}		3.5	15	mA	CPU operation, IDC stop V_{DD} = 5.5 V
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0D P1B, P1C, P2C
Input Voltage High	V_{IH2}	0.8 V_{DD}		V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0D, P1B, P1C, P2A
Input Voltage Low	V_{IL2}	0		0.2 V_{DD}	V	CE, RMC, $\overline{V_{SYNC}}$ $\overline{H_{SYNC}}$
Output Current High	I_{OH}	−1	−2		mA	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK $V_{OH} = V_{DD} - 1$ V
Output Current Low	I_{OL1}	2	3		mA	P0A, P0B, P0C, P1B, P1C, P1D, RED, GREEN, BLUE, BLANK V_{OL} = 1 V
Output Current Low	I_{OL2}	15	20		mA	P1A V_{OL} = 1 V
Output Current Low	I_{OL3}	1	2		mA	P2B, P2C, PWM V_{OL} = 1 V
Input Current High	I_{IH}		50		μA	When P0D is pulled down $V_{IH} = V_{DD}$
Data Hold Current	I_{DR}			10	μA	Clock oscillation stop T_a = 25 °C, V_{DD} = 5.5 V
Output Leakage	I_L			1	μA	$P0A_0$, $P0A_1$, P1A, P2B, P2C, PWM V_{OH} = 5 V

AC CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

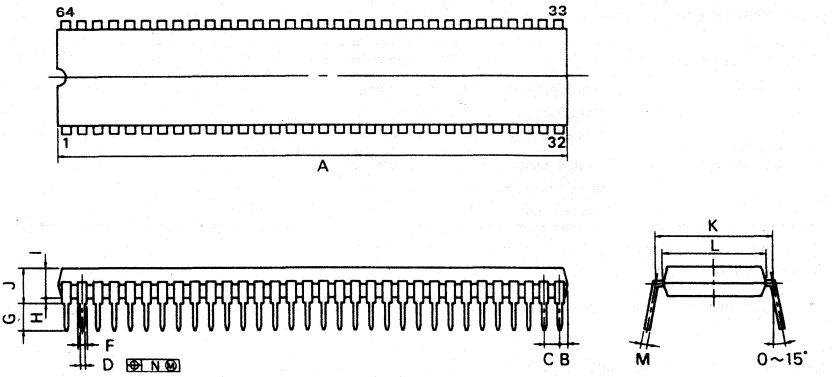
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Frequency	f_{TMIN}	50		60	Hz	$P1B_3$/TMIN
Input Frequency	f_{HS}	10		20	kHz	$P0B_3$/HSCNT
IDC Jitter	IDC_G		3	4	ns	V_{DD} = 4.5 to 5.5 V

A/D CONVERTER CHARACTERISTICS (T_a = −20 to +70 °C, V_{DD} = 4.0 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
A/D conversion total error		±1/2		±1	LSB	
A/D input impedance		1			M	

PACKAGE DIMENSION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17053CW-xxx

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below. Flow time: 10 seconds or below. Number of flow process: 1, Exposure limits: None	
Partial heating method	Terminal temperature: 300 °C or below. Flow time: 10 seconds or below. Exposure limits*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65% or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below. Flow time: 10 seconds or below	

SINGLE-CHIP MICROCONTROLLER

The μPD17102 is a four-bit single chip microcontroller which has a built-in LCD controller, D/A converter, and operational amplifier. This CPU uses the μPD17000 architecture, allowing data transfer and operation between data memory areas or between data memory areas and peripheral circuits with only one instruction. It also supports 16-bit (1-word) instructions.

FEATURES

- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 208 words (208 x 4 bits)
- Command execution time : 2.0 μs (8 MHz, ceramic/crystal oscillator)
- Interrupting function (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 channels (built-in modulo)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
  (Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel multiplexer input comparator
- 6-bit D/A converter
- Feasible to realize the 4-channel 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller/driver
  (14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detection selectable
- Standby function (Stop/Halt)

USE:

Electronic rice cooker and blood pressure meter, etc.

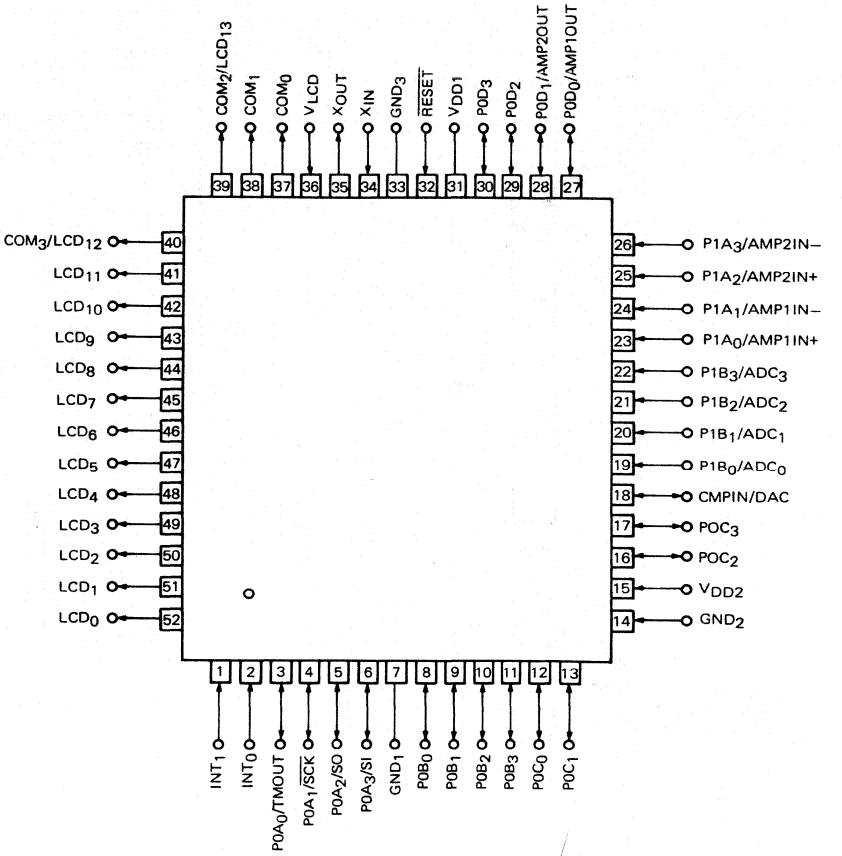
ORDERING INFORMATION

Order Code	Package
μPD17102G-XXX-00	52-pin plastic QFP (bent lead)
μPD17102G-XXX-03	52-pin plastic QFP (straight lead)

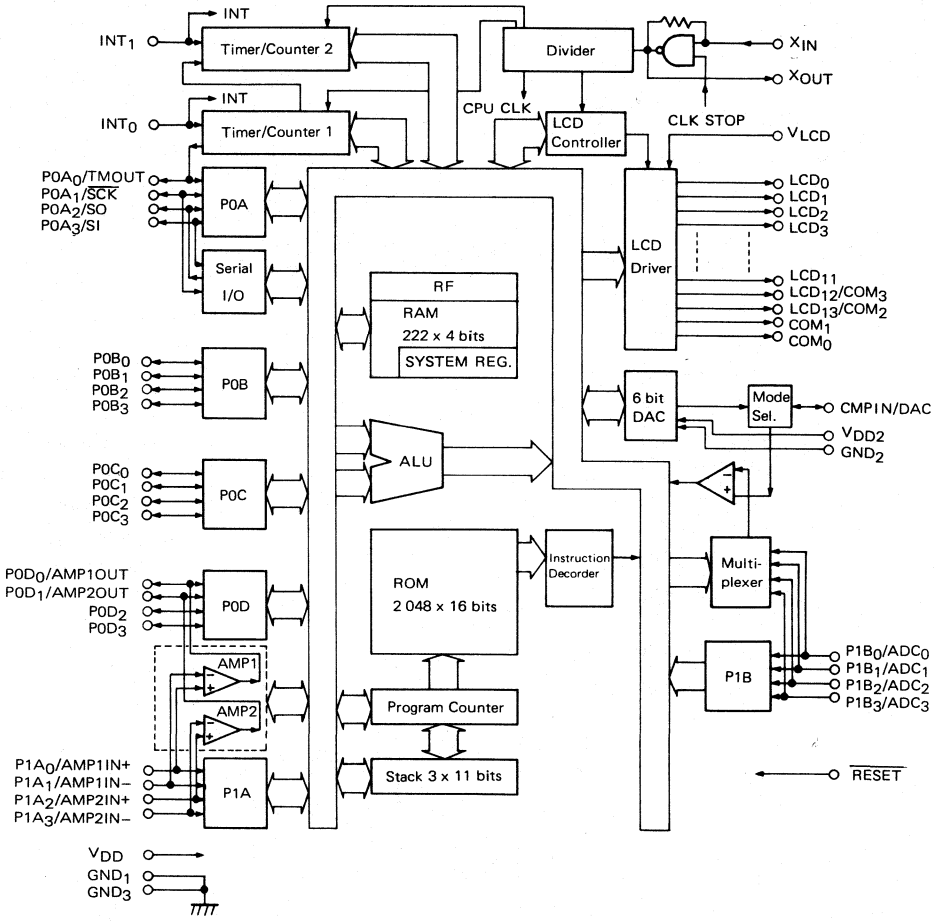
OUTLINE OF FUNCTIONS

- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 222 words (222 x 4 bits)
- Stack level : 3 levels
- Instruction cycle : 2 μs (when operated at 5.0 V and 8 MHz)
- Interrupting function : (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 CH (with modulo integrated)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
  (Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel input comparator with multiplexer
- 6-bit D/A converter
- Feasible to realize 4-channel, 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller (14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detecting function
- Standby function (STOP/HALT)
- Data/memory low supply voltage holding function
- Oscillator circuit for system clock (ceramic and crystal)
- Single power unit (3.0 to 6.0 V, but 4.5 to 6.0 V when the operational amplifier is used)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. OUTLINE

The μPD17102 is a 4-bit single chip microcontroller which integrates all the following circuits on one chip: 4-bit ALU, program memory (ROM), data memory (RAM), I/O ports, timer/event counter, serial interface, vector interrupt circuit.

This chip using the μPD17000 Series architecture has various built-in peripheral circuits including analog circuits, allowing the user to incorporate it into electrical appliances and intelligent units in a distributed system for home automation.

For program development, NEC supports the in-circuit emulator (IE-17K), so that the user can debug programs easily by using the emulator together with the SE board for each product.

2. PIN FUNCTIONS

2.1 Input/Output Ports

2.1.1 $P0A_0$ to $P0A_3$ (Port 0A): Bi-directional input/output ports

Port 0A is a 4-bit input port (pins from $P0A_0$ to $P0A_3$) with output latch circuits.

This port is mapped to 70H at bank 0 in the data memory space and accessed with normal data memory operation instructions. The direction of input/output is switched for all four bits by the P0AGIO value. Setting P0AGIO to "1" outputs the value stored at 70H of bank 0 to the pin and setting to "0" disables output and sets input mode.

Regardless of the P0AGIO value, the pin status can be read with a data memory reference instruction. The contents of the output latch remain unchanged unless the data at 70H of bank 0 is rewritten.

$P0A_0$ is shared by the timer 1 output pin TMOUT. It operates as TMOUT when PTOUTON in the register file is "0" and in normal input/output mode.

When TMOUT is selected, this pin outputs "1" at time 1 reset and reverses the output each time the timer 1 value matches the contents of the modulo register. At this time, this pin is set in output mode regardless of the P0AGIO value. The pin status at this time can also be read with a data memory reference instruction. The output latch as $P0A_0$ is independent of TMOUT, and therefore data can be written to 70H of bank 0 even if the pin operates as TMOUT and the data is output when PTOUTON is set to "0" while P0AGIO is "1."

$P0A_1$ to $P0A_3$ are shared by $\overline{SCK}$, SO, and SI of the serial interface. The PA0 pin is set in normal input/output mode when the SIOON value in the register file is "0" and used as the SIO pin when it is "1."

In the port 0A input/output format, either of the Nch open/drain input/output or Nch open/drain input/output with a built-in pull-up resistor is selectable by the mask option. In Nch open/drain input/output mode, the port has a 9 V withstanding voltage and is suitable for an interface with a circuit using a different supply voltage. By using the Nch open/drain input/output structure, a 2-wire serial interface can also be used.

When SIOON is "1," data cannot be output to the $\overline{SCK}$ and SO pins as a port. Even if data is transferred to address 70H of bank 0, this data cannot be input to $P0A_1$ to $P0A_3$. At this time, only $P0A_3$ is available.

When the $\overline{SCK}$ pin is in input mode, however, data can be written to the $P0A_1$ output latch.

Table 2-1 Port 0A functions

PTOUTON	SIOON	P0AGIO	Write to bank 0, 70H	Read from bank 0, 70H	Pin function			
					$P0A_0$	$P0A_1$	$P0A_2$	$P0A_3$
0	0	0	All four bits are valid.	Enable. (Pin status)	$P0A_0$ IN	$P0A_1$ IN	$P0A_2$ IN	$P0A_3$ IN
		1	All four bits are valid.		$P0A_0$ OUT	$P0A_1$ OUT	$P0A_2$ OUT	$P0A_3$ OUT
	1	0	Only $P0A_0$ is valid.		$P0A_0$ IN	$\overline{SCK}$	SO	SI
		1	Only $P0A_0$ is valid.		$P0A_0$ OUT			
1	0	0	All four bits are valid		TMOUT	$P0A_1$ IN	$P0A_2$ IN	$P0A_3$ IN
		1	All four bits are valid.			$P0A_1$ OUT	$P0A_2$ OUT	$P0A_3$ OUT
	1	0	Only $P0A_0$ is valid.			$\overline{SCK}$	SO	SI
		1	Only $P0A_0$ is valid.					

Note: If data is written to 70H of bank 0 when SIOON is "1," this data can be written to $P0A_1$ only when the $\overline{SCK}$ pin is in input mode.

2.1.2 $P0B_0$ to $P0B_3$ (port 0B), $P0C_0$ to $P0C_3$ (port 0C): Bi-directional input/output

Ports 0B and 0C are 4-bit input/output pins with output latch circuits: From $P0B_0$ to $P0B_3$ and from $P0C_0$ to $P0C_3$. These ports are mapped to 71H and 72H of bank 0 in the data memory space, respectively and are accessed with normal data memory operation instructions like port 0A. The direction of input/output is switched for all 4-bits by the P0BGIO or P0CGIO value in the register file. Setting the value to "1" outputs the data at 71H or 72H of bank 0 to the corresponding pin and "0" disables the output and sets the input mode. Regardless of the P0BGIO and P0CGIO values, the pin status is read when a data memory reference instruction is executed. At this time, the contents of the output latch remain unchanged.

The input/output format of ports 0B and 0C is the CMOS (push/pull) type.

Table 2-2 Functions of ports 0B and 0C

P0BGIO P0CGIO	Input/output direction of pin	Write to bank 0, 71H or 72H	Read from bank 0, 71H or 72H
0	Input (output disable)	Available	Available (pin status input)
1	Output		

2.1.3 $P0D_0$ to $P0D_3$ (port D): Bi-directional input/output

Port 0D comprises 4-bit input/output pins with output latch circuits. It is mapped to 73H of bank 0 in the data memory space. The input/output direction is switched by the P0DGIO value in the register file.

$P0D_0$ is shared with the AMP1 output pin AMP1OUT, and $P0D_1$ is shared with the AMP2 output pin AMP2OUT. These bits are used in normal input/output mode when the AMP1EN or AMP2EN values in the register file are "0" and as AMP1OUT and AMP2OUT respectively when the values are "1."

When AMP1OUT and AMP2OUT are selected, the pins are used as the AMP1OUT and AMP2OUT output pins, regardless of the P0DGIO value. A data memory reference instruction reads the pin status regardless of the function selected for the pin. At this time, the pin potential is intermediate, the read value is undefined. The μPD17102 reads only at the moment the instruction is executed and disables other input circuits. Therefore, the through current does not flow through the input circuit.

The $P0D_0$ and $P0D_1$ output latch circuits are independent of AMP1OUT and AMP2OUT. Therefore, data can be written to bank 0, 73H by setting AMP1EN and AMP2EN to "1" even if the pins operate as AMP1OUT and AMP2OUT. When P0DGIO is "1," the pins output data as a port by setting AMP1EN and AMP2EN to "0."

The port 0D input/output format is CMOS (push/pull) input/output.

Table 2-3 Port 0D functions

AP1EN AP2EN	P0DGIO	Write to bank 0, 73H	Read from bank 0, 73H	Pin function			
				$P0D_0$	$P0D_1$	$P0D_2$	$P0D_3$
0	0	All four bits are valid.	Enable. Pin status.	$P0D_0$ IN	$P0D_1$ IN	$P0D_2$ IN	$P0D_3$ IN
	1			$P0D_0$ OUT	$P0D_1$ OUT	$P0D_2$ OUT	$P0D_3$ OUT
1	0			AMP1OUT	AMP2OUT	$P0D_2$ IN	$P0D_3$ IN
	1					$P0D_2$ OUT	$P0D_3$ OUT

Note: The AMP output control is selectable for AMP1/2 separately.

2.1.4 $P1A_0$ to $P1A_3$ (port 1A): Input

Port 1A comprises 4-bit input pins.

It is mapped to 70H of bank 1 in the data memory space.

$P1A_0$ and $P1A_1$ are shared with AMP1 non-reverse input (AMP1IN+) and reverse input (AMP1IN−), PI1A and P1A3 are shared with AMP2 non-reverse input (AMP2IN+) and reverse input (AMP2IN−). These pins are not switched and are always connected to both input circuits of the operator amplifier (analog input) and port (digital input).

When used as analog input pins, apply an intermediate potential or AC voltage. If a data memory reference instruction is executed at this time, an undefined value is read. Similar to port 0D, the through current does not flow through the input circuit.

Port 1A has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to the port (data write to 70H in bank 1) are invalid.

Table 2-4 Port 1A function

Read from bank 1, 70H (logical input)	Write to bank 1, 70H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Always connected to AMP input.

2.1.5 $P1B_0$ to $P1B_3$ (port 1B): Input

Port 1B comprises 4-bit input pins.

It is mapped to 71H of bank 1 in the data memory space.

Only one of these pins can be set as the input pin of the non-reserve input from the comparator by ADCCH0 and ADCCH1. For more information, see Section 3.12. Similar to ports 0D and 1A, the pin status of port 1B is read with the data memory reference instruction, regardless of the selected pin function, and the through current does not flow through the input circuit even if the intermediate potential is applied.

Port 1B also has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to port 1B (data write to 71H in bank 1) are invalid.

Table 2-5 Port 1B function

Read from bank 1, 71H (logical input)	Write to bank 1, 71H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Either pin is connected to the comparator input (by ADCCH0 and ADCCH1).

2.2 INT_0, INT_1

INT_0 and INT_1 are interrupt request input pins for which the active rising or falling edge is selectable by IEG_0 and IEG_1. At the rising or falling edge of the INT_0 or INT_1 signal selected by IEG_0 and IEG_1, the interrupt request flag (IRQ0, IRQ1) is set.

To prevent malfunctions from noise, the pins has a built-in noise remover. The status of the pin for which noise is eliminated by the noise remover is read by referencing INT_0 and INT_1 in the register file with the PEEK instruction, so that the pins are simply used as input pins.

In addition, INT_0/INT_1 are the count clock input pins of timer 1/2, respectively, and are used when external clocks are selected as timer count clock sources. When sharing the timer input and INT_0/INT_1 interrupt request input, note that the INT_0/INT_1 interrupt request flag is also set by the clock.

The INT_1 pin is also used to detect zero-cross when ZCROSS in the register file is set to "1."

2.3 CMPIN/DAC, V_{DD2}, GND_2

V_{DD2} and GND_2 are pins used to apply the reference voltage of the built-in 6-bit D/A converter. Apply the V_{DD} potential to V_{DD2} and the GND potential to GND_2. These two pins are separated from V_{DD} and GND and can have separated digital and analog power sources. The applied voltage between the pins is divided into 2^6 steps (64 steps). The analog value corresponding to digital data stored in four bits of 72H and high-order two bits of 73H of bank 1 in the data memory space is the D/A converter output.

To output the D/A converter data from the CMPIN/DAC pin, set DACEN to "1" and CMPEN to "0" in the register file.

To use a comparator, set DACEN to "0" and CMPEN to "1" in the register file. At this time, the CMPIN/DAC pin operates as the reverse input pin of the comparator (CMPIN). Apply a voltage with the same potential as V_{DD} to the V_{DD2} pin. Also apply the same potential to GND_2 pin to minimize the current flowing through the D/A converter which is not used.

When using the 6-bit D/A converter under program control, set DACEN to "1" and CMPEN to "1" in the register file. At this time, D/A converter data is not output externally, but is directly input to the comparator reverse input pin. Therefore, the CMPIN/DAC pin is not used.

Table 2-6 V_{DD2}, GND_2, and CMPIN/DAC functions

DACEN	CMPEN	V_{DD2}	GND_2	CMPIN/DAC	Function
0	0	V_{DD} potential	V_{DD} potential	V_{DD} potential	D/A converter and comparator are not used.
		V_{DD2}	GND_2	High impedance	Initial state when the D/A converter is used **(Note)**.
0	1	V_{DD} potential	V_{DD} potential	CMPIN	When the comparator is used.
1	0	V_{DD2}	GND_2	DAC	When the D/A converter is used.
1	1	V_{DD2}	GND_2	V_{DD} potential	Used as D/A converter

V_{DD} potential indicates that V_{DD} potential is applied externally.

Note: DACEN and CMPEN are set to "0" at reset.

2.4 V_{LCD}

V_{LCD} is a power supply pin for driving the liquid crystal display panel (LCD panel).

Depending on the bias method used, it generates the 1/2 V_{LCD}, 1/3 V_{LCD}, and 2/3 V_{LCD} voltages. When using LCD_0 to LCD_{13} as the output pins, apply the high voltage under the supply voltage (V_{DD}).

2.5 LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}, COM_1, COM_0

LCD_0 to LCD_{11}, COM_3, LCD_{12}, COM_2/LCD_{13}, COM_1, and COM_0 are LCD panel segment driver pins used to select drive method, such as 14-segment 2-common, 13-segment 3-common, 12-segment 4-common.

LCD_0 to LCD_{13} are used as output pins when LCDEN in the register file is "0." At this time, COM_1 and COM_0 are not used.

For more information on the LCD panel, see Section 3.10.

Table 2-7 LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}, COM_1, and COM_0 functions

LCDEN	LCD_0 to LCD_{11}, COM_3/LCD_{12}, COM_2/LCD_{13}	COM_1, COM_0
0	All are output pins.	Not used
1	LCD drivers and common drivers	Common drivers

2.6 X_{IN}, X_{OUT}

X_{IN} and X_{OUT} are pins used to connect the oscillation vibrator in the system clock generator.

2.7 $\overline{RESET}$

$\overline{RESET}$ is a low-level active reset input pin. The reset has priority over all other operations.

In addition to CPU initial start, this pin is also used to release standby mode.

2.8 V_{DD1}

V_{DD1} is a positive power supply pin.

2.9 GND_1, GND_2

GND_1 and GND_2 are GND potential pins. Wire them so that the same potential is used externally.

2.10 Pin Mask Options

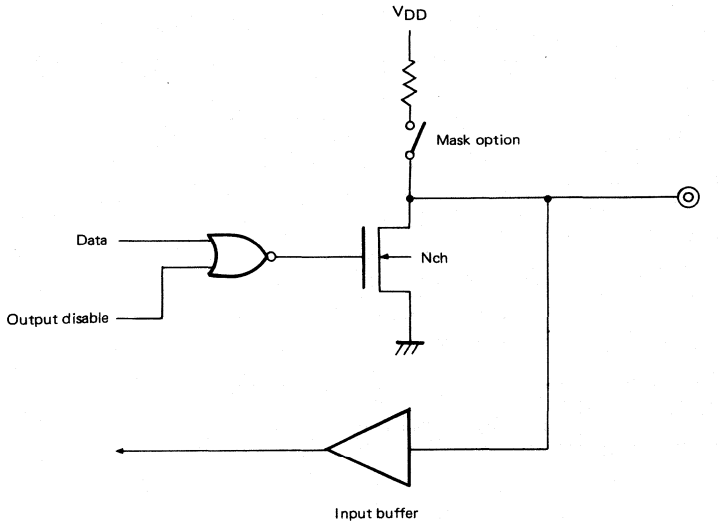
The μPD17102 pins have the mask options listed below. These option can be selected bit according to purpose.

Pin name	Mask option
POA_0 to POA_3	(1) Nch open-drain input/output (2) Nch open-drain plus built-in pull-up resistor input/output
$P1A_0$ to $P1A_3$ $P1B_0$ to $P1B_3$	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
INT_0 INT_1	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
$\overline{RESET}$	(1) No built-in resistor (2) Built-in pull-up resistor

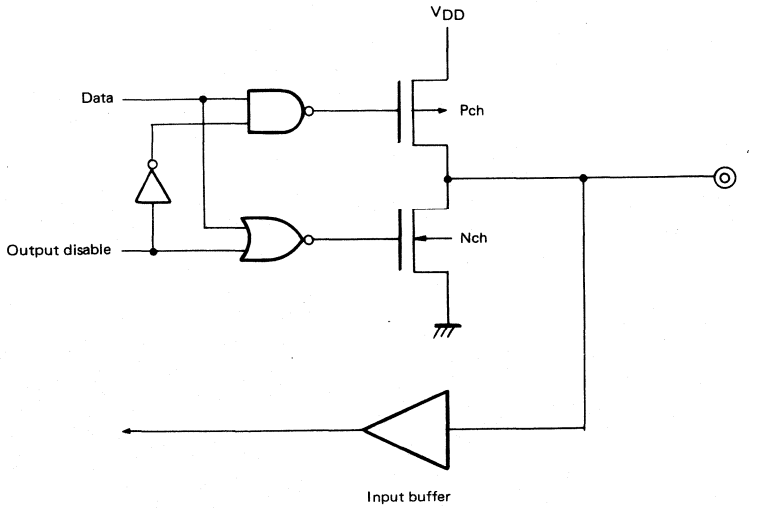
2.11 Pin Input/Output Circuits

The Input/output circuit of each pin of the μPD17102 is shown below in a partly simplified format:

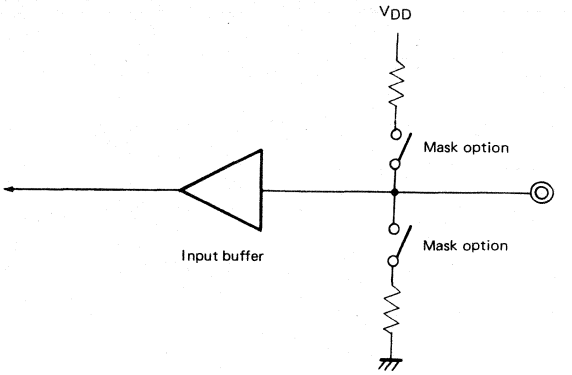
(1) POA_0 to POA_3



(2) POB_0 to POB_3, POC_0 to POC_3, POD_0 to POD_3



(3) $P1A_0$ to $P1A_3$, $P1B_0$ to $P1B_3$, INT_0, INT_1



(4) $\overline{RESET}$

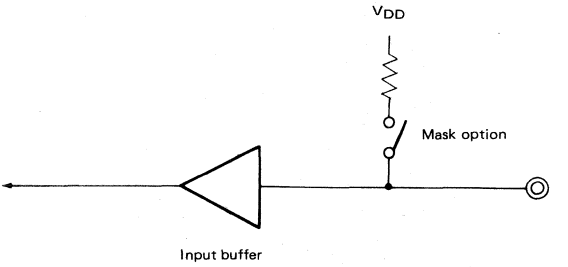


Table 2-8 Digital input/output port pin functions

PIN NAME	I/O	COMBINED USE	FUNCTION	WHEN RESET
$P0A_0$	Input/output	TMOUT	4-bit I/O port (port 0A)	High impedance (P0An input)
$P0A_1$		$\overline{SCK}$		
$P0A_2$		SO		
$P0A_3$		SI		
$P0B_0$ to $P0B_3$	Input/output		4-bit I/O port (port 0B) Large current (15 mA)	High impedance (input)
$P0C_0$ to $P0C_3$	Input/output		4-bit I/O port (port 0C) Large current (15 mA)	High impedance (input)
$P0D_0$	Input/output	AMP1OUT	4-bit I/O port (port 0D) Middle current (10 mA)	High impedance (P0Dn input)
$P0D_1$		AMP2OUT		
$P0D_2$ to $P0D_3$				High impedance (input)
$P1A_0$	Input	AMP1IN+	4-bit input port (port 1A)	Input
$P1A_1$		AMP1IN–		
$P1A_2$		AMP2IN+		
$P1A_3$		AMP2IN–		
$P1B_0$	Input	ADC_0	4-bit input port (port 1B)	Input
$P1B_1$		ADC_1		
$P1B_2$		ADC_2		
$P1B_3$		ADC_3		

Table 2-9 Pins other than port pins

Pin name	Input/output	Shared	Function	At reset
INT_0	Input		Used as both the timer 1 count clock input pin and the external interrupt input pin.	Input
INT_1	Input		Used as the timer 2 count clock input pin and external interrupt input pin. Zero-cross detection function is selectable.	Input
TMOUT	Output	$P0A_0$	Timer 1 output pin	$P0A_0$ input
$\overline{SCK}$	Input/output	$P0A_1$	Serial clock input/output pin	$P0A_1$ input
SO	Output	$P0A_2$	Serial data output pin	$P0A_2$ input
SI	Input	$P0A_3$	Serial data input pin	$P0A_3$ input
AMP1OUT	Output	$P0D_0$	AMP1 output pin	$P0D_0$ input
AMP2OUT		$P0D_1$	AMP2 output pin	$P0D_1$ input
AMP1IN+	Input	$P1A_0$	AMP1 non-reversed input pin	Input
AMP1IN−		$P1A_1$	AMP1 reversed input pin	
AMP2IN+		$P1A_2$	AMP2 non-reversed input pin	
AMP2IN−		$P1A_3$	AMP2 reversed input pin	
ADC_0 to ADC_3	Input	$P1B_0$ to $P1B_3$	Comparator input pin	Input
V_{DD2}	Input		D/A converter reference voltage input pin (high-potential side)	
GND_2	Input		D/A converter reference voltage input pin (low-potential side)	
CMPIN	Input/output	DAC	Used as the D/A converter output pin and comparator input pin.	High impedance
LCD_0 to LCD_{11}	Output		LCD segment driver output pin. Also used as the output port.	Output
COM_3	Output	LCD_{12}	Used as the LCD common driver output and LCD segment driver pin. Also used as an output port.	Output
COM_2		LCD_{13}		
COM_0, COM_1	Output		LCD common driver output pin	Output
V_{LCD}	Input		LCD driver split potential setting pin	Input
$\overline{RESET}$	Input		System reset input pin	Input
V_{DD1}			Positive power supply pin	
GND_1, GND_3			GND potential pin	
X_{IN}, X_{OUT}			System clock oscillator pin	

9. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V		
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V	P0A	(1)
		−0.3 to +11	V		(2)
		−0.3 to V_{DD} + 0.3	V	All pins other than P0A	
Output Voltage	V_O	−0.3 to V_{DD} +0.3	V	P0A	(1)
		−0.3 to +11	V		(2)
		−0.3 to V_{LCD} +0.3	V	Segment/common pins	
		−0.3 to V_{DD} +0.3	V	Pins other than above	
High-Level Output Current	I_{OH}	−5	mA	1 pin	
		−20	mA	Total of all pins	
Low-Level Output Current	I_{OL}	15	mA	1 pin	P0A, P0D
		30	mA		P0B, P0C
		100	mA	Total of all pins	
Operating Temperature	T_{opt}	−40 to +85	°C		
Storage Temperature	T_{stg}	−65 to +150	°C		
Power Consumption	P_d	190	mW	T_a = 85 °C	

Remarks: 1. N-ch open/drain output plus built-in pull-up resistor output
2. N-ch open/drain input/output

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_{IN}			15	pF	f = 1 MHz Pins other than those measured: 0 V
Output Capacity	C_{OUT}			15	pF	
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		9	V	At SI or $\overline{SCK}$ input	
	V_{IH2}	0.7 V_{DD}		9	V	At P0A input	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	INT_1, INT_1, $\overline{RESET}$	
	V_{IH4}	0.7 V_{DD}		V_{DD}	V	Pins other than above	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	SI, $\overline{SCK}$, INT_0, INT_1, $\overline{RESET}$	
	V_{IL2}	0		0.3 V_{DD}	V	Pins other than above	
High-Level Output Voltage	V_{OH}	V_{DD}−2.0	V_{DD}−0.4		V		V_{DD} = 4.5 to 6.0 V I_{OH} = −1 mA
		V_{DD}−1.0	V_{DD}−0.04		V		I_{OH} = −100 μA
Low-Level Output Voltage	V_{OL}		0.85	2.0	V	P0B, P0C	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA
			0.06	0.5	V		I_{OL} = 600 μA
			0.85	2.0	V	P0A, P0D	V_{DD} = 4.5 to 6.0 V I_{OL} = 10 mA
			0.15	0.4	V		V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA
			0.04	0.5	V		I_{OL} = 400 μA
High-Level Input Leak Current	I_{LIH1}			3	μA	Other than XI and XO	V_{IN} = V_{DD}
	I_{LIH2}			10	μA	XI, XO	V_{IN} = V_{DD}
	I_{LIH3}			10	μA	P0A (3)	V_{IN} = 9 V
Low-Level Input Leak Current	I_{LIL}			−3	μA	Other than XI and XO	V_{IN} = 0 V
				−10	μA	XI, XO	V_{IN} = 0 V
High-Level Output Leak Current	I_{LOH1}			3	μA		V_{OUT} = V_{DD}
	I_{LOH2}			10	μA	P0A (3)	V_{OUT} = 9 V
Low-Level Output Leak Current	I_{LOL}			−3	μA		V_{OUT} = 0 V
Input pin with built-in resistor (pull up/pull down)		35	65	110	kΩ	INT0, INT1, P1A, P1B	
Input pin with built-in resistor (pull up)		35	65	110	kΩ	$\overline{RESET}$	
Input pin with built-in resistor (pull down)		7	15	26.5	kΩ	P0A	
Supply Current (4)	I_{DD1}		1500	4500	μA	Operation mode	V_{DD} = 5 V ± 10 % f_{CC} = 8 MHz
			250	750	μA		V_{DD} = 3 V ± 10 % f_{CC} = 2 MHz
	I_{DD2}		550	1600	μA	Halt mode	V_{DD} = 5 V ± 10 % f_{CC} = 8 MHz
			110	330	μA		V_{DD} = 3 V ± 10 % f_{CC} = 2 MHz
	I_{DD3}		0.1	10	μA	Stop mode	V_{DD} = 5 V ± 10 %
			0.1	5	μA		V_{DD} = 3 V ± 10 %

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
V_{LCD} Voltage Range	V_{LCD}	3.0		V_{DD}	V		
Common Output Impedance (5)	R_{COM}		40		kΩ		V_{DD} = 4.5 to 6.0 V
Segment Output Impedance (5)	R_{SEG1}		40		kΩ	At LCD drive	V_{DD} = 4.5 to 6.0 V
	R_{SEG2}		5		kΩ	At port operation	Total output of all segment pins Current 2 mA or less $V_{DD} = V_{LCD}$ = 4.5 to 6.0 V
Resistance Between V_{LCD} and GND	R_{VLC}		100		kΩ	When normal	
			3.0		kΩ	When switching	

Remarks: 3. When N-ch open/drain input/output is selected
4. The current that flows through the built-in pull-up or pull-down resistor is excluded
5. 3.5 kΩ (typ.) when switching between the common and segment output.

AMPLIFIER CHARACTERISTICS (T_a = −40 = +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Offset Voltage	V_{OS}		±6	±18	mV	Normal amplifier mode
In-phase Input Voltage	V_{ICM}	0.0		3.6	V	V_{DD} = 5.0 V
Output Voltage Range	V_{OUT}	0.12		4.8	V	V_{DD} = 5.0 V, I_{OUT} = 0 μA
Unity Gain Frequency	f_O		1.5		MHz	
Large Amplitude Gain	A_V		85		dB	V_{DD} = 5.0 V
Output Current	I_{OUT}	−50		100	μA	V_{DD} = 5.0 V
CMRR			75		dB	
SVRR			−60		dB	
Through Rate		1.0			V/μs	
Hold Time	t_{SAMP}		0.05		ms	Sample/hold amplifier mode
Input/Output Voltage Error	V_{DIF}		±6	±18	mV	Sample/hold amplifier mode
Input Voltage Range	V_{IN}		0.12	2.5	V	Sample/hold amplifier mode
Supply Current	I_{AMP}		230	500	μA	

COMPARATOR CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage Range	V_{IN}	V_{SS}		V_{DD}	V	
Response Speed (6)	t_{COMP}	2			IC	
Power Consumption	V_{COMP}		100		μA	V_{DD} = 5.0 V
Absolute Accuracy	V_{IT}		±8.0	±15.0	mV	
Input Resolution	V_{RE}		3.0		mV	

D/A CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V, V_{REFH} = V_{DD}, V_{REFL} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		6	6	6	Bit	
Linearity				±0.5	LSB	
D/A Conversion Time (6)	t_{CONV}	2			IC	At no output load
DAC Current	I_{DAC}		220	390	μA	
A/D Conversion Time (6)		4			IC	

Remarks 6: IC indicates "instruction cycle".

ZERO-CROSS CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Detection Input Level	V_{ZX}	0.8	3.0		V_{P-P}	Input AC
Accuracy	A_{ZX}		±120		mV	50/60 Hz
Detection Input Frequency	f_{ZX}	0.04	1		kHz	

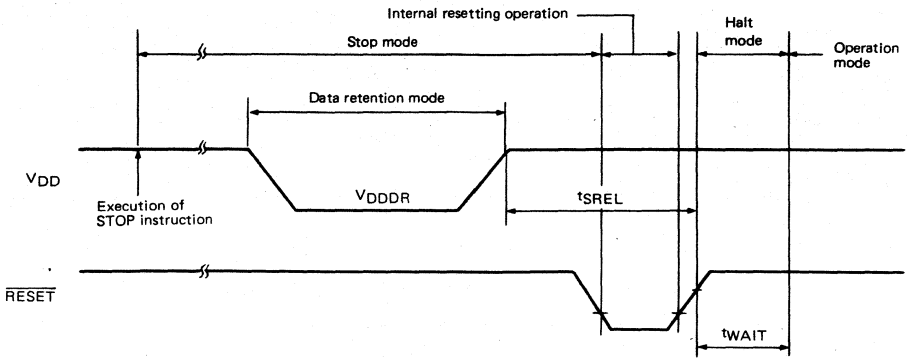
DATA MEMORY DATA RETENTION CHARACTERISTICS AT LOW SUPPLY VOLTAGE IN STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Retention Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	
Wait Time for Stable Oscillation	t_{WAIT}		$2^{19}/fx$		ms	Release by $\overline{\text{RESET}}$ (7)
			(8)		ms	Release by interrupt request

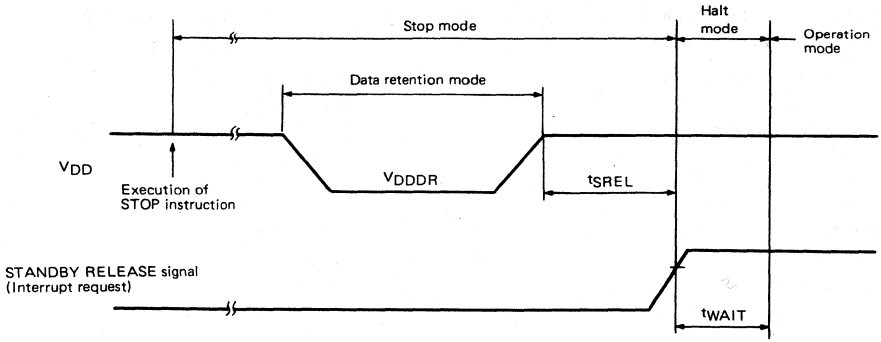
Remarks: 7. fx indicates the oscillator frequency.

8. According to the timer 2 value.

Data Retention Timing (Stop Mode Release by Reset)



Data Retention Timing (Stand-by Release Signal: Stop Mode Release)

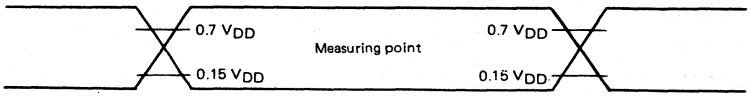


AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

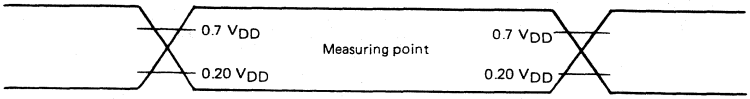
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Internal Clock Cycle Time	t_{CY}	2		30	μs	V_{DD} = 4.5 to 6.0 V	
		8		30	μs		
Event Input Frequency	f_{PO}	0		1000	kHz	duty = 50 %	V_{DD} = 4.5 to 6.0 V
		0		350	kHz		
Event Input Rising/Falling Time	t_{POR} t_{POF}			0.1	μs	Excluding zero-cross mode	
Event Input High/Low Level Width	t_{POH} t_{POL}	0.5			μs	V_{DD} = 4.5 to 6.0 V	
		1.45			μs		
$\overline{SCK}$ Input Cycle Time (9)	t_{KCY}	2.0			μs	At data input	V_{DD} = 4.5 to 6.0 V
		10.0			μs	At data output	
		5.0			μs	At data input	
		13.0			μs	At data output	
$\overline{SCK}$ Input High/Low Level Width (9)	t_{KH} t_{KL}	1.0			μs	At data input	V_{DD} = 4.5 to 6.0 V
		5.0			μs	At data Output	
		2.5			μs	At data input	
		6.5			μs	At data Output	
SI Setup Time (to $\overline{SCK}$↑)	t_{SIK}	100			μs		
SI Hold Time (to $\overline{SCK}$↑)	t_{KSI}	100			μs		
$\overline{SCK}$↓ → SO output delay time (9)	t_{KSO}			4.5	μs	Cp = 100 pF	
INT high/low level width	t_{IOH} t_{IOL}	10			μs		
$\overline{RESET}$ low level width	t_{RSL}	10			μs		

Remarks 9: For SI, SO and $\overline{SCK}$ pins, the N-ch open/drain output plus built-in pull-up resistor input/output.

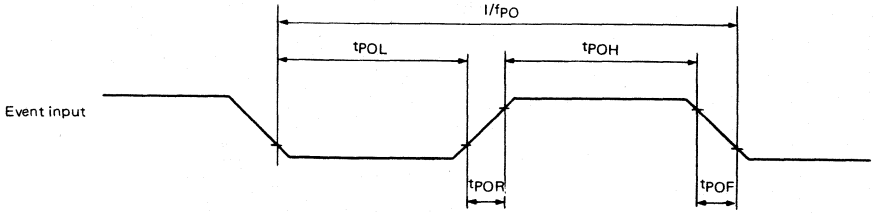
AC Timing Measuring Point (INT_0, INT_1, SI, $\overline{SCK}$ and SO Pins)



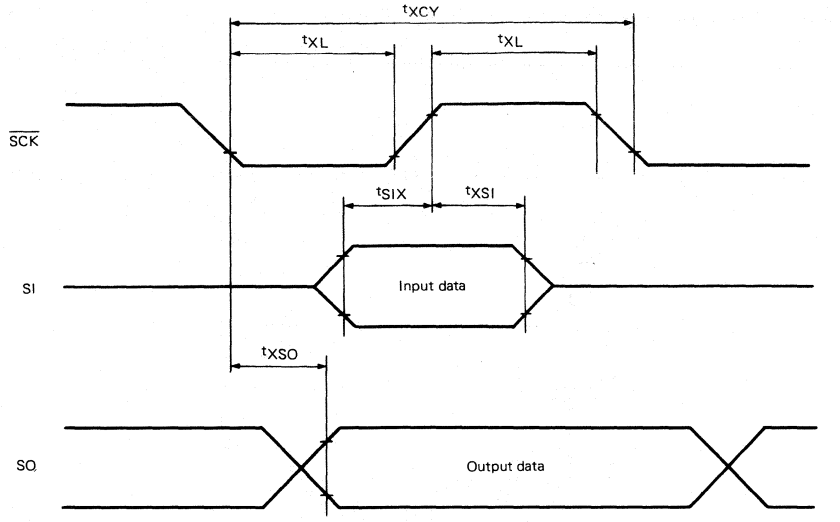
AC Timing Measuring Point (Pins other than INT_0, INT_1, SI, $\overline{SCK}$ SO)



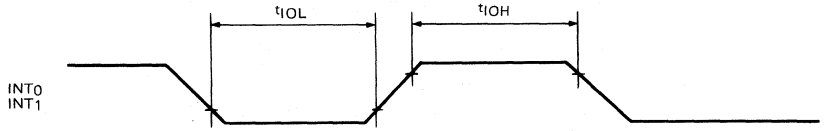
Event Input Timing



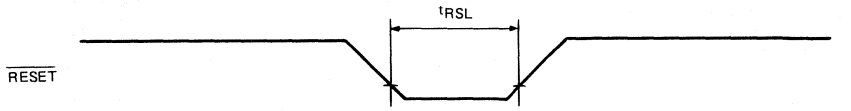
Serial Transfer Timing



INT Input Timing

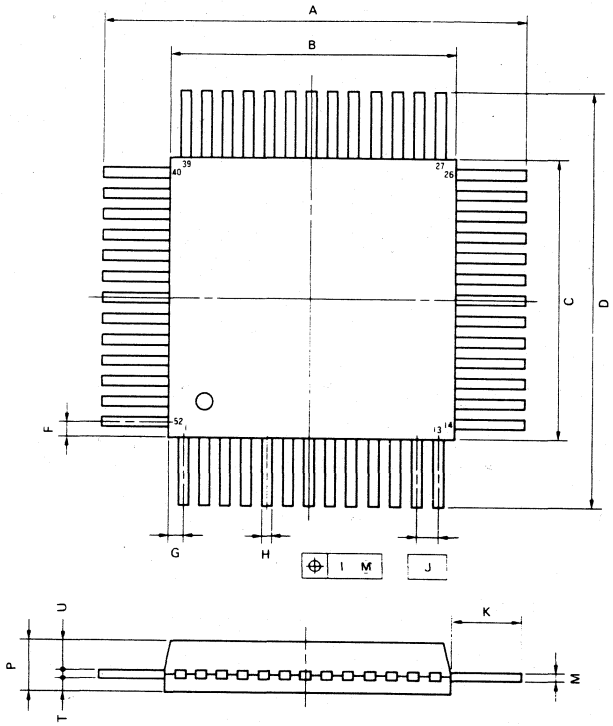


$\overline{\text{RESET}}$ Input Timing



52-PIN PLASTIC QFP

μPD17102G-XXX-03 (Straight lead)



P52G-100-03-1

NOTE

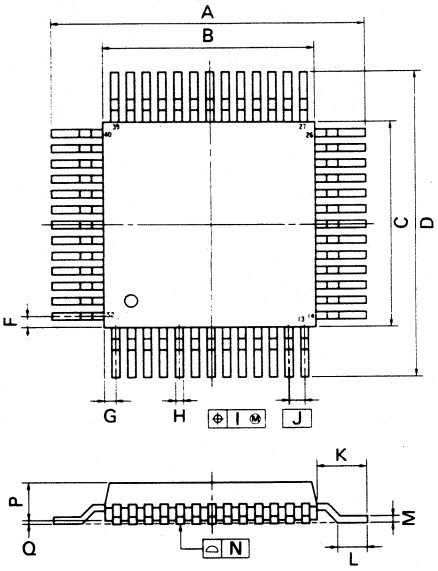
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

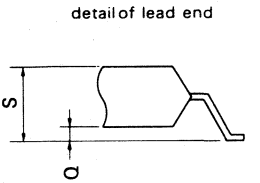
ITEM	MILLIMETERS	INCHES
A	$19.8^{-0.4}$	$0.780^{-0.016}_{-0.017}$
B	$14.0^{-0.2}$	$0.551^{-0.009}_{-0.008}$
C	$14.0^{-0.2}$	$0.551^{-0.009}_{-0.008}$
D	$19.8^{-0.4}$	$0.780^{-0.016}_{-0.017}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{-0.10}$	$0.016^{-0.004}_{-0.005}$
I	0.20	0.008
J	1.0 T.P.	0.039 T.P.
K	$2.9^{-0.2}$	$0.114^{-0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
P	$2.6^{+0.2}_{-0.1}$	$0.102^{-0.008}_{-0.004}$
T	1.0	0.039
U	1.45	0.057

PACKAGE DIMENSIONS

52-PIN PLASTIC QFP

μPD17102G-XXX-00 (bent lead)





P52G-100-00-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$21.0^{\pm 0.4}$	$0.827^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$3.5^{\pm 0.2}$	$0.138^{+0.008}_{-0.009}$
L	$2.2^{\pm 0.2}$	$0.087^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$2.6^{+0.2}_{-0.1}$	$0.102^{+0.009}_{-0.004}$
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

FRONT PANEL CONTROLLER (FPC)

μPD17106

SINGLE-CHIP MICROCONTROLLER

The μPD17106 is a 4-bit single-chip CMOS microcomputer for front panel control.

The CPU uses the μPD17000 architecture, allowing direct operation of data memory, arithmetic operation, and peripheral hardware control by the use of a single instruction. Every instrustion consists of a 16-bit word.

The peripheral hardware includes an abundant series of input/output ports, serial interface, clock generator port,LCD driver for front panel control, key source decoder, and timer for remote control decoding.

The μPD17106 can make up a sophisticated, high performance front panel system.

The OTP (one-time PROM) version of the μPD17106 is also available as the μPD17P106 (*). The μPD17P106 is used for program evaluation or limited production of the μPD17106.

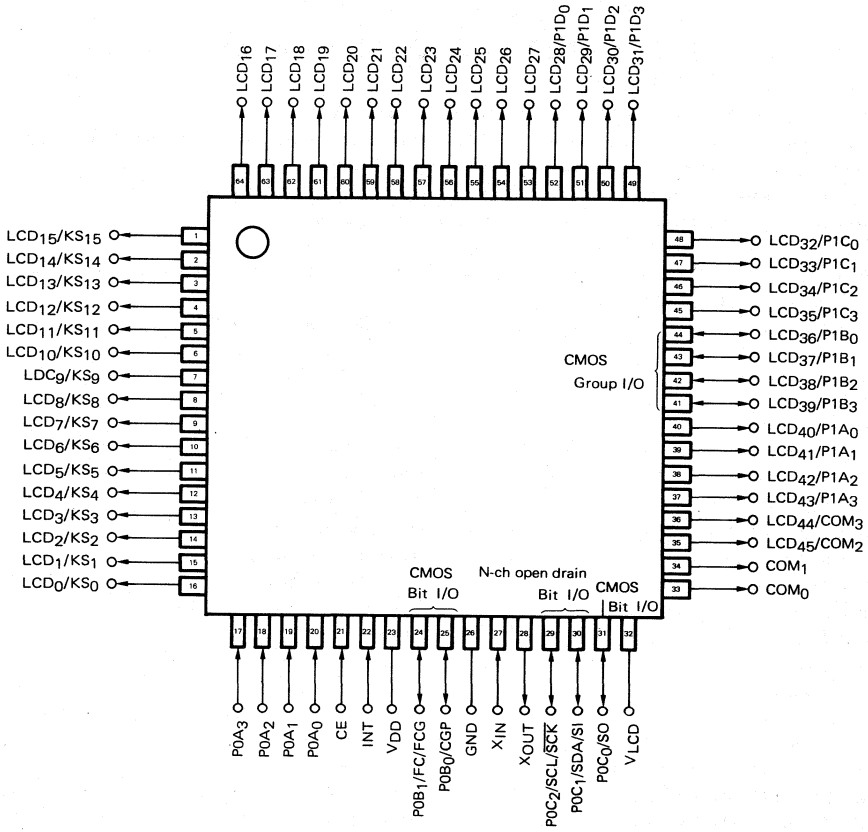
NEC provides easy-to-use tools for μPD17106 system development: in-circuit emulator (IE-17K) and assembler (AS17K).

*:under development

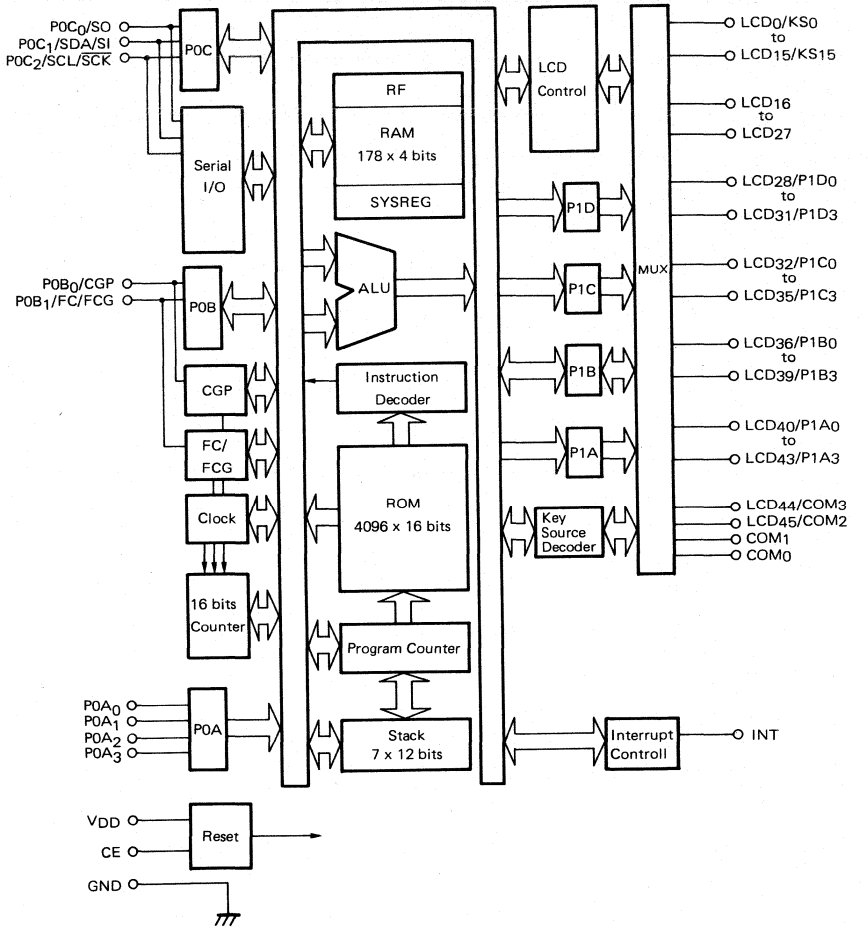
Features

- 4-bit microcontroller for front panel control
- Program memory (ROM):
  8K bytes (4096 steps x 16bits)
- General-purpose data memory (RAM):
  178 nibbles (178 nibbles x 4 bits)
- Instruction executionn time:
  4.44μs (using a 4.5MHz crystal oscillator)
- Stack level: 7
- Easy 46-instruction set
- Decimal operation possible
- Table reference possible
- Built-in LCD driver
  Static : 46 x 1= 46 segments
  1/2 duty, 1/2 bias : 46 x 2= 92 segments
  1/3 duty, 132 bias: 45 x 3= 135 segments
  1/4 duty, 1/4 bias : 44 x 4= 176 segments
- Built-in key source decoder
  16 lines (Output by time division with LCD segment signal)
- Built-in 16-bit counter providing four functions
  Timer modulo
  Frequency counter
  Pulse width counter
  CGP (clock generator port)
- Built-in 8-bit serial interface
  Two 1-system channels (2- or 3-wire type)
- Interrupt
  - External interrupt : 1 channel (INT pin)
  - Internal interrupt : 2 channels
    (timer and serial interface)
- General-purpose I/O ports
  - Input/output ports : 5 lines (+4: segment pin)
  - Input ports : 4 lines (built-in pull-up resistor)
  - Output ports : 0 line (+12: segment pins.8 out of 12 allows LED direct drive.)
- Built-in power-on reset, CE reset, and power failure detection circuit
- Low-power consumption CMOS
- Power-supply voltage: 5 V ±10%
- 64-pin plastic QFP

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



FRONT PANEL CONTROLLER (FPC) WITH ON-CHIP ONE TIME PROM

μPD17P106

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P106 is a 4-bit single-chip CMOS microcontroller with on-chip ONE TIME PROM, for use in front panel control.

The CPU uses the μPD17000 architecture, which allows direct data memory manipulation and various operations with a single instructionand peripheral hardware control. Moreover, all instrustions are one 16-bit word in lenght.

In addition to a wide range of input/output ports, serial interface, and clock generator port, on chip peripheral hardware includes, for front panel control, an LCD driver, key source decoder, and remote control decoding timer, enabling high-performance front panel systems of various kinds to be configured.

As the μPD17P106 includes on-chip ONE TIME PROM,it is ideal for system evaluation in program development for the μPD17106* mask ROM version, or for small-volume production.

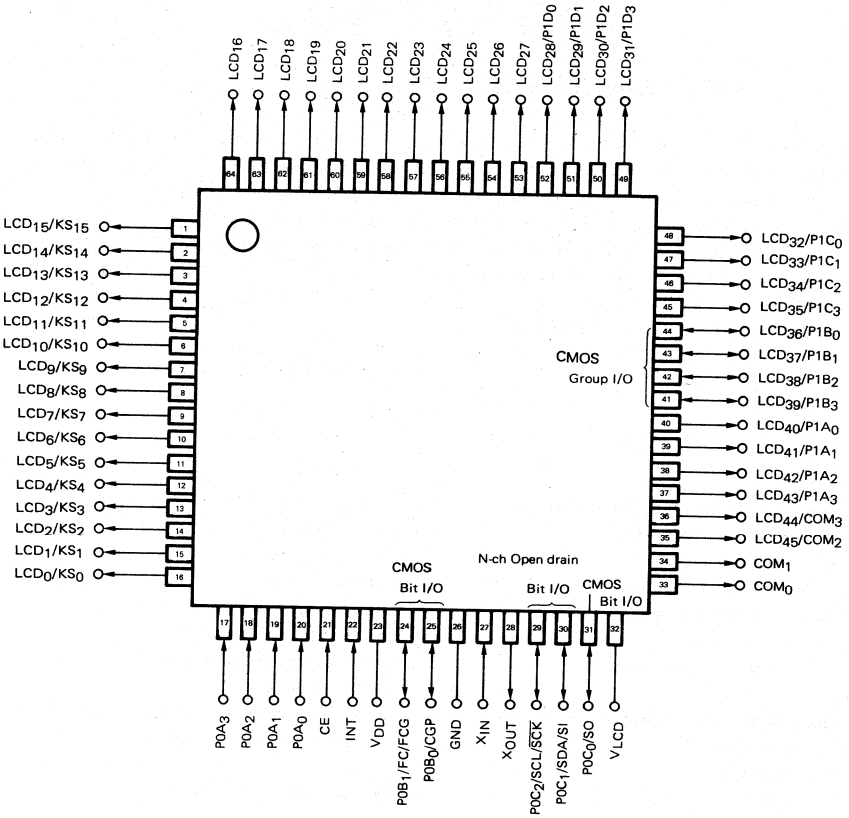
An easy-to-use in-circuit emulator (IE-17K) and assembler (AS17K) are available as μPD17P106 system development tools.

*:under development

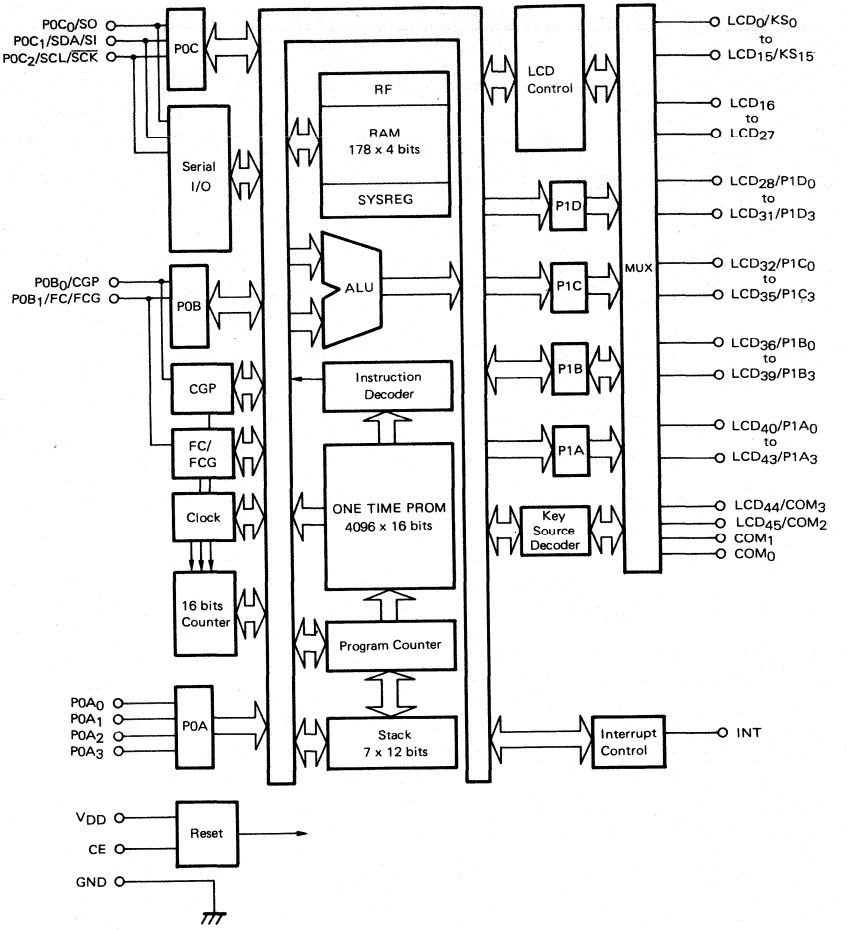
Features

- 4-bit microcontroller for front panel controller use
- Program memory (ONE TIME PROM):
  8K bytes (4096 steps x 16bits)
- General-purpose data memory (RAM):
  178 nibbles (178 nibbles x 4 bits)
- Instruction executionn time:
  4.44μs (using a 4.5MHz crystal oscillator)
- Stack levels: 7
- Easy-to-understand instructiion set (46 instructions)
- Decimal operation capability
- Table reference capability
- On-chip LCD driver
  Static : 46 x 1= 46 segments
  1/2 duty, 1/2 bias : 46 x 2= 92 segments
  1/3 duty, 132 bias: 45 x 3= 135 segments
  1/4 duty, 1/4 bias : 44 x 4= 176 segments
- On-chip key source decoder
- 16 lines (Output by time-division multiplexing with LCD segment signal)
- On-chip 16-bit counter with 4 functions:
  Timer modulo
  Frequency count
  Pulse width count
  CGP (clock generator port)
- On-chip 8-bit serial interface
  1 system 2 channels (2-wire and 3-wire)
- Variety of interrupts
  External interrupts : 1 channel (INT pin)
  Internal interrupts : 2 channels
  (timer, serial interface)
- General input/output ports
  - Input/output ports : 5 lines (+4: Segment pins)
  - Input ports : 4 lines (with internal pull-up resistor)
  - Output ports : 0 (+12: segment pins, 8 with LED direct drive capability.)
- Power-on reset, CE reset, and power failure detection circuit on chip
- Low-power consumption CMOS
- Supply voltage : 5 V ±10%
- 64-pin plastic QFP
- Mask ROM version : μPD17106

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17103, tiny microcontroller, consists of 512 × 16 bit ROM, 16 × 4 bit RAM, and 11 I/O ports.

The 17K architecture of the CPU uses general-purpose registers so that data memory can be manipulated directly for effective porgramming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM): 512 words × 16 bits
- Data memory (RAM): 16 words × 4 bits
- Input/output ports: 11 ports (including 3 N-ch open-drain outputs)
- Instruction execution time: 2 μs (when the 8 MHz crystal or ceramic resonator is used)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function (with the STOP and HALT instructions)
- Data memory can retain data on low voltage (2.0 V at MIN.)
- An oscillator for the system clock (for crystal or ceramic resonator)
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

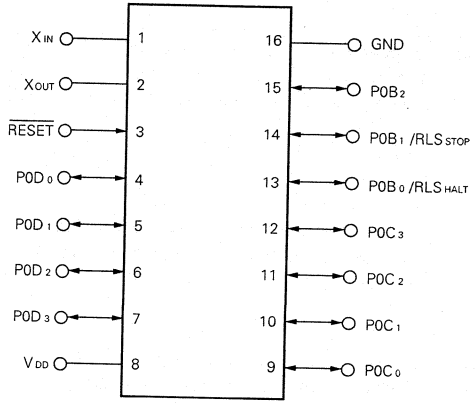
- Controlling electric appliances or toys

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17103CX-xxx	16-pin plastic DIP (300 mil)	Standard
μPD17103GS-xxx	16-pin plastic SOP (300 mil)	Standard

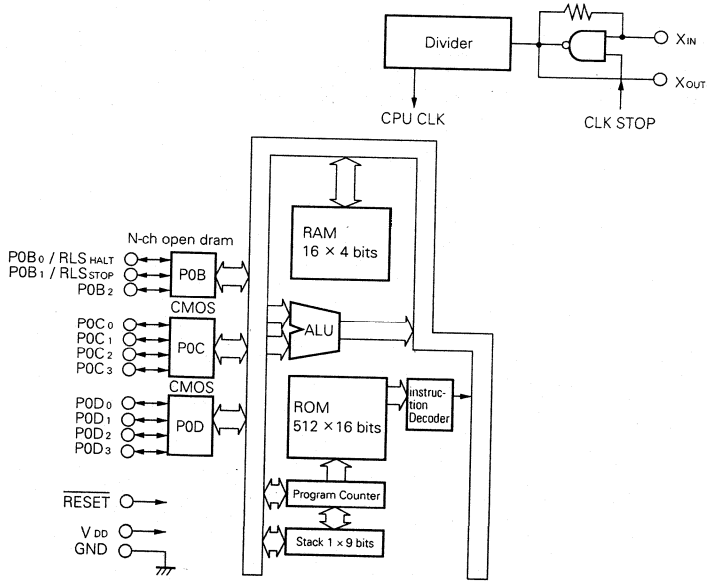
PIN CONFIGURATION (Top View)

μPD17103CX, μPD17103GS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM of the μPD17103



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

Pin name	I/O	Function	Reset
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor selected: High Level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A built-in pull-up resistor can be mask-selected bit by bit. • 9 V in open-drain mode	
$P0C_0$-$P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$-$P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

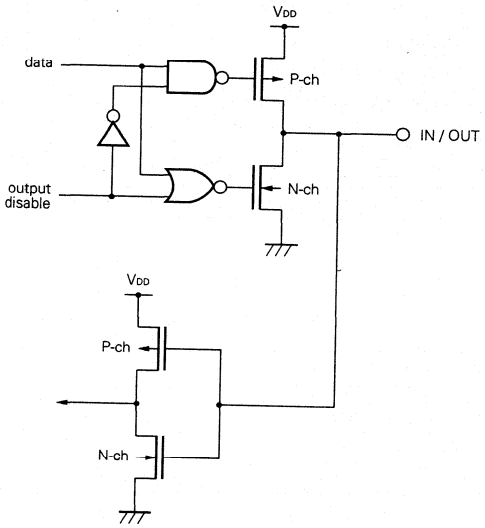
Pin name	I/O	Function
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be mask-selected.
V_{DD}		• Positive power supply pin
GND		• GND pin
X_{IN}, X_{OUT}		• Pins to be connected to the system clock resonator

I/O: Input/Output

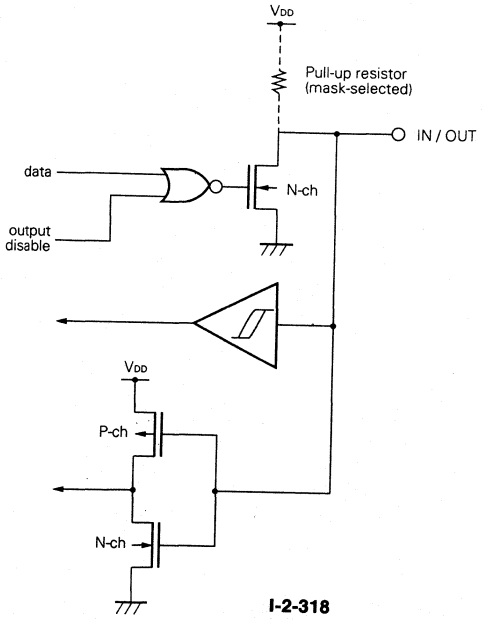
EQUIVALENT CIRCUITS OF PINS

The following are the diagrams of the equivalent circuits of the μPD17103 pins. Part of each circuit diagram has been simplified.

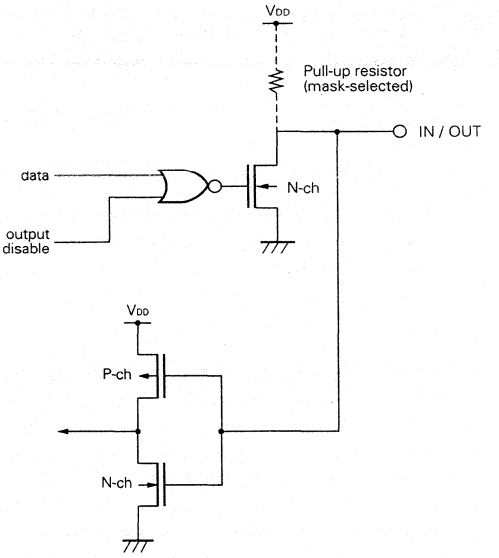
(1) P0C and P0D



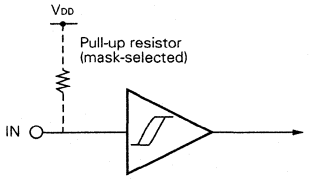
(2) P0B0 and P0B1



(3) $P0B_2$



(4) $\overline{\text{RESET}}$

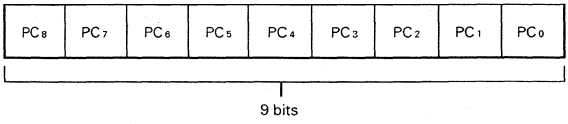


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER

As shown in Fig. 1-1, the program counter is a 9-bit binary counter.

Fig. 1-1 Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

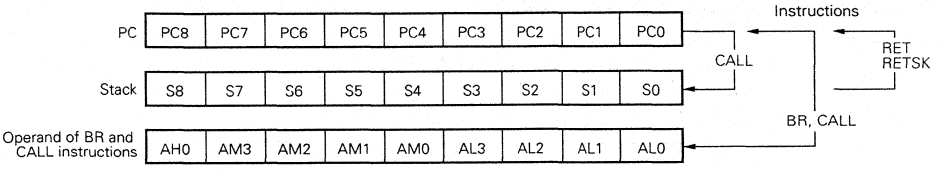
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17103 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

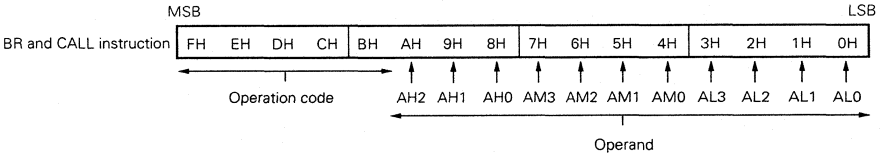
Fig. 2-1 shows the relationship between the PC, the stack, and the operand of BR and CALL instructions.

Fig. 2-1 Relationship between the PC, the Stack, and the Operand of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leq n \leq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-Bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leq n \leq 8$) denotes a stack.

Reset input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the program memory (ROM) configuration.

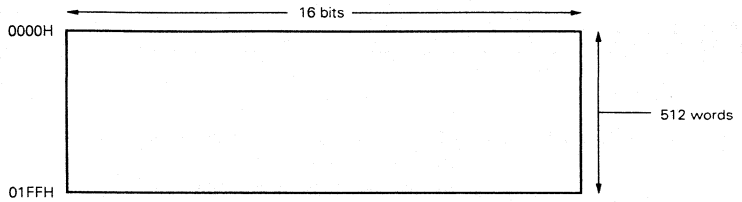
As shown in the figure, the program memory has 512 words by 16 bits.

The program memory has been addressed in units of 16 bits. The addresses 0000H to 01FFH are specified by the program counter (PC).

Every instruction is a 1 word long, consisting of 16 bits. One instruction can therefore be stored at one address in program memory.

Address 0000H is used as a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

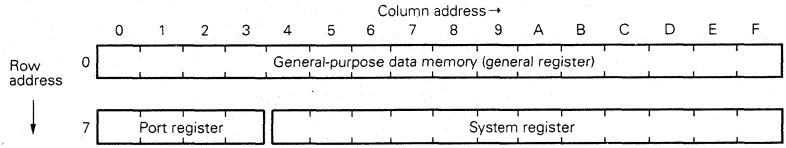
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into 3 blocks as shown below: General-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation and comparison, evaluation, and transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17103 register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

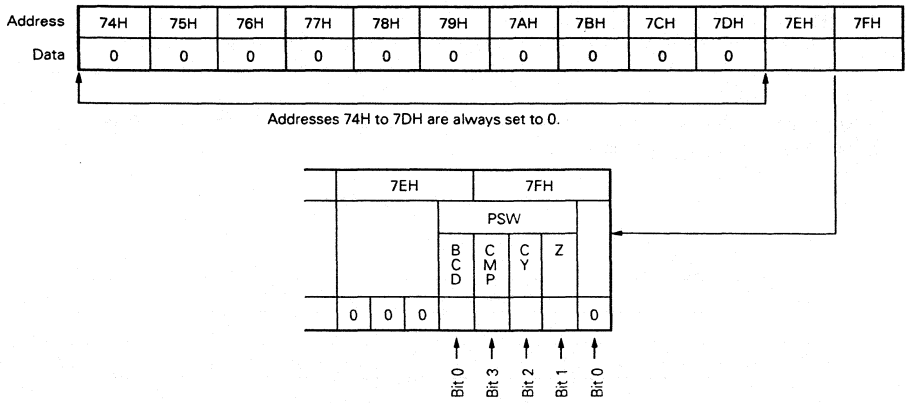
The port register is used to set output data or to read the input data of input/output ports.

Once data are written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicate the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17103.

Fig. 4-2 System Register Map

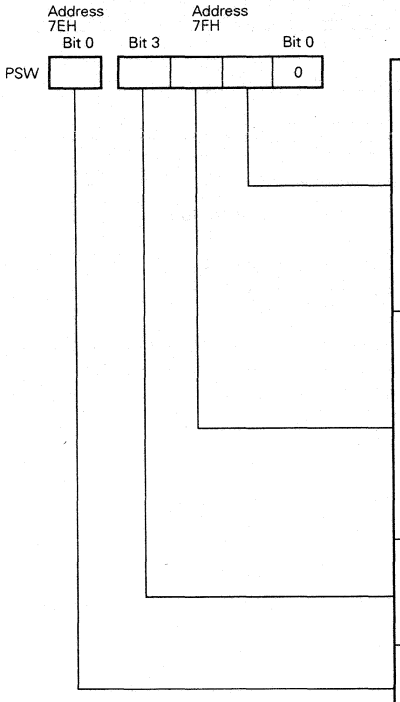


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the CY flag is mapped in bit 2, and the Z flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general-purpose registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0	0	0
Memory manipulation sets the Z flag to 1	1	1
Arithmetic operation results in a non-zero value	0	0
Arithmetic operation results in 0	1	Zn-1

Remark Zn – 1: The Z flag value present immediately before arithmetic operation.

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the CY flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the Z flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is made. If it is less than zero, a borrow is made. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is made. If it is less than 0, a borrow is made. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0B ($P0B_0$/RLS_{HALT}, $P0B_1$/RLS_{STOP}, $P0B_2$)

Port 0B is a 3-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of port 0B are placed in the output mode to continue to output written data. The data is retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port 0B consists of 4 bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17103 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (See **7. STANDBY FUNCTIONS**)

6.2 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port 0C are placed in the output mode to continue to output written data. The data is retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.3 PORT 0D ($P0D_0$ to $P0D_3$)

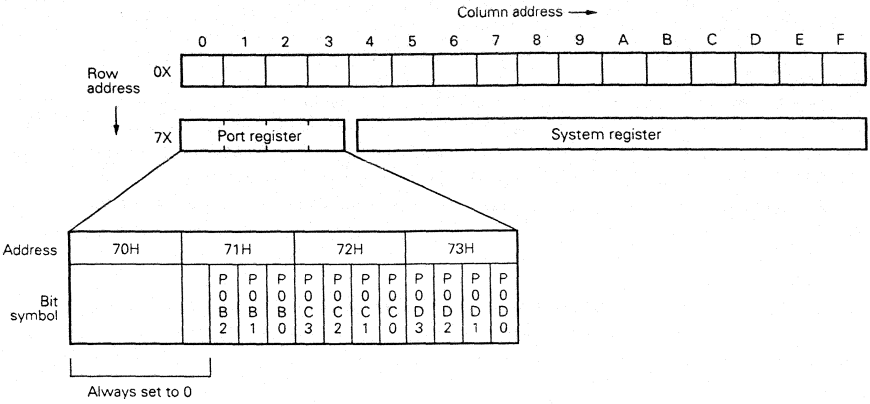
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.4 RECOMMENDED CONDITIONS FOR UNUSED μPD17103 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports 0B to 0D	Connect to V_{DD} or GND
Output mode	CMOS ports (ports 0C and 0D)	Open
	N-ch open-drain port (port 0B)	

7. STANDBY FUNCTIONS

The μPD17103 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting/Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

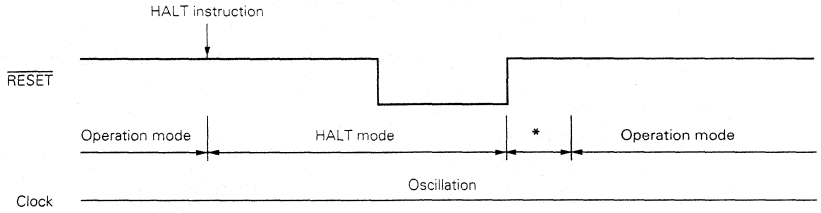
Table 7-2 Setting/Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
  At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

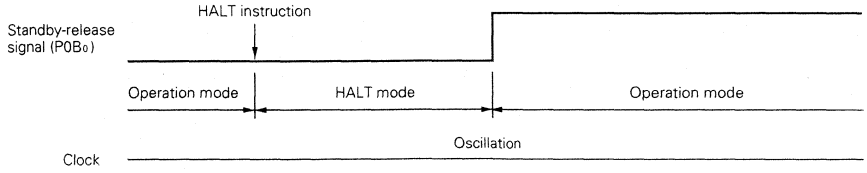
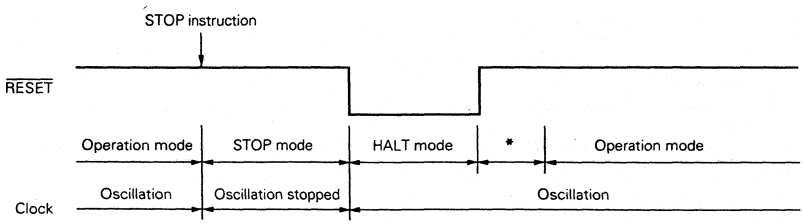


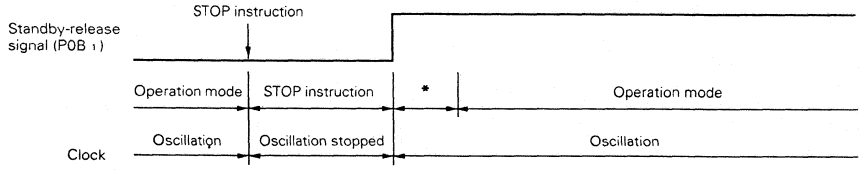
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0B to 0D	71H to 73H	Data is retained. All pins are placed in the input mode.

9. RESERVED WORDS USED IN ASSEMBLY LANGUAGE

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17103 must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17103.OPT file in AS17103 (device file for the μPD17103) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is as follows.

Only the two pseudo instructions listed in Table 9-1 can be coded in the block.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

9 .1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the pseudo instructions to define mask options of each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand
$P0B_2$-$P0B_0$	OPTP0B	3	P0BPLUP (pull-up resistor provided) OPEN (no pull-up resistor provided)
$\overline{RESET}$	OPRTES	1	RESPLUP (pull-up resistor provided) OPEN (no pull-up resistor provided)

The coding format of OPTP0B is as follows. To define the mask option, specify $P0B_2$ (first operand), $P0B_1$, and $P0B_3$ in the operand field.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is as follows.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	($\overline{\text{RESET}}$)	[;comment]

Example The following mask options are set in a μPD17103 source file to be assembled:

$P0B_2$: Pull-up $P0B_1$: Open
$P0B_0$: Open $\overline{\text{RESET}}$: Pull-up

```
                    ⋮
;17103
 Setting mask options: OPTION
                       OPTP0B   P0BPLUP,  OPEN,  OPEN
                       OPTRES   RESPLUP
                       ENDOP
                    ⋮
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17103 device file (AS17103).

Table 9-2 Reserved Symbols

Name	Attribute	Value	R / W	Description
P0B0	FLG	0.71H.0	R / W	Bit 0 of port 0B
P0B1	FLG	0.71H.1	R / W	Bit 1 of port 0B
P0B2	FLG	0.71H.2	R / W	Bit 2 of port 0B
P0B3[Note]	FLG	0.71H.3	R	Always set to 0
P0C0	FLG	0.72H.0	R / W	Bit 0 of port 0C
P0C1	FLG	0.72H.1	R / W	Bit 1 of port 0C
P0C2	FLG	0.72H.2	R / W	Bit 2 of port 0C
P0C3	FLG	0.72H.3	R / W	Bit 3 of port 0C
P0D0	FLG	0.73H.0	R / W	Bit 0 of port 0D
P0D1	FLG	0.73H.1	R / W	Bit 1 of port 0D
P0D2	FLG	0.73H.2	R / W	Bit 2 of port 0D
P0D3	FLG	0.73H.3	R / W	Bit 3 of port 0D
BCD	FLG	0.7EH.0	R / W	BCD arithmetic flag
PSW	MEM	0.7FH	R / W	Program status word
Z	FLG	0.7FH.1	R / W	Zero flag
CY	FLG	0.7FH.2	R / W	Carry flag
CMP	FLG	0.7FH.3	R / W	Compare flag

R / W: Read / write

Note Although P0B3 does not exist in the μPD17103, it is defined as a read-only flag so that it is treated as a dummy bit when a built-in macro is used.

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14}–b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #i
0001	1	SUB	r, m	SUB	m, #i
0010	2	ADDC	r, m	ADDC	m, #i
0011	3	SUBC	r, m	SUBC	m, #i
0100	4	AND	r, m	AND	m, #i
0101	5	XOR	r, m	XOR	m, #i
0110	6	OR	r, m	OR	m, #i
0111	7	REC RETSK RORC STOP HALT NOP	 r s h 		
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #i	SKGE	m, #i
1010	A				
1011	B	SKNE	m, #i	SKLT	m, #i
1100	C	BR	addr	CALL	addr
1101	D			MOV	m, #i
1110	E			SKT	m, #n
1111	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M : One of data memory
m : Data memory address specified by [mH, mL] of each bank
mH : Data memory address high (row address); 3 bits
mL : Data memory address low (column address); 4 bits
R : One of general register specified by [(RP), r]
r : General register address low (column address); 4 bits
RP : General register pointer
PC : Program counter
SP : Stack pointer
STACK : Stack specified by (SP)
i : Immediate data; 4 bits
n : Bit position; 4 bits
addr : One of program memory address; 11 bits
aH : Program memory address high; 3 bits
aM : Program memory address middle; 4 bits
aL : Program memory address low; 4 bits
CY : Carry flag
CMP : Compare flag
s : Stop release condition
h : Halt release condition
[ ] : Address of M, R
( ) : Contents of M, R

Instructions	Mnemonic	Operand	Function	Operation	Machine code			
					OP code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R ← (R) + (M)	00000	mH	mL	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	mH	mL	i
	ADDC	r, m	Add memory to register with carry	R ← (R) + (M) + (CY)	00010	mH	mL	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	mH	mL	i
Subtract	SUB	r, m	Subtract memory from register	R ← (R) – (M)	00001	mH	mL	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	mH	mL	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	mH	mL	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	mH	mL	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M – i, skip if zero	01001	mH	mL	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M – i, skip if not borrow	11001	mH	mL	i
	SKLT	m, #i	Skip if memory less than immediate data	M – i, skip if borrow	11011	mH	mL	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M – i, skip if not zero	01011	mH	mL	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	mH	mL	i
		r, m	Logica AND of register and memory	R ← (R) AND (M)	00100	mH	mL	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	mH	mL	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	mH	mL	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	mH	mL	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	mH	mL	r
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	mH	mL	r
	ST	m, r	Store register of memory	(M) ← R	11000	mH	mL	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	mH	mL	i

Instructions	Mnemonic	Operand	Function	Operation	Machine code			
					OP code	3 bits	4 bits	4 bits
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if Mn = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if Mn = all "0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry.	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) – 1, STACK ← ((PC) + 1), PC ← ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}				−0.3 to +7.0	V
Input Voltage	V_I	P0C, P0D, $\overline{RESET}$			−0.3 to V_{DD} +0.3	V
		P0B		*1	−0.3 to V_{DD} +0.3	V
				*2	−0.3 to +11	V
		P0C, P0D			−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	P0B		*1	−0.3 to V_{DD} +0.3	V
				*2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C or P0D			−5	mA
		Total of all pins			−15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C or P0D			30	mA
		Total of all pins			100	mA
Operating Temperature	T_{opt}				−40 to +85	°C
Storage Temperature	T_{stg}				−65 to +150	°C
Power Consumption Power	P_d	Ta = 85 °C	16-pin plastic DIP		400	mW
			16-pin plastic SOP		190	

*1 When the use of the internal pull-up resistors is specified by the mask options

*2 When the use of the internal pull-up resistors is not specified by the mask options

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
I/O Capacitance	C_{IO}			15	pF	

I/O: Input/output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note 1**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note 2**
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0C, P0D	
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.2 V_{DD}	V	P0B	
High-Level Ouput Voltage	V_{OH1}	V_{DD} −2.0			V	P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
	V_{OH2}	V_{DD} −1.0			V	P0C, P0D I_{OH} = −200 μA	
Low-Level Ouput Voltage	V_{OL1}			2.0	V	P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
	V_{OL2}			0.5	V	P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} Note 1
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V Note 2
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} Note 1
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9V Note 2
Low-Level Output Leakage Curent	I_{LOL}			−5	μA	P0B, P0C, P0D, V_{OUT} = 0 V	
Pull-Up Resistor for Pin $\overline{RESET}$	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor for Pin P0B	R_{P0B}	5	15	30	kΩ		
Power Supply Current Note 3	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD} = 5 V ±10%, f_{CC} = 8 MHz
			250	750	μA	Operation mode	V_{DD} = 3 V ±10%, f_{CC} = 2 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD} = 5 V ±10%, f_{CC} = 8 MHz
			200	600	μA	HALT mode	V_{DD} = 3 V ±10%, f_{CC} = 2 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10%
			0.1	5	μA	STOP mode	V_{DD} = 3 V ±10%

Note 1. When the use of the internal pull-up resistors is specified by the mask options
2. When the use of the internal pull-up resistors is not specified by the mask options
3. This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	t_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/Low Level Width On $P0B_0$ and $P0B_1$	t_{PBH} t_{PBL}	10			μs	
High/Low Level Width On $\overline{RESET}$	t_{RSH} t_{RSL}	10			μs	

Remark t_{CY} = 16/fcc (fcc: frequency of the system clock oscillator)

CHARACTERISTICS OF THE OSCILLATOR (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CONSTANT	CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITION
Ceramic resonator		Oscillator frequency	0.49		2.04	MHz	V_{DD} = 2.7 to 6.0 V
			0.49		5.00	MHz	V_{DD} = 4.0 to 6.0 V
			0.49		8.16	MHz	V_{DD} = 4.5 to 6.0 V
Crystal resonator		Oscillation stability time (ceramic resonator)			4	ms	After V_{DD} reaches the minimum of the oscillation volatage range

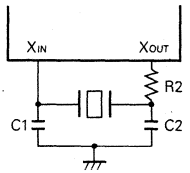
RECOMMENDED CERAMIC RESONATORS

MANUFACTURER	PART NAME	RECOMMENDED CONSTANTS			OSCILLATION VOLTAGE RANGE [V]	
		C1 [pF]	C2 [pF]	R2 [kΩ]	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSB500E	100	100	6.8	2.7	6.0
	CSA2.00MG	30	30	0	2.7	6.0
	CSA4.00MG	30	30	0	4.0	6.0
	CSA8.00MT	30	30	0	4.5	6.0
Toko, Inc.	CRK500	47	47	8.2	2.7	6.0
	CRHB4.00M	27	27	0	4.0	6.0
	CRHB8.00M	27	27	0	4.5	6.0

RECOMMENDED CRYSTAL RESONATORS

MANUFACTURER	PART NAME	RECOMMENDED CONSTANTS			OSCILLATION VOLTAGE RANGE [V]	
		C1 [pF]	C2 [pF]	R2 [kΩ]	MIN.	MAX.
Kinseki Co., Ltd.	HC-49/u 2 MHz	27	27	0	2.7	6.0
	HC-49/u 4 MHz	27	27	0	4.0	6.0
	HC-49/u 8 MHz	24	24	0	4.5	6.0

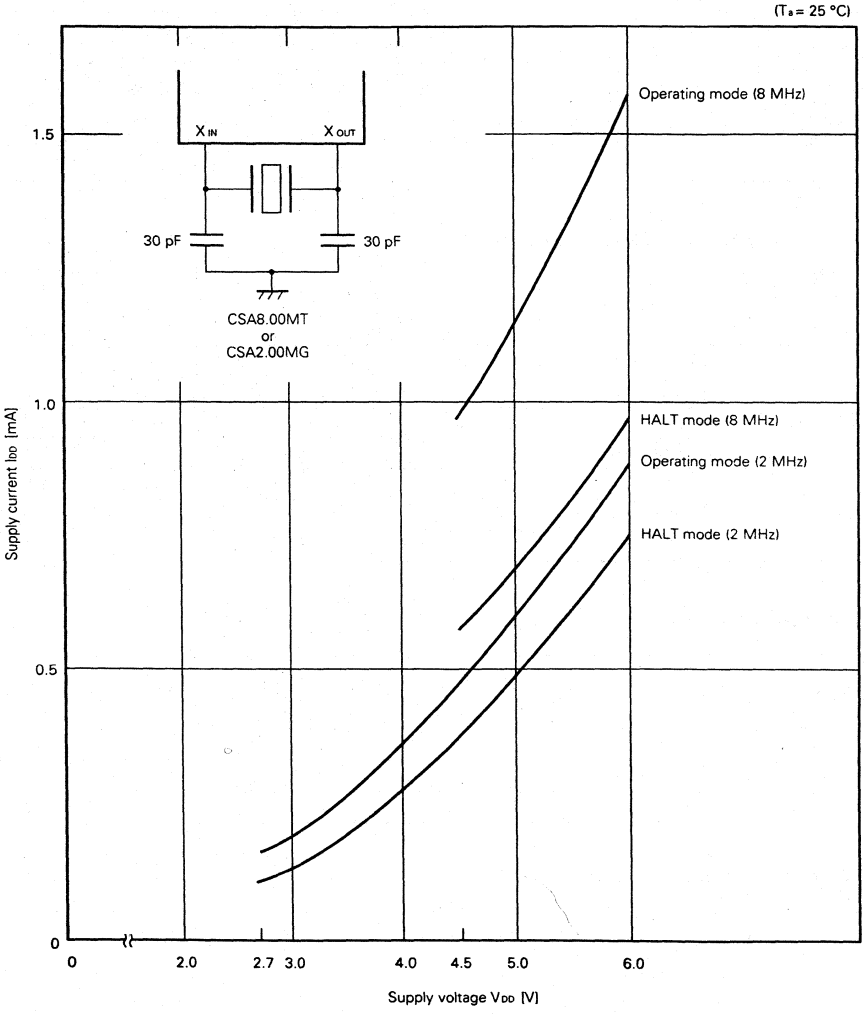
Example of connection



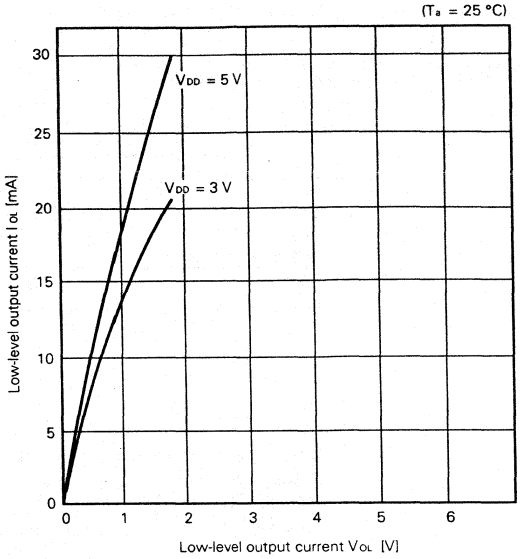
12. CHARACTERISTIC CURVES

I_{DD} vs. V_{DD}

(T_a = 25 °C)

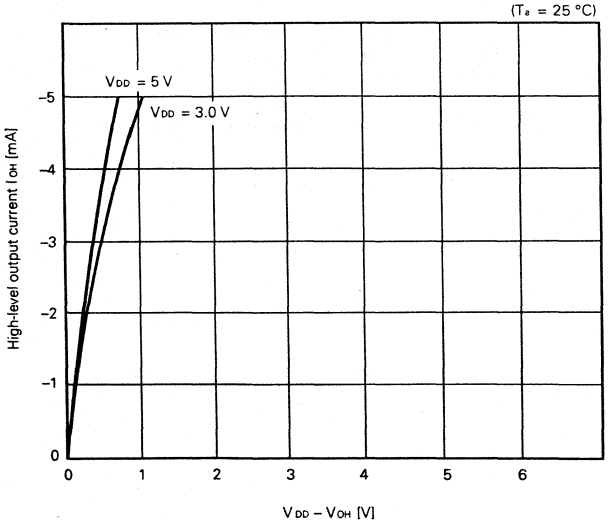


I_{OL} vs. V_{OL}



Note **The maximum absolute rating is 30 mA per pin.**

I_{OH} vs. (V_{DD} - V_{OH})

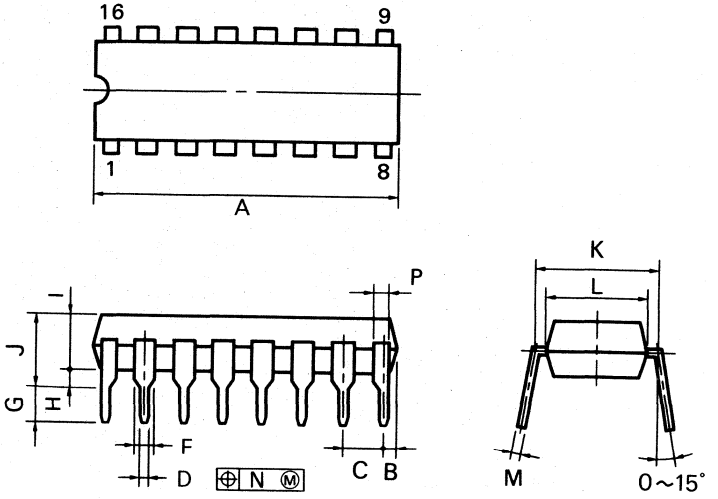


Note **The maximum absolute rating is –5 mA per pin.**

Remark Every characteristic curve indicates the reference values.

13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

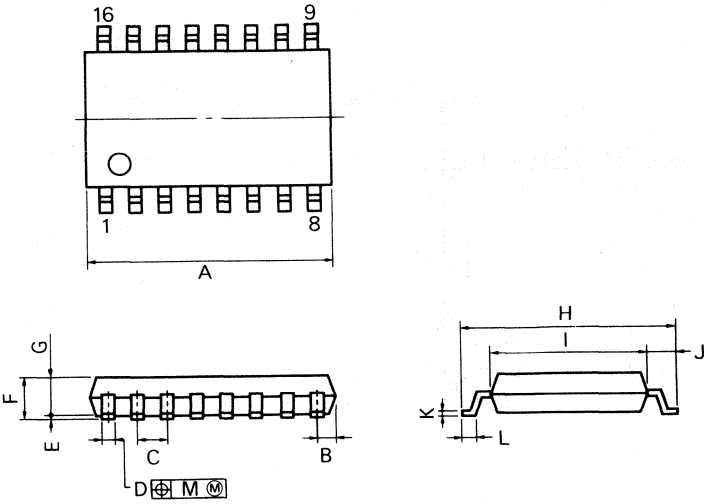
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



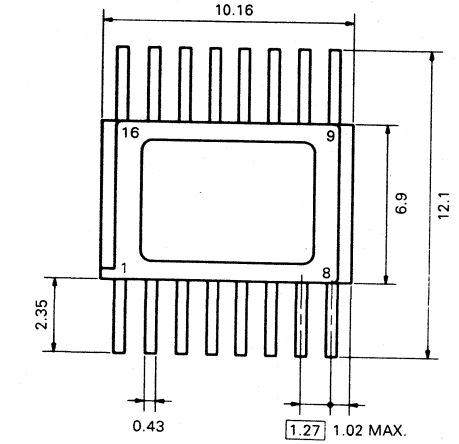
P16GM-50-300B-1

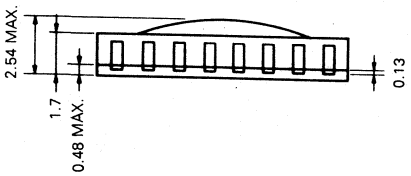
NOTE

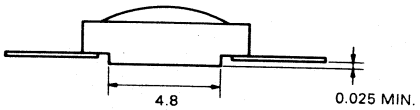
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

PACKAGE DIMENSIONS OF THE 16-PIN CERAMIC SOP FOR ES (reference) (Unite: mm)

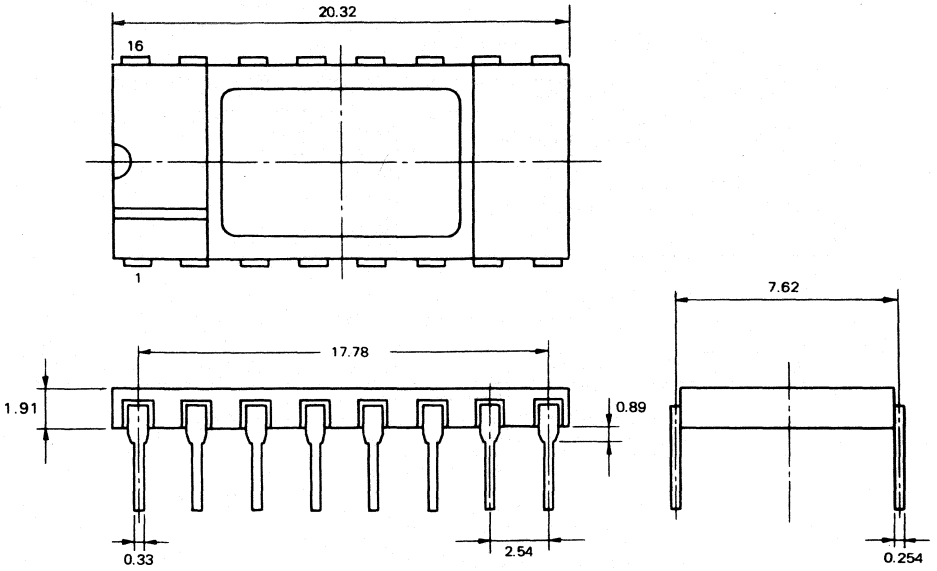






X16B-50B

PACKAGE DIMENSIONS OF THE 16-PIN CERAMIC DIP FOR ES (reference) (Unite: mm)



14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17103.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product name	Package	Symbol
μPD17103CX-xxx	16-pin plastic DIP (300 mil)	• Wave soldering • Partial heating method
μPD17103GS-xxx	16-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering Process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Thermal temperature: 300 °C or below Flow timer: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remarks For details of the recommended soldering conditions for surface mount type products, refer to out document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of Input/ Output Port Pins*	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System Clock	Ceramic/crystal oscillation				RC oscillation			
Power Supply Voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM Version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the numbe of input/output port pins selectable between N-ch opn-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17104, tiny microcontroller, consist of 512 × 16 bit ROM, 16 × 4 bit RAM, and 16 input/output ports.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is one word long, consisting of 16 bits.

FEATURES

- Program memory (ROM) : 512 words × 16 bits
- Data memory (RAM) : 16 words × 4 bits
- Input/output ports : 16 ports (including 4 N-ch open-drain outputs)
- Instruction execution time : 2 μs (when the 8 MHz crystal or ceramic resonator is used)
- Number of instructions : 24 (Each instruction is one word long.)
- Stack level : 1
- A standby function : (with the STOP and HALT instructions)
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator for the system clock (for crystal or ceramic resonator)
- Operating supply voltage : 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

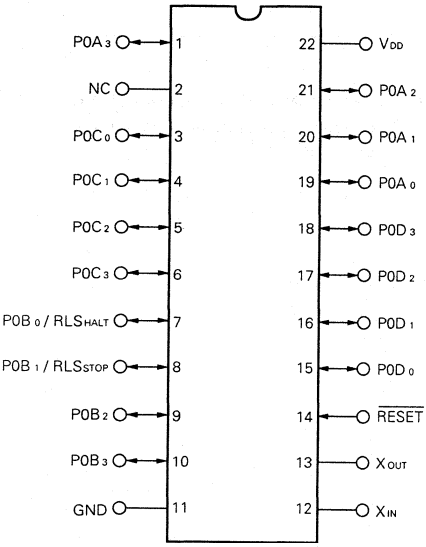
- Controlling electric appliances or toys

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17104CS-xxx	22-pin plastic shrink DIP (300 mil)	Standard
μPD17104GS-xxx	24-pin plastic SOP (300 mil)	Standard

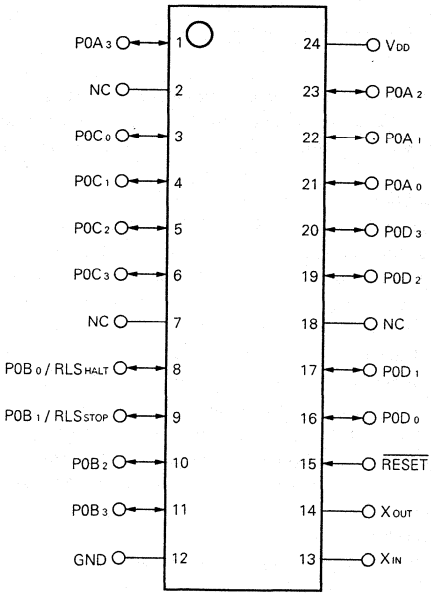
PIN CONFIGURATION (Top View)

μPD17104CS



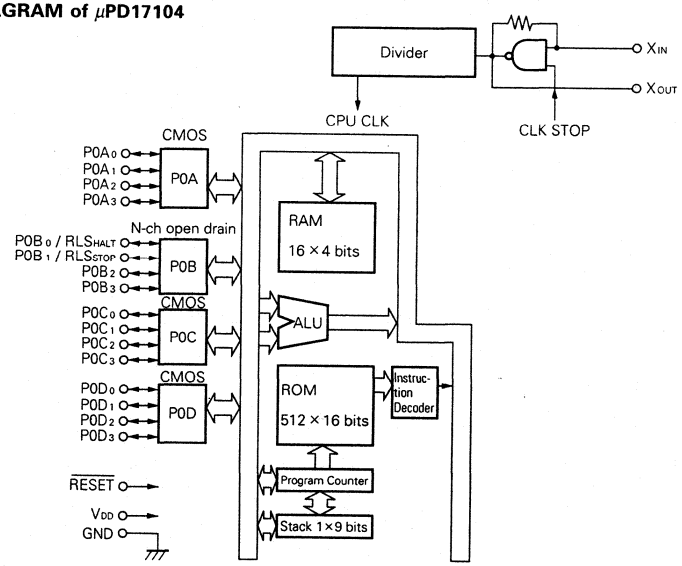
22-pin plastic shrink DIP

μPD17104GS

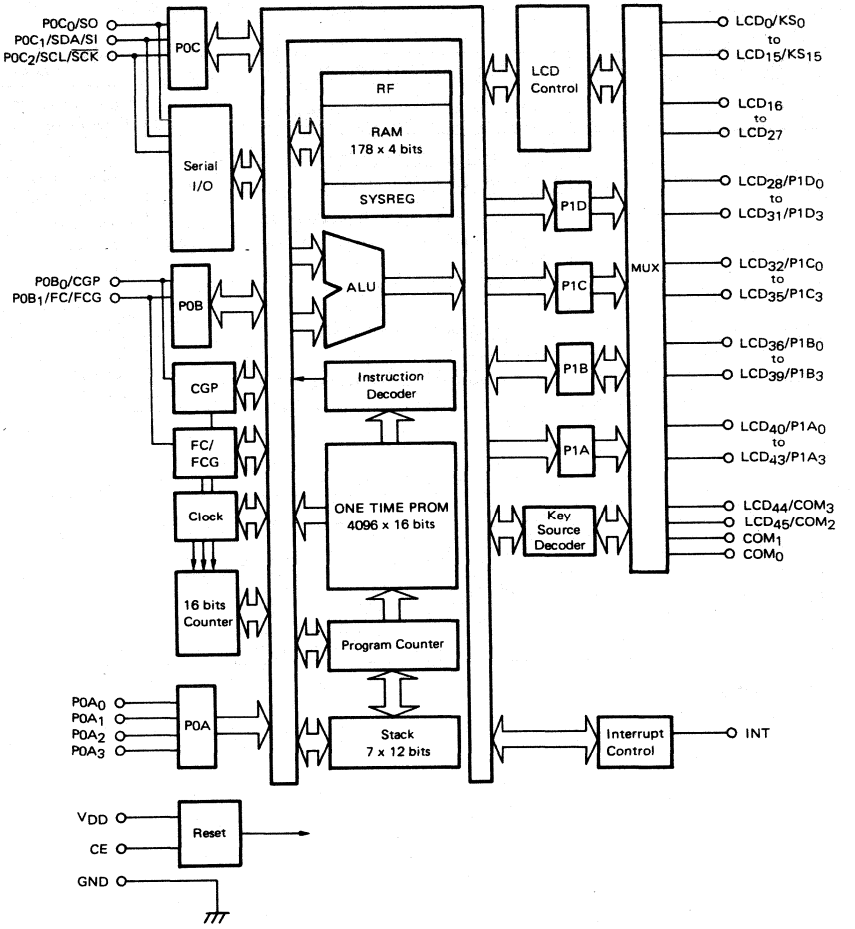


24-pin plastic SOP

BLOCK DIAGRAM of μPD17104



BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

PIN NAME	I/O	FUNCTION	RESET
$P0A_0$ to $P0A_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0A)	High impedance (input mode)
$P0B_0$/RLSHALT	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor selected: High level (input mode)
$P0B_1$/RLSSTOP		For releasing the STOP mode	
$P0B_2$, $P0B_3$		• N-ch open-drain 4-bit I/O port (port 0B) • A built-in pull-up resistor can be mask-selected bit by bit. • 9 V in open-drain mode	
$P0C_0$ - $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ - $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

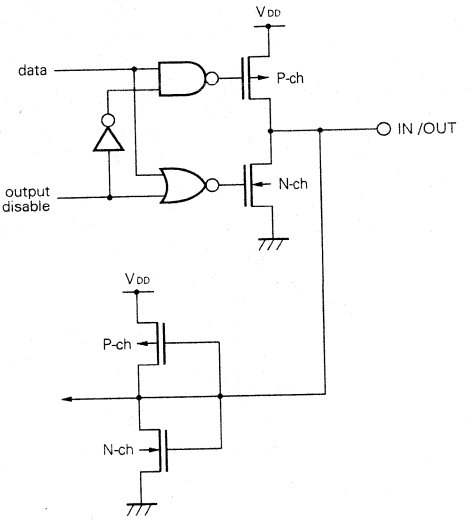
Pin name	I/O	Function
$\overline{\text{RESET}}$	Input	• System reset input pin • A built-in pull-up resistor can be mask-selected.
V_{DD}		• Positive power supply pin
GND		• GND pin
X_{IN}, X_{OUT}		• Pins to be connected to the system clock resonator

I/O: Input/output

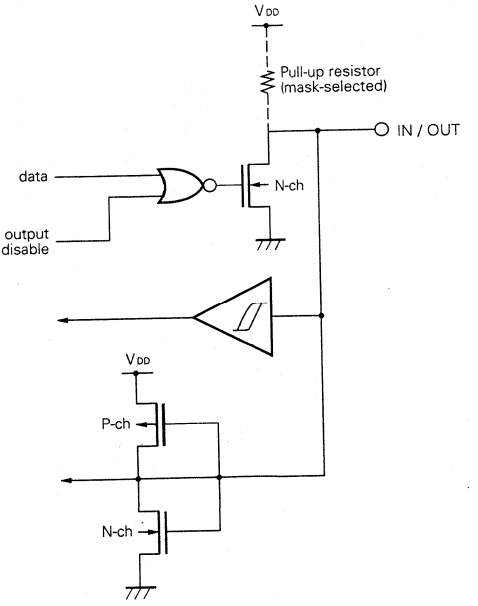
EQUIVALENT CIRCUITS OF PINS

The following are the diagrams of the equivalent circuits of the μPD17104 pins. Part of each circuit diagram has been simplified.

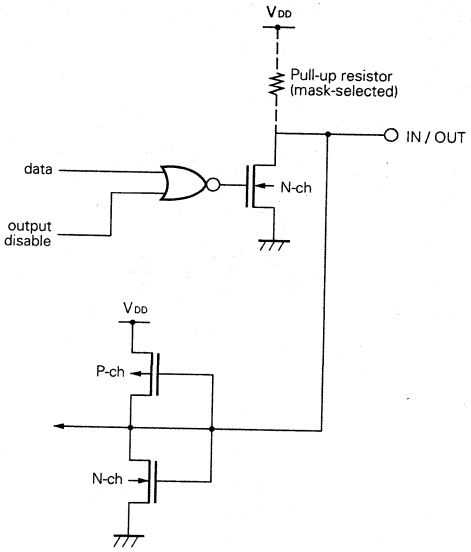
(1) P0A, P0C and P0D



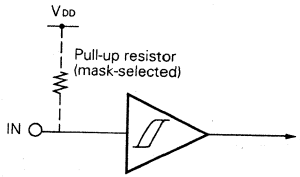
(2) P0B0 and P0B1



(3) $P0B_2$ and $P0B_3$



(4) $\overline{\text{RESET}}$

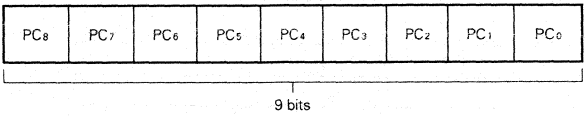


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER

As shown in Fig. 1-1, the program counter is a 9-bit binary counter.

Fig. 1-1 Program Counter



1.2 Functions of the Program Counter (PC)

The program counter specifies the address of a program memory (ROM) or a program.

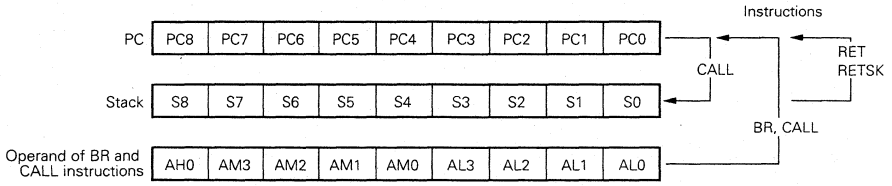
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specificd.

2. STACK

Stack of the μPD17104 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

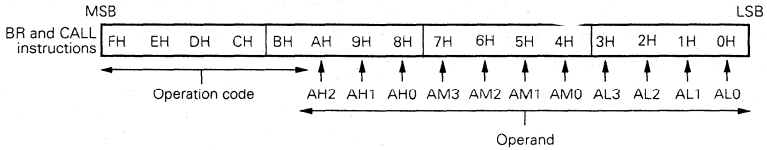
Fig. 2-1 shows the relationship between the PC, the stack, and the operand of BR and CALL instructions.

Fig. 2-1 Relationship between the PC, the Stack, and Operand of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leq n \leq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-Bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leq n \leq 8$) denotes a stack.

Reset input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows thc program memory (ROM) configuration.

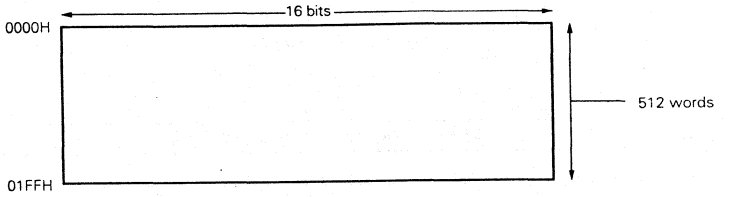
As shown in the figure, the program memory has 512 words by 16 bits.

The program memory has been addressed in units of 16 bits. The addresses 0000H to 01FFH are specified by the program counter (PC) .

Every instruction is one word long, consisting of 16 bits. One instruction can therefore be stored at one address in program memory.

Address 0000H is used as a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

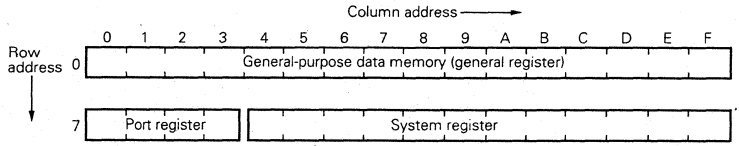
4.1 Format of the Data Memory (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of four bits, or "one nibble," and an address is assigned to each 4 bits of data. The three high-order bits are called the "row address," and the four low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: General-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data memory

The general -purpose data memory is a part of the data memory from which the system register.(SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a four-bit arithmetic operation and comparison, evaluation, and transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Function of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17104 register pointer is always set to 0, the general-purpose data memory is also used as general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

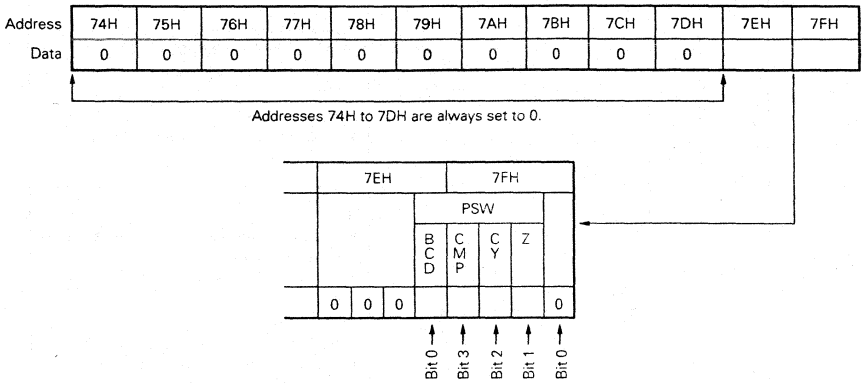
The port register is used to set output data or to read the input data input/output ports.

Once data are written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicate the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17104.

Fig. 4-2 System Register Map

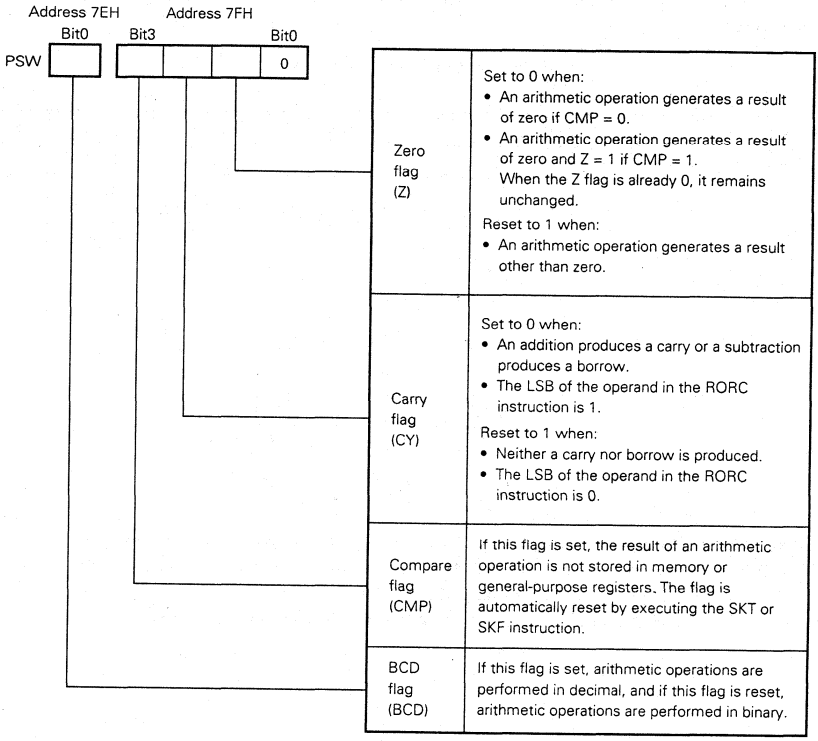


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the CY flag is mapped in bit 2, and the Z flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0	0	0
Memory manipulation sets the Z flag to 1	1	1
Arithmetic operation results in a non-zero value	0	0
Arithmetic operation results in 0	1	Z_{n-1}

Remark Z_{n-1}: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the CY flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the Z flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is made. If it is less than zero, a borrow is made. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is made. If it is less than 0, a borrow is made. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0A ($P0A_0$ to $P0A_3$)

Port 0A is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 70H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0A are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.2 PORT 0B ($P0B_0$/RLS_{HALT} P0BI/RLS_{STOP}, $P0B_2$, $P0B_3$)

Port 0B is a four-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch opendrain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of port 0B are placed in the output mode to continue to output written data. The data is retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

When the μPD17104 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (See **7. STANDBY FUNCTIONS**)

6.3 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a four-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port 0C are placed in the output mode to continue to output written data. The data is retained unless new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.4 PORT 0D (P0D0 to P0D3)

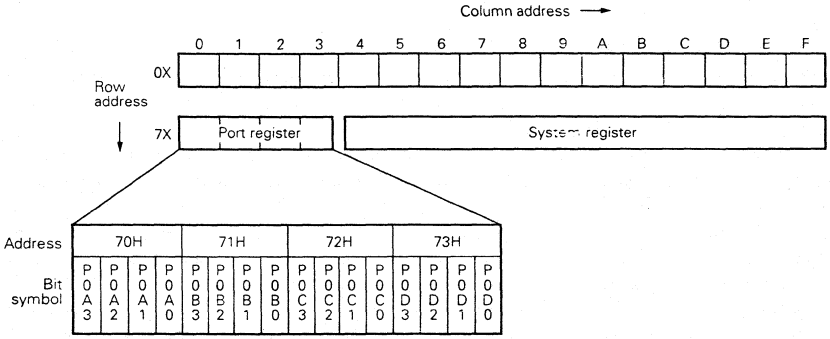
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data are written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data are written to the register.

Whenever the port register is read, the read data indicate the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.5 RECOMMENDED CONDITIONS FOR UNUSED μPD17104 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports 0A to 0D	Connect to VDD or GND.
Output mode	CMOS ports (ports 0A, 0C and 0D)	Open
	N-ch open-drain port (port 0B)	

7. STANDBY FUNCTIONS

The μPD17104 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting/Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

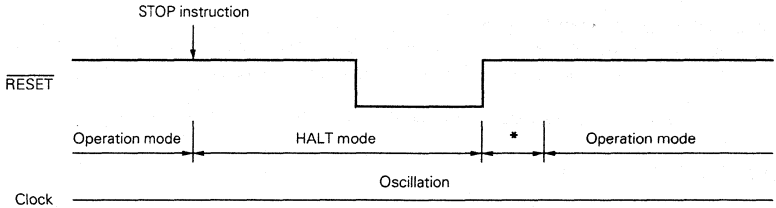
Table 7-2 Setting/Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the P0B1 pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

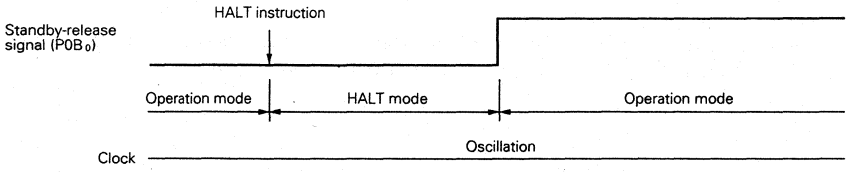
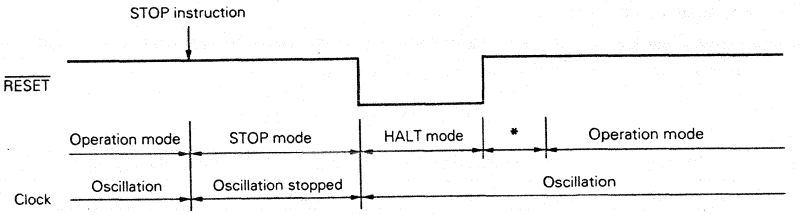


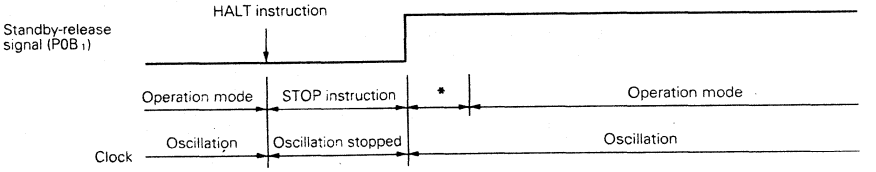
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0A to 0D	70H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. RESERVED WORDS USED IN ASSEMBLY LANGUAGE

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17104 must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17104. OPT file in AS17104 (device file for the μPD17104) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is as follows.

Only the two pseudo instructions listed in Table 9-1 can be coded in the block.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the pseudo instructions to define mask options of each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand
$P0B_3$ to $P0B_0$	OPTP0B	4	P0BPLUP (pull-up resistor provided) OPEN (no pull-up resistor provided)
$\overline{RESET}$	OPTRES	1	RESPLUP (pull-up resistor provided) OPEN (no pull-up resistor provided)

The coding format of OPTP0B is as follows. To define the mask option, specify $P0B_3$ (first operand), $P0B_2$, $P0B_1$, and $P0B_0$ in the operand field.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_3$), ($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is as follows.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	($\overline{\text{RESET}}$)	[;comment]

Example The following mask options are set in a μPD17104 source file to be assembled:

$P0B_3$: Pull-up $P0B_2$: Pull-up $P0B_1$: Open
$P0B_0$: Open $\overline{\text{RESET}}$: Pull-up

```
                    ⋮
; 17104
  Setting mask options:   OPTION
                          OPTP0B   P0BPLUP, P0BPLUP, OPEN, OPEN
                          OPTRES   RESPLUP
                          ENDOP
                    ⋮
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17104 device file (AS17104).

Table 9-2 Reserved Symbols

Name	Attribute	Value	R / W	Description
P0A0	FLG	0.70H.0	R / W	Bit 0 of port 0A
P0A1	FLG	0.70H.1	R / W	Bit 1 of port 0A
P0A2	FLG	0.70H.2	R / W	Bit 2 of port 0A
P0A3	FLG	0.70H.3	R / W	Bit 3 of port 0A
P0B0	FLG	0.71H.0	R / W	Bit 0 of port 0B
P0B1	FLG	0.71H.1	R / W	Bit 1 of port 0B
P0B2	FLG	0.71H.2	R / W	Bit 2 of port 0B
P0B3	FLG	0.71H.3	R / W	Bit 3 of port 0B
P0C0	FLG	0.72H.0	R / W	Bit 0 of port 0C
P0C1	FLG	0.72H.1	R / W	Bit 1 of port 0C
P0C2	FLG	0.72H.2	R / W	Bit 2 of port 0C
P0C3	FLG	0.72H.3	R / W	Bit 3 of port 0C
P0D0	FLG	0.73H.0	R / W	Bit 0 of port 0D
P0D1	FLG	0.73H.1	R / W	Bit 1 of port 0D
P0D2	FLG	0.73H.2	R / W	Bit 2 of port 0D
P0D3	FLG	0.73H.3	R / W	Bit 3 of port 0D
BCD	FLG	0.7EH.0	R / W	BCD arithmetic flag
PSW	MEM	0.7FH	R / W	Program status word
Z	FLG	0.7FH.1	R / W	Zero flag
CY	FLG	0.7FH.2	R / W	Carry flag
CMP	FLG	0.7FH.3	R /W	Compare flag

R / W: Read / write

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14} - b_{11} BIN	HEX	b_{15} = 0		b_{15} = 1	
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M : One of data memory
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (row address); 3 bits
m_L : Data memory address low (column address); 4 bits
R : One of general register specified by [(RP), r]
r : General register address low (column address); 4 bits
RP : General register pointer
PC : Program counter
SP : Stack pointer
STACK : Stack specified by (SP)
i : Immediate data; 4 bits
n : Bit position; 4 bits
addr : One of program memory address; 11 bits
a_H : Program memory address high; 3 bits
a_M : Program memory address middle; 4 bits
a_L : Program memory address low; 4 bits
CY : Carry flag
CMP : Compare flag
s : Stop release condition
h : Halt release condition
[ ] : Address of M, R
( ) : Contents of M, R

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to resister with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r ,m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M – i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M – i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M – i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M – i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register of memory	(M) ← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if Mn = all "0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) − 1, STACK ← ((PC)+1), PC ←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionally	PC ← (STACK), SP ← (SP)+1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, or P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, or P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin plastic shrink DIP	400	mW
			24-pin plastic SOP	250	

Note 1. When the use of the internal pull-up resistors is specified by the mask options

2. When the use of the internal pull-up resistors is not specified by the mask options

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
I / O Capacitance	C_{IO}			15	pF	

I / O: Input / Output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note 1**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note 2**
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0C, P0D	
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$	
	V_{IL3}	0		0.2 V_{DD}	V	P0B	
High-Level Output Voltage	V_{OH1}	V_{DD} −2.0			V	P0A, P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
	V_{OH2}	V_{DD} − 1.0			V	P0A, P0C, P0D I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL1}			2.0	V	P0A, P0C, P0D, V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
	V_{OL2}			0.5	V	P0A, P0B, P0C, P0D, I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0A, P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 1**
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V **Note 2**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0A, P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0A, P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 1**
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V **Note 2**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, V_{OUT} = 0 V	
Pull-Up Resistor for Pin $\overline{\text{RESET}}$	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor for Pin P0B	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note 3**	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD} = 5 V ±10 %, f_{CC} = 8 MHz
			250	750	μA	Operation mode	V_{DD} = 3 V ±10 %, f_{CC} = 2 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD} = 5 V ±10 %, f_{CC} = 8MHz
			200	600	μA	HALT mode	V_{DD} = 3 V ±10% f_{CC} = 2MHz
	I_{DD3}		0.1	1.0	μA	STOP mode	V_{DD} = 5 V ±10 %
			0.1	5	μA	STOP mode	V_{DD} = 3 V ±10 %

Note 1. When the use of the internal pull-up resistors is specified by the mask option
2. When the use of the internal pull-up resistors is not specified by the mask option
3. This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	t_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/low Level Width on $P0B_0$ and $P0B_1$	t_{PBH} t_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	t_{RSH} t_{RSL}	10			μs	

Remark $t_{CY} = 16/f_{CC}$ (f_{CC}: frequency of the system clock oscillator)

CHARACTERISTICS OF THE OSCILLATOR (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	MIN	TYP.	MAX.	UNIT	CONDITION
Ceramic Resonator		Oscillator Frequency	0.49		2.04	MHz	V_{DD} = 2.7 – 6.0 V
			0.49		5.00	MHz	V_{DD} = 4.0 – 6.0 V
			0.49		8.16	MHz	V_{DD} = 4.5 – 6.0 V
Crystal Resonator		Oscillation Stability Time (ceramic resonator)			4	ms	After V_{DD} reaches the minimum of the oscillation voltage range

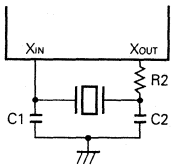
RECOMMENDED CERAMIC RESONATORS

MANUFACTURER	PART NUMBER	RECOMMENDED CONSTANTS			OSCILLATION VOLTAGE RANGE [V]	
		C1 [pF]	C2 [pF]	R2 [kΩ]	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSB500E	100	100	6.8	2.7	6.0
	CSA2. 00MG	30	30	0	2.7	6.0
	CSA4. 00MG	30	30	0	4.0	6.0
	CSA8. 00MT	30	30	0	4.5	6.0
Toko, Inc .	CRK500	47	47	8.2	2.7	6.0
	CRHB4. 00M	27	27	0	4.0	6.0
	CRHB8. 00M	27	27	0	4.5	6.0

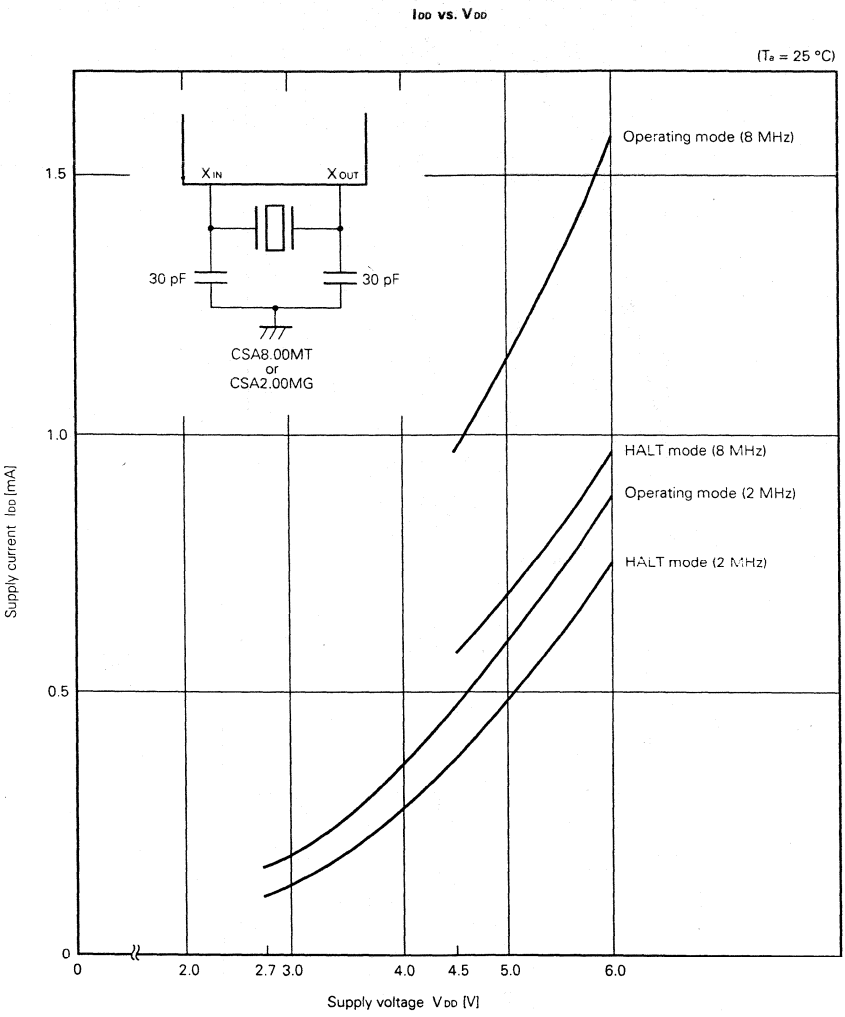
RECOMMENDED CRYSTAL RESONATORS

MANUFACTURER	PART NUMBER	RECOMMENDED CONSTANTS			OSCILLATION VOLTAGE RANGE [V]	
		C1 [pF]	C2 [pF]	R2 [kΩ]	MIN.	MAX.
Kinseki Co., Ltd.	HC-49/u 2 MHz	27	27	0	2.7	6.0
	HC-49/u 4 MHz	27	27	0	4.0	6.0
	HC-49/u 8 MHz	24	24	0	4.5	6.0

Example of connection

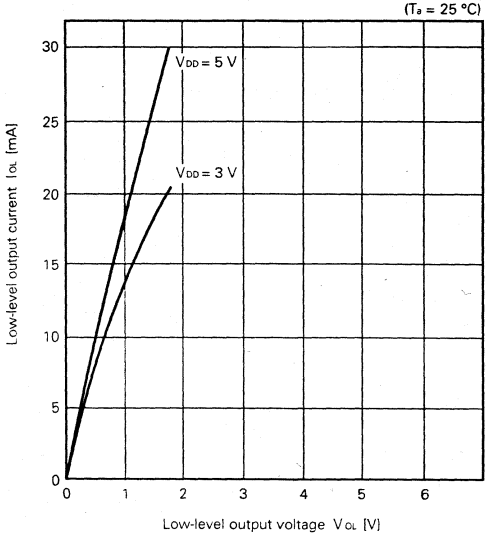


12. CHARACTERISTICS CURVE



I_{OL} vs. V_{OL}

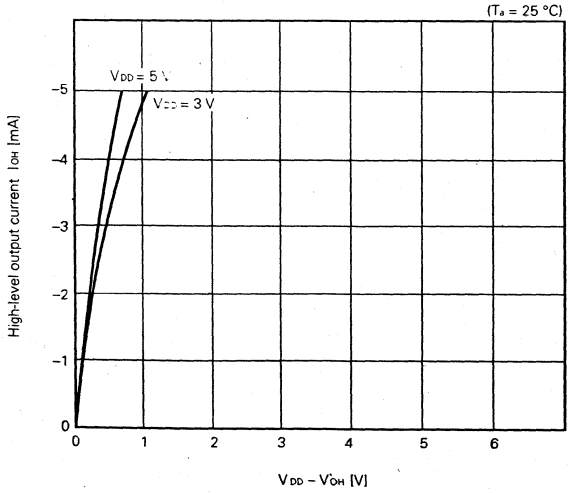
(T_a = 25 °C)



Note **The maximum absolute rating is 30 mA per pin.**

I_{OH} vs. (V_{DD} – V_{OH})

(T_a = 25 °C)

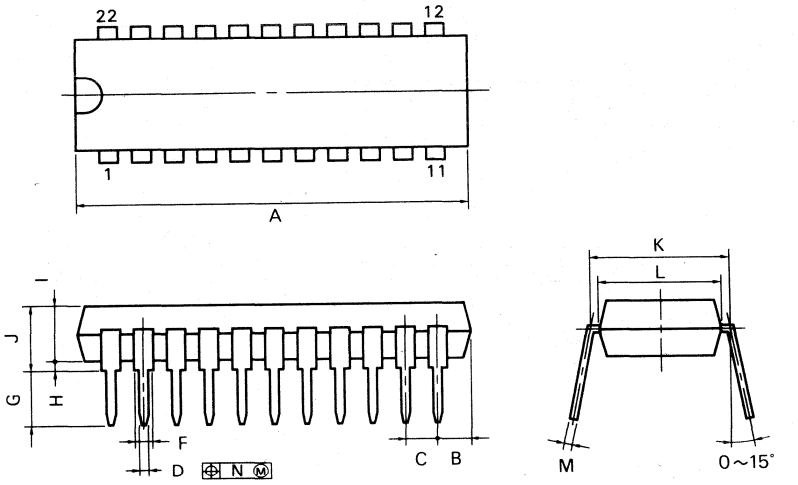


Note **The maximum absolute rating is –5 mA per pin.**

Remark Every characteristic curve indicates the reference values.

13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-300B

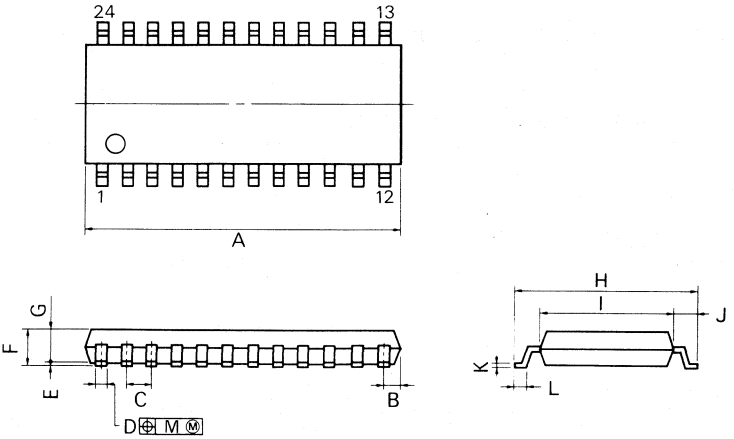
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



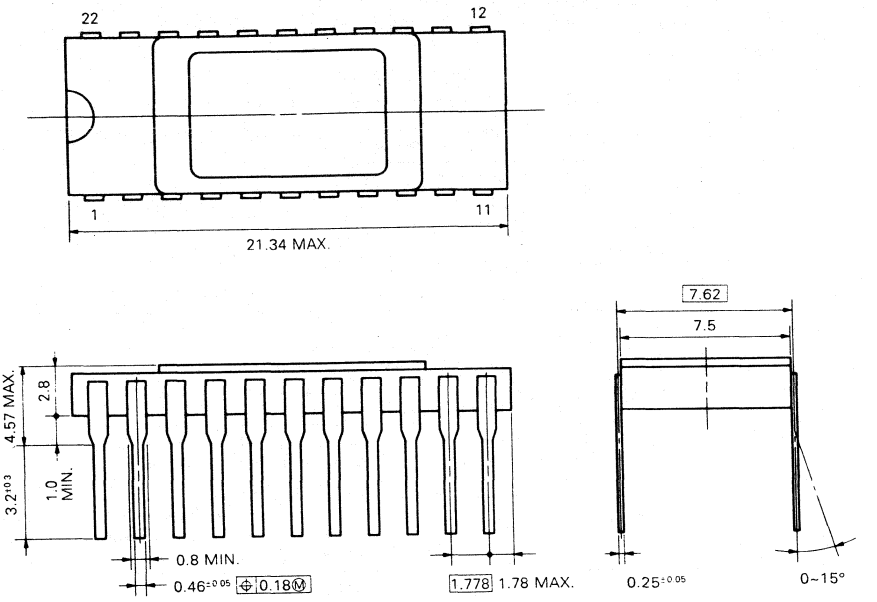
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

Package dimensions of the 22-pin ceramic of shrink DIP for ES (300 mil) (Unit: mm)



P22D-70-300B

14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17104.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

PRODUCT	PACKAGE	SYMBOL
μPD17104CS-xxx	22-pin plastic shrink DIP (300 mil)	• Wave soldering • Partial heating method
μPD17104GS-xxx	24-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

SYMBOL	SOLDERING PROCESS	SOLDERING CONDITIONS
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial Heating Method	Partial heating method	Thermal temperature: 300 °C or below Flow time: 10 seconds or below
Wave Soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions for surface mount type device, refer to our document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of input/ output port pins*	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the number of input/output port pins selectable between N-ch open-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17103L is a tiny microcontroller consisting of a ROM (512 × 16 bits), RAM (16 × 4 bits), and 11 input/output ports. The functions and pins of the μPD17103L are compatible with those of the μPD17103.

The μPD17103L can operate at the low voltage (1.8 V min.). It can be used for wide variety of products controlled by one lithium battery or two dry cells.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM) : 512 words × 16 bits
- Data memory (RAM) : 16 × 4 bits
- Input/output ports : 11 ports (including 3 N-ch open-drain outputs)
- Instruction execution time : 8 μs (with 2 MHz crystal or ceramic resonator used)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function : STOP and HALT modes
- Data memory can retain data on low voltage (1.5 V min.).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage : 1.8 to 3.6 V (at 2 MHz)

APPLICATIONS

- Controlling electric appliances or toys

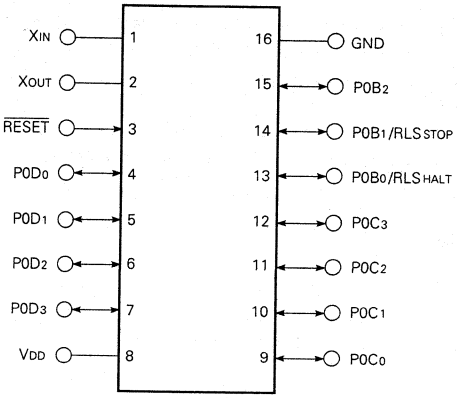
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17103LCX-xxx	16-pin plastic DIP (300 mil)	Standard
μPD17103LGS-xxx	16-pin plastic SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

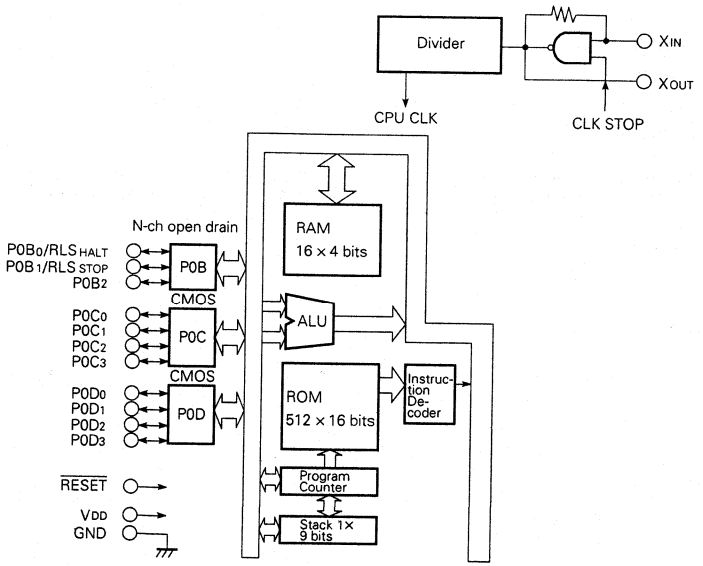
PIN CONFIGURATION (Top View)

μPD17103LCX, μPD17103LGS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM of μPD17103L



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	I/O	Function	Reset
$P0B_0$/RLSHALT	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLSSTOP		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0C_0$ - $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ - $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

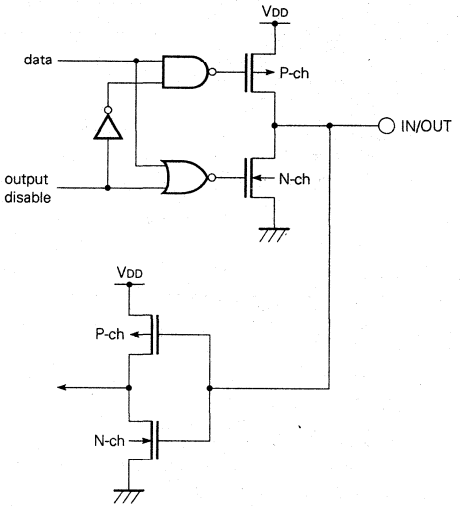
Pin name	I/O	Function
$\overline{\text{RESET}}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).
V_{DD}		• Positive power supply pin
GND		• GND pin
X_{IN}, X_{OUT}		• Pins to be connected to the system clock resonator

I/O: Input/output

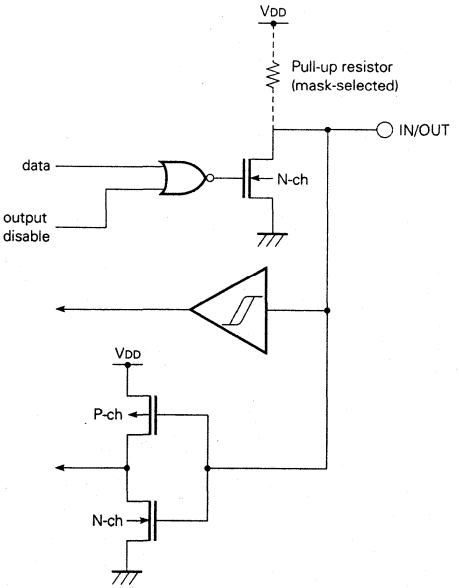
PIN EQUIVALENT CIRCUITS

Following are schematics of the equivalent circuits of the pins of the μPD17103L.

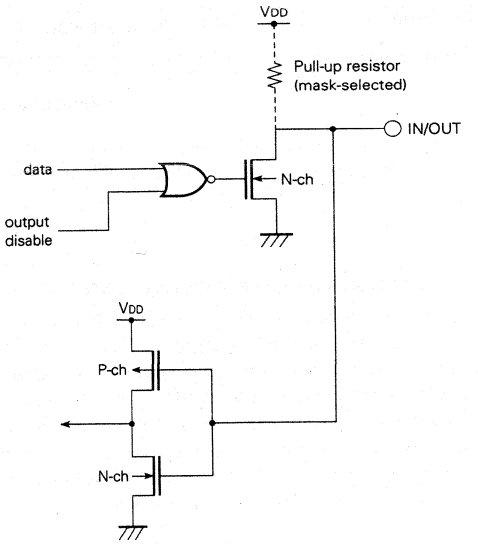
(1) P0C and P0D



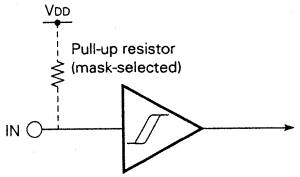
(2) P0B0 and P0B1



(3) $P0B_2$



(4) $\overline{\text{RESET}}$

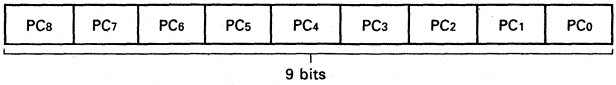


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

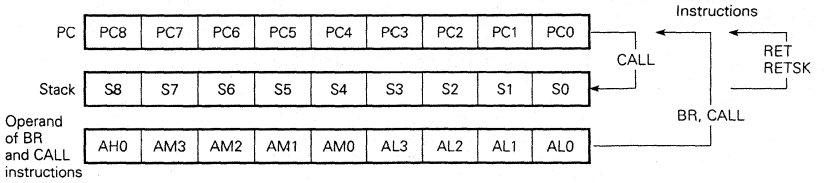
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17103L is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

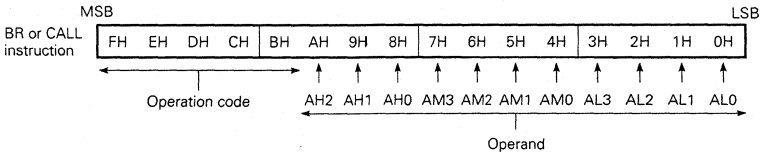
Fig. 2-1 shows the relationship between PC, stack, and operands of BR and CALL instructions.

Fig. 2-1 Relationship between PC, Stack, and Operands of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leqq n \leqq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leqq n \leqq 8$) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

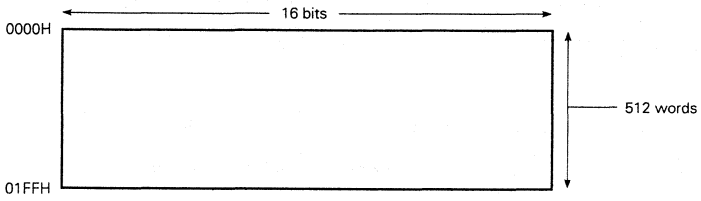
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory (ROM).

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory (RAM) stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

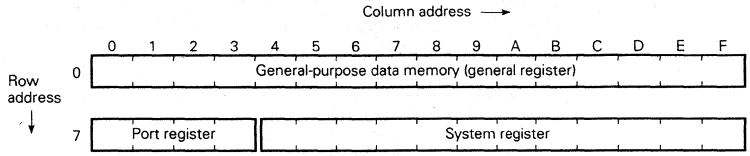
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation, comparison, evaluation, or transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17103L register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

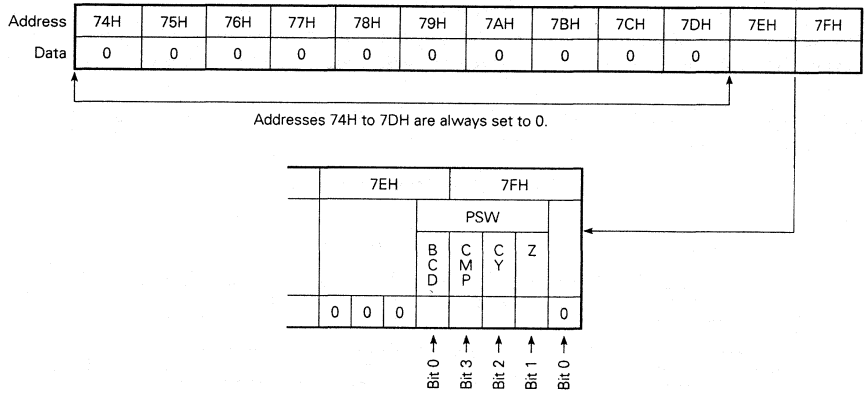
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17103L.

Fig. 4-2 System Register Map

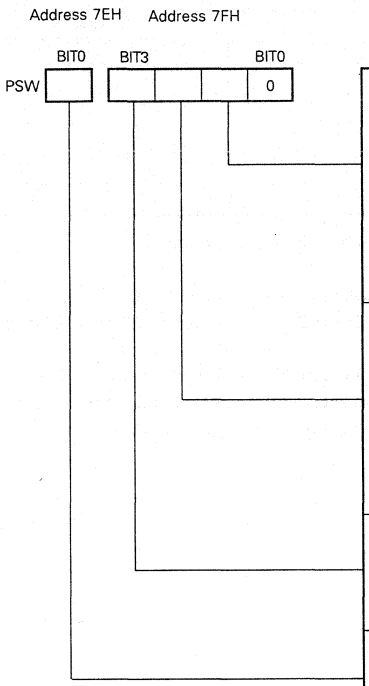


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7FH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Remark Z_{n-1}: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0B (P0B0/RLSHALT, P0B1/RLSSTOP, P0B2)

Port 0B is a 3-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port B consists of 4 bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17103L is in the HALT or STOP mode, P0B0 and P0B1 function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to **7. STANDBY FUNCTIONS.**)

6.2 PORT 0C (P0C0 to P0C3)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.3 PORT 0D (P0D0 to P0D3)

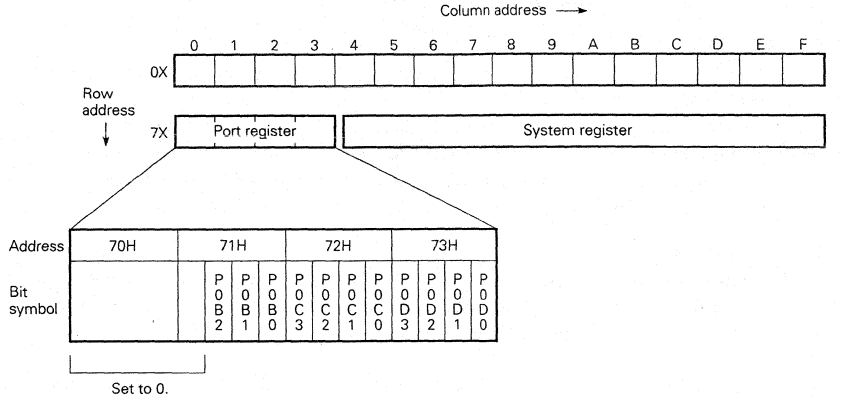
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.4 RECOMMENDED CONDITIONS FOR UNUSED μPD17103L PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports C and D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17103L provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting and releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

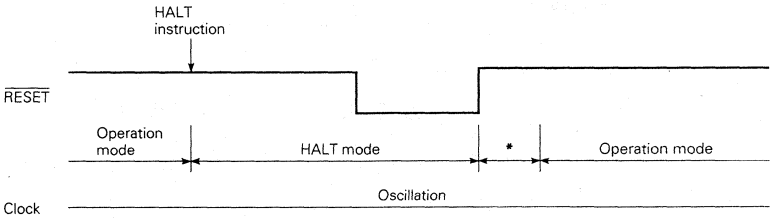
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting and releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instruction are executed starting at address 0H. The rising edge of the signal applied to the P0B1 pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the XIN pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

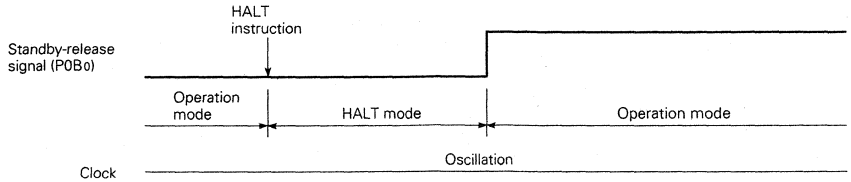
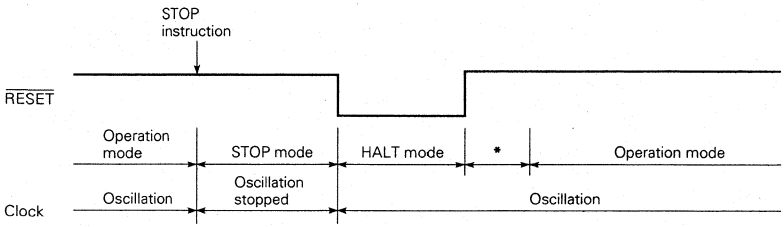


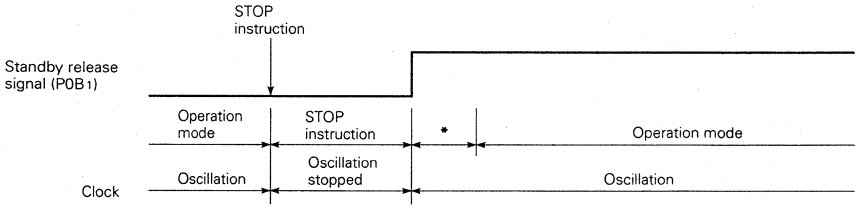
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bit 3 to bit 1 at 7FH	All 0s
Ports 0B to 0D	71H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17103L must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17103L.OPT file in AS17103L (device file for the μPD17103L) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instructions listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_2$ to $P0B_0$	OPTP0B	3	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	(RESET)	[;comment]

Example To set the following mask option in a μPD17103L source file to be assembled:

$P0B_2$: Pull-up $P0B_1$: Open
$P0B_0$: Open $\overline{RESET}$: Pull-up

```
                    ⋮
;17103L
 Setting mask options:   OPTION
                         OPTP0B  P0BPLUP, OPEN, OPEN
                         OPTRES  RESPLUP
                         ENDOP

                    ⋮
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17103L device file (AS17103L).

Table 9-2 Reserved symbols

Name	Attribute	Value	Read/write	Description
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3*	FLG	0.71H.3	Read	Set to 0.
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

* Although P0B3 does not exist in the μPD17103L, it is defined as a read-only flag so that it is treated as a dummy bit when a built-in macro is used.

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14} - b_{11} \ b_{15}			0		1	
BIN		HEX				
0 0 0 0		0	ADD	r, m	ADD	m, #i
0 0 0 1		1	SUB	r, m	SUB	m, #i
0 0 1 0		2	ADDC	r, m	ADDC	m, #i
0 0 1 1		3	SUBC	r, m	SUBC	m, #i
0 1 0 0		4	AND	r, m	AND	m, #i
0 1 0 1		5	XOR	r, m	XOR	m, #i
0 1 1 0		6	OR	r, m	OR	m, #i
0 1 1 1		7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0		8	LD	r, m	ST	m, r
1 0 0 1		9	SKE	m, #i	SKGE	m, #i
1 0 1 0		A				
1 0 1 1		B	SKNE	m, #i	SKLT	m, #i
1 1 0 0		C	BR	addr	CALL	addr
1 1 0 1		D			MOV	m, #i
1 1 1 0		E			SKT	m, #n
1 1 1 1		F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M	: One of data memory	STACK	: Stack specified by (SP)
m	: Data memory address specified by [m_H, m_L] of each bank	i	: Immediate data; 4 bits
		n	: Bit position; 4 bits
m_H	: Data memory address high (row address); 3 bits	addr	: One of program memory address; 11 bits
		a_H	: Program memory address high; 3 bits
m_L	: Data memory address low (column address); 4 bits	a_M	: Program memory address middle; 4 bits
		a_L	: Program memory address low; 4 bits
R	: One of general register specified by [(RP), r]	CY	: Carry flag
		CMP	: Compare flag
r	: General register address low (column address); 4 bits	s	: Stop release condition
		h	: Halt release condition
RP	: General register pointer	[ ]	: Address of M, R
PC	: Program counter	( )	: Contents of M, R
SP	: Stack pointer		

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to resister with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r ,m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M – i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M – i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M – i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M – i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if Mn = all "0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) – 1, STACK ← ((PC)+1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP)+1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C, or P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C, or P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	16-pin plastic DIP	400	mW
			16-pin plastic SOP	190	

Note 1. When a built-in pull-up resistor is mask-selected

2. When a built-in pull-up resistor is not mask-selected

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
Input/output capacitance	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.8 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note 1**
	V_{IH4}	0.8 V_{DD}		9	V		**Note 2**
Low-Level Input Voltage	V_{IL1}	0		0.25 V_{DD}	V	R0C, P0D	
	V_{IL2}	0		0.15 V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.15 V_{DD}	V	P0B	
High-Lovel Output Voltage	V_{OH}	V_{DD} − 1.0			V	P0C, P0D, I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL}			0.5	V	P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 1**
	I_{LIL3}			10	μA		V_{IN} = 9 V **Note 2**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 1**
	I_{LOH3}			10	μA		V_{OUT} = 9 V **Note 2**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0B, P0C, P0D, V_{OUT} = 0 V	
Pull-Up Resistor Provided for $\overline{RESET}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note 3**	I_{DD1}		500	900	μA	Operation mode	V_{DD} = 3 V ±10%, f_{CC} = 2 MHz
	I_{DD2}		400	700	μA	HALT mode	V_{DD} = 3 V ±10%, f_{CC} = 2 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 3 V ±10%

Note 1. When a built-in pull-up resistor is mask-selected
2. When a built-in pull-up resistor is not mask-selected
3. This current excludes the current which flows through the built-in pull-up resistors.

DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS ON LOW SUPPLY VOLTAGE
(T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	UNIT	TYP.	MAX.	CONDITION
Data Retention Supply Voltage	V_{DDDR}	1.5		3.6	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 1.5 V
Release Signal Set Time	t_{SREL}	0			μs	

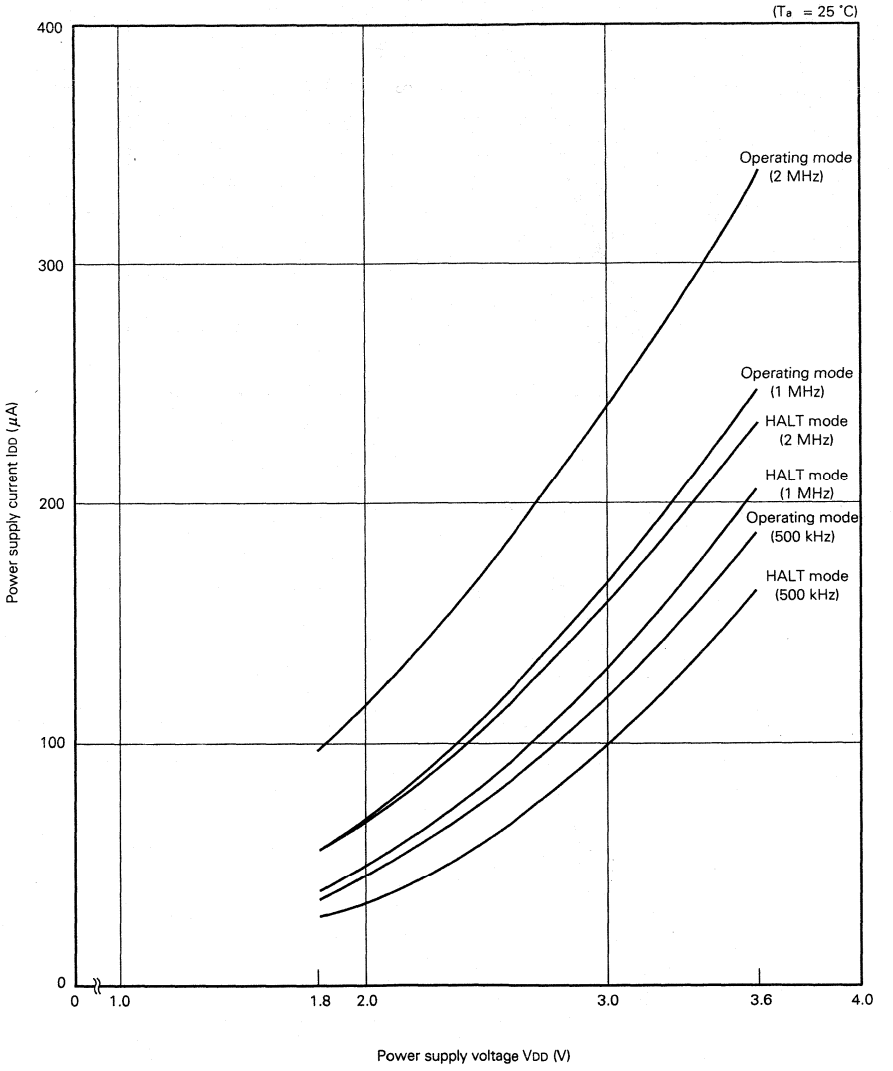
AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.8 to 3.6 V)

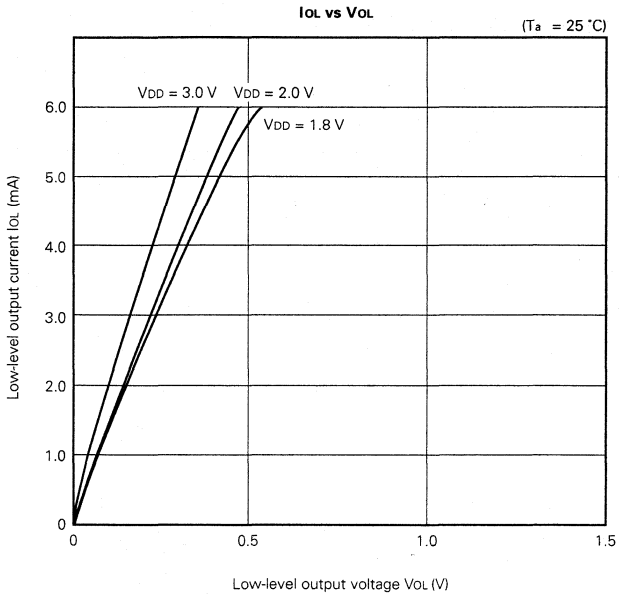
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	t_{CY}	7.6		33	μs	
High/low Level Width on P0B0 and P0B1	t_{PBH} t_{PBL}	100			μs	
High/Low Level Width on $\overline{\text{RESET}}$	t_{RSH} t_{RSL}	100			μs	

Remark t_{CY} = 16/f_{CC} (f_{CC}: System clock oscillation frequency)

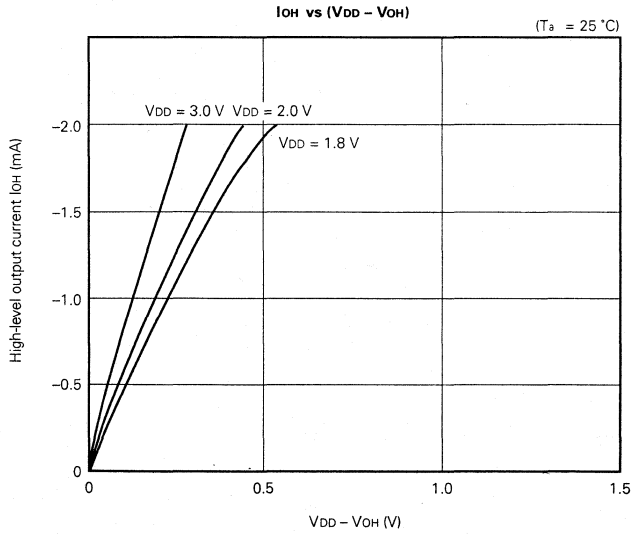
12. CHARACTERISTICS CURVE

I_{DD} vs V_{DD}





Caution The absolute maximum rated current is 30 mA per pin.

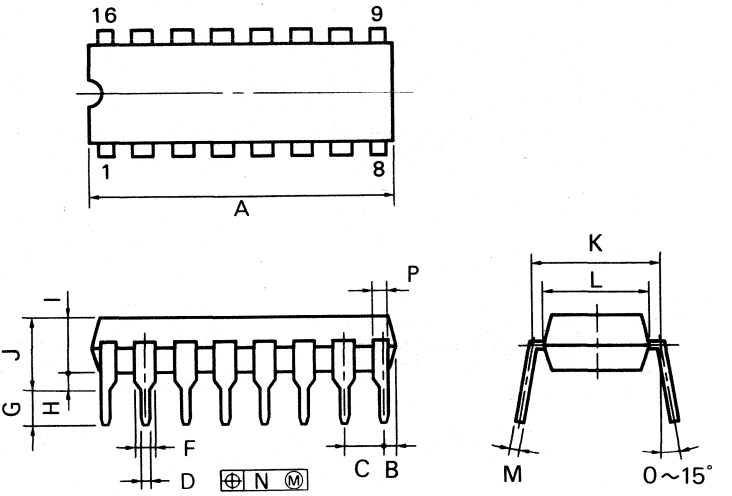


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values.

13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

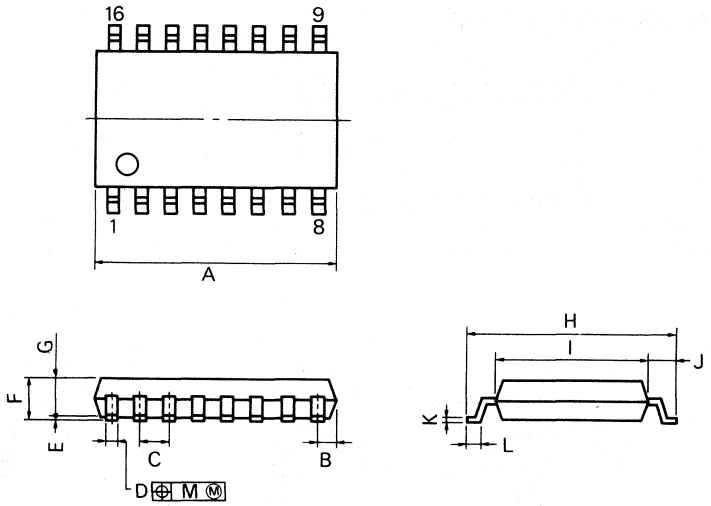
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{+0.3}$	$0.138^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



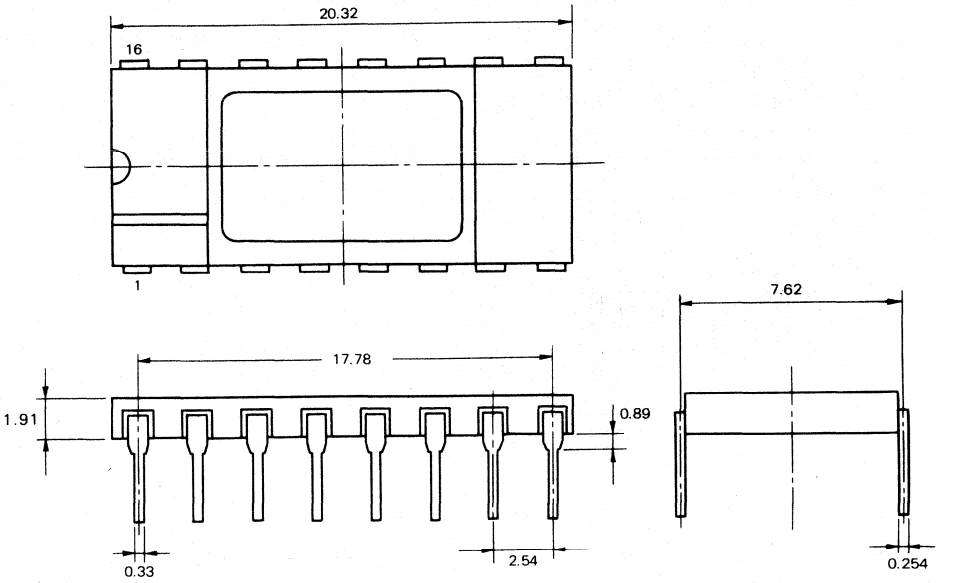
P16GM-50-300B-1

NOTE

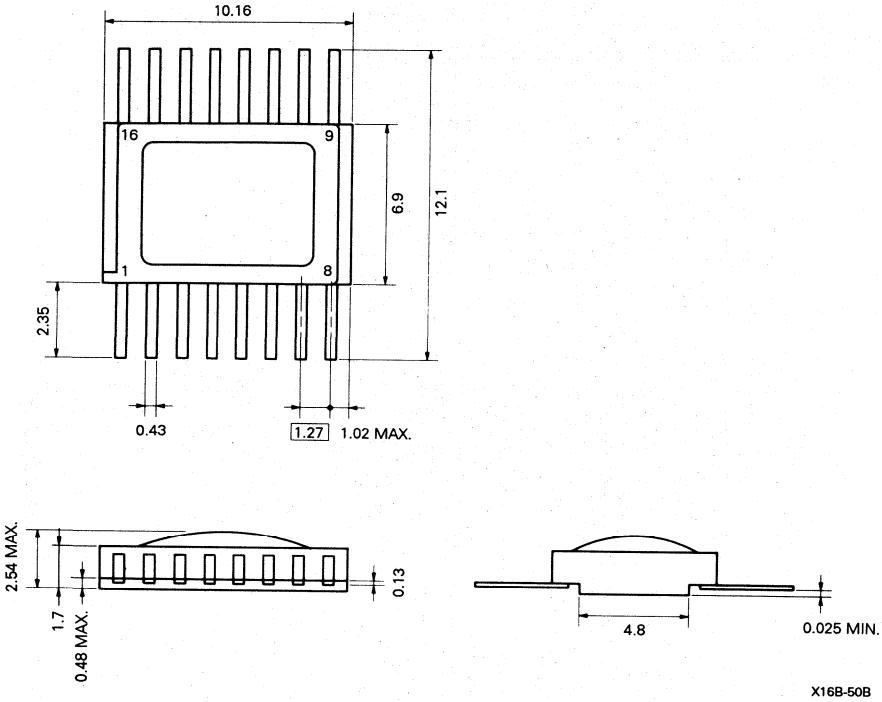
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

Package dimensions of the 16-pin ceramic DIP for ES (reference) (Unit: mm)



Package dimensions of the 16-pin ceramic SOP for ES (reference) (Unit: mm)



14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17103L.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17103LCX-xxx	16-pin plastic DIP (300 mil)	• Wave soldering • Partial heating method
μPD17103LGS-xxx	16-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions for surface mount type products, refer to our document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of input/ output port pins*	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the number of input/output port pins selectable between N-ch open-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICRCONTROLLER

The μPD17104L is a tiny microcontroller consisting of a ROM (512 x 16 bits), RAM (16 x 4 bits), and 16 input/output ports. The functions and pins of the μPD17104L are compatible with those of the μPD17104.

The μPD17104L can operate at the low voltage (1.8 V min.). It can be used for wide variety of products controlled by one lithium battery or two dry cells.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM): 512 words x 16 bits
- Data memory (RAM): 16 x 4 bits
- Input/output ports: 16 ports (including three N-ch open-drain outputs)
- Instruction execution time: 8 use (with 2 MHz crystal or ceramic resonator used)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function: STOP and HALT modes
- Data memory can retain data on low voltage (1.5 V min.).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 1.8 to 3.6 V (at 2 MHz)

APPLICATIONS

- Controlling electric appliances or toys

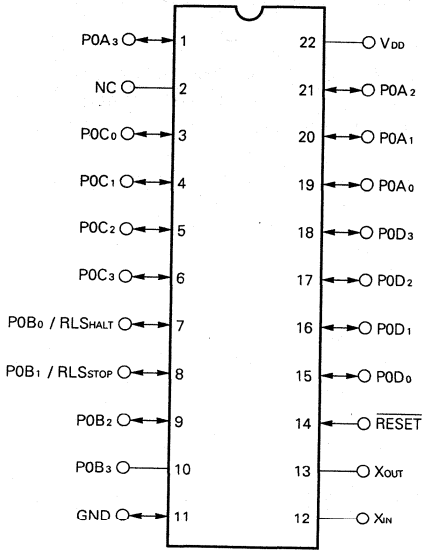
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17104LCS-xxx	22-pin plastic shrink DIP (300 mil)	Standard
μPD17104LGS-xxx	24-pin plastic SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

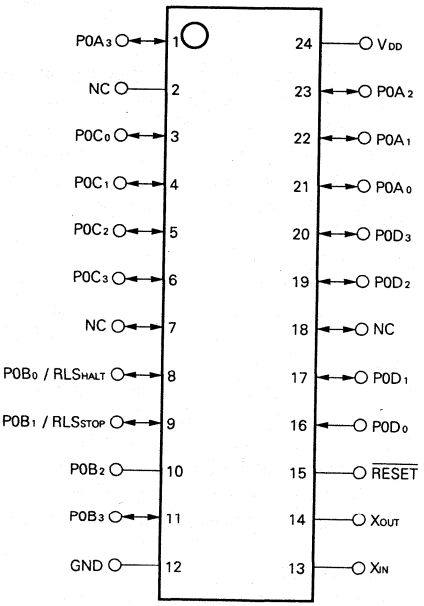
PIN CONFIGURATION (Top View)

μPD17104LCS



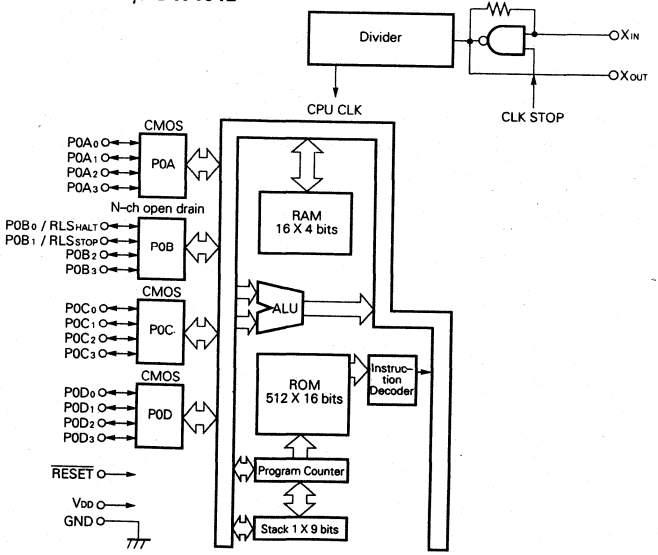
22–pin plastic shrink DIP

μPD17104LGS



24–pin plastic SOP

BLOCK DIAGRAM OF μPD17104L



PIN FUNCTIONS

Pin Funcctions

• Port pins

Pin name	I/O	Function	Reset
$P0A_0$-$P0A_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0A) (port 0A)	High impedance (input mode)
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: Highlevel (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$, $P0B_3$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0C_0$-$P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$-$P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

• Non-port pins

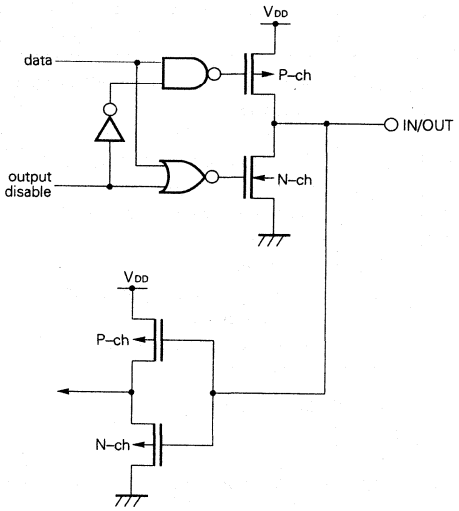
Pin name	I/O	Function
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).
V_{DD}		• Positive power supply pin
GND		• GND pin
X_{IN}, X_{OUT}		• Pins to be connected to the system clock resonator

I/O: Input/output

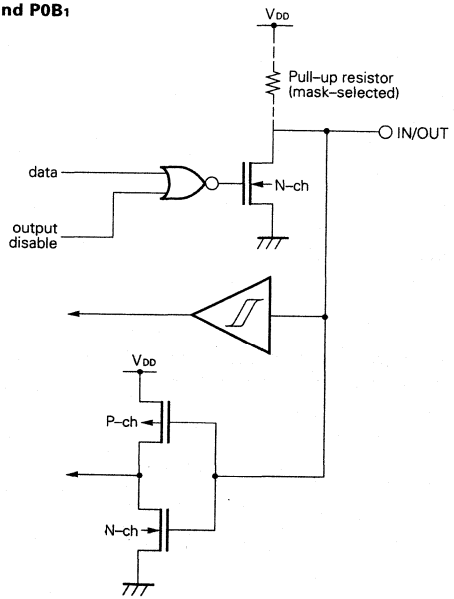
PIN EQUIVALENT CIRCUITS

Following are schematics of the euivalent circuits of the pins of the μPD17104L.

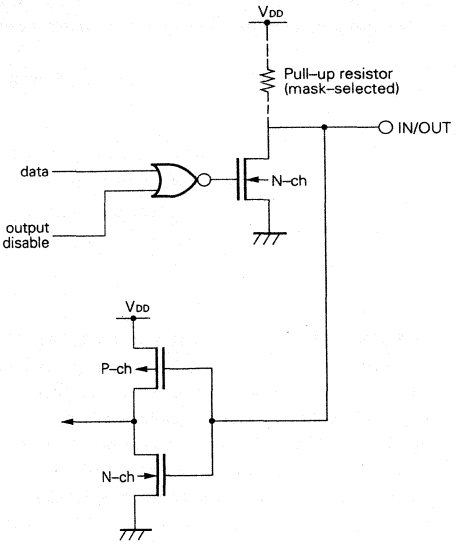
(1) P0A, P0C, and P0D



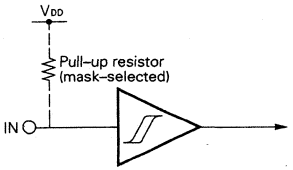
(2) P0B0, and P0B1



(3) $P0B_2$, and $P0B_3$



(4) $\overline{\text{RESET}}$

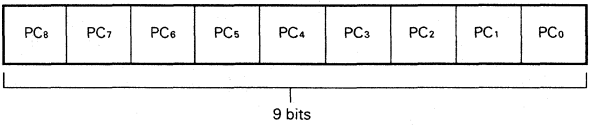


1. PROOGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

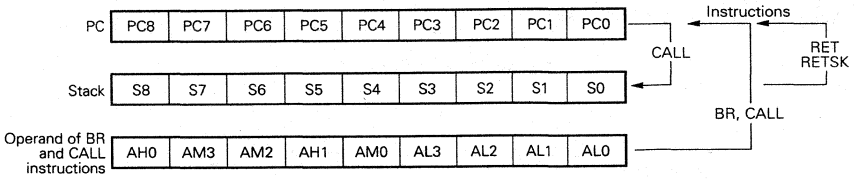
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17104L is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

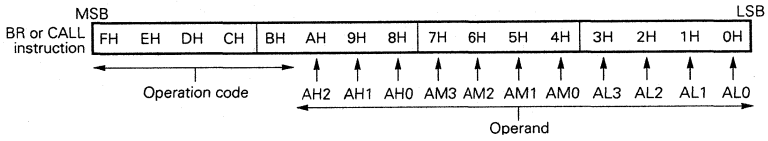
Fig. 2-1 shows the relationship between PC, stack, and operands of BR and CALL instructions.

Fig. 2-1 Relationship between PC, Stack, and Operands of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leqq n \leqq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leqq n \leqq 8$) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM)

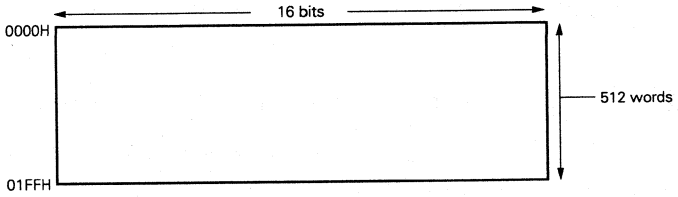
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01 FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory (ROM).

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory (RAM) stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

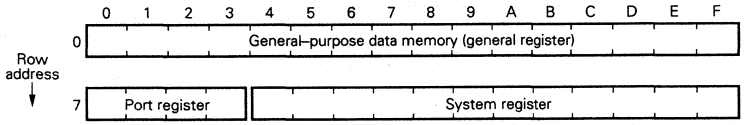
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM)

The data memory is configured in units of 4 bits, or "one nibble," and an address on assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation, comparison, evaluation, or transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17104L regisster pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

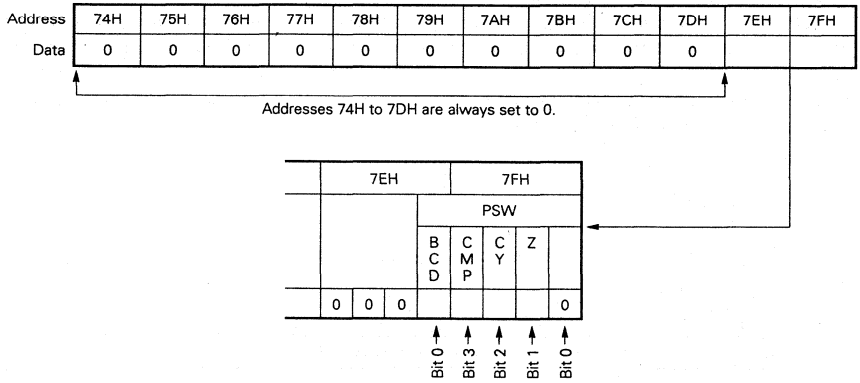
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed foor a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17104L.

Fig. 4-2 System Register Map

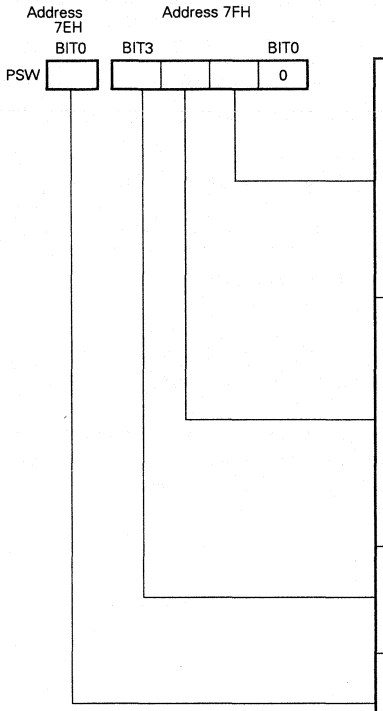


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when : • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 When : • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when : • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when : • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, the arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Conditon	Z flag value	
	CMP = 0	CMP = 1
Reset	0	–
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Remark Z_{n-1}: The Z flag value present immediately before arithmetic operation.

While CMP is 1, if an arithmetic operation results in OH when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than OH, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in OH.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERRATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or -10 to -1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XOR ing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0A (P0A0 to P0A3)

Port 0A is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 70H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0A are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of wheter the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.2 PORT 0B (P0B0/RLSHALT, P0B1/RLSSTOP, P0B2, P0B3)

Port 0B is a 4-bit input/output port. Only N-ch open-drain outputs appear on the pins of port of 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

When the μPD17104L is in the HALT or STOP mode, P0B0 and P0B1 function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to **7. STANDBY FUNCTIONS**)

6.3 PORT 0C (P0C0 to P0C3)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port POC are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.4 PORT 0D (P0D0 to P0D3)

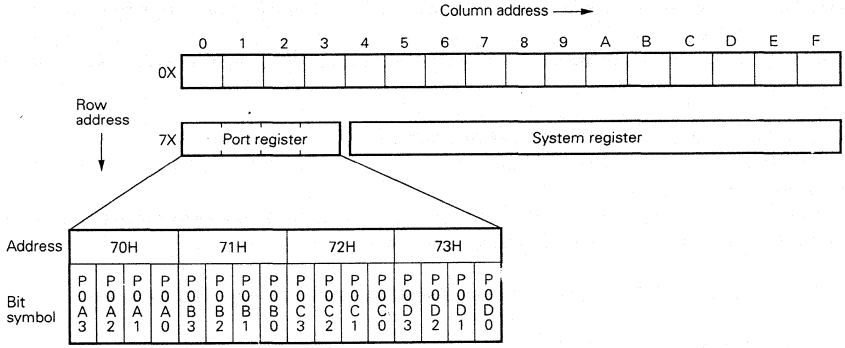
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.5 RECOMMENDED CONDITIONS FOR UNUSED μPD17104L PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/Output mode	Port	Recommended connection
Input mode	Ports A, B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports A, C, and D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17104L provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000$\underline{X}$B ←4-bit data in the operand

X	Conditions for setting and releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_0$ is 0, executing the HALT instruction enters the HALT mode. If $P0B_0$ is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and Releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

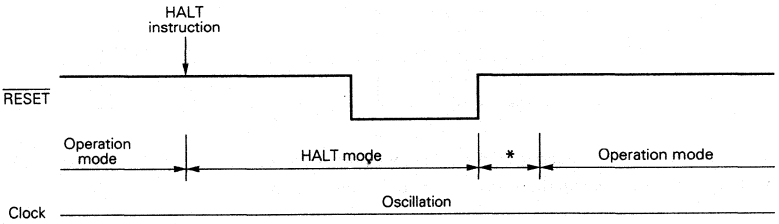
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

HALT 000XB ←4-bit data in the operand

X	Conditions for setting and releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_1$ is 0, executing the STOP instruction enters the STOP mode. If $P0B_1$ is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the X_{IN} pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

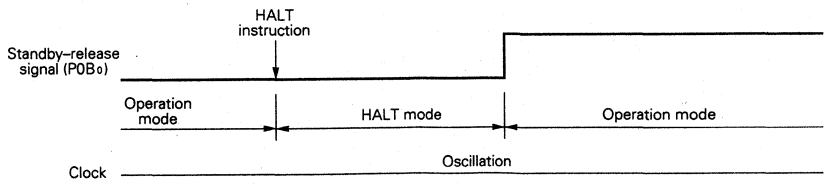
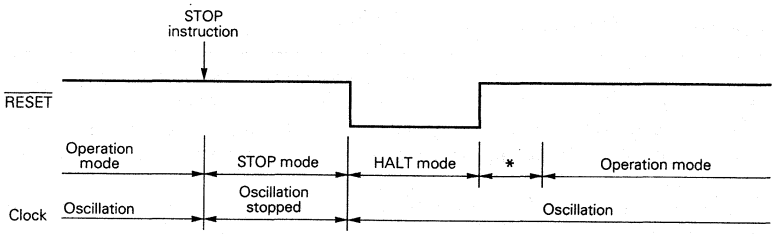


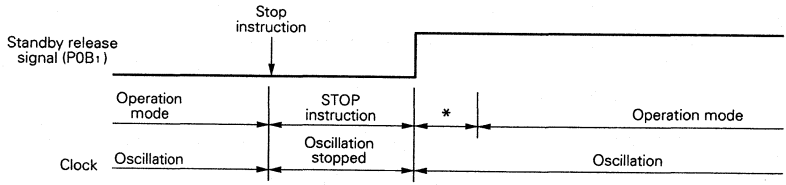
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin clause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the X_{IN} pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bit 3 to bit 1 at 7FH	All 0s
Ports 0A to 0D	70H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17104L must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17104L.OPT file in AS17104L (device file for the μPD17104L) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseduo instructions listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_3$ to $P0B_0$	OPTP0B	4	POBPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_3$, $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_3$), ($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	(RESET)	[;comment]

Example

To set the following mask options in a μPD17104L source file to be assembled:

P0B3: Pull-up
P0B2: Pull-up
P0B0: Open
P0B1: Open
RESET: Pull-up

```
                    :
;17104L
 Setting mask options:  OPTION
                        OPTP0B      P0BPLUP, P0BPLUP, OPEN, OPEN
                        OPTRES      RESPLUP
                        ENDOP
                    :
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17104L device file (AS17104L).

Table 9-2 Reserved symbols

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14} - b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #i
0001	1	SUB	r, m	SUB	m, #i
0010	2	ADDC	r, m	ADDC	m, #i
0011	3	SUBC	r, m	SUBC	m, #i
0100	4	AND	r, m	AND	m, #i
0101	5	XOR	r, m	XOR	m, #i
0110	6	OR	r, m	OR	m, #i
0111	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #i	SKGE	m, #i
1010	A				
1011	B	SKNE	m, #i	SKLT	m, #i
1100	C	BR	addr	CALL	addr
1101	D			MOV	m, #i
1110	E			SKT	m, #n
1111	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M	:	One of data memory	n	:	Bit position; 4 bits
m	:	Data memory address specified by [mH, mL] of each bank	addr	:	One of program memory address; 11 bits
m_H	:	Data memory address high (row address); 3 bits	a_H	:	Program memory address high; 3 bits
m_L	:	Data memory address low (column address); 4 bits	a_M	:	Program memory address middle; 4 bits
R	:	One of general register specified by [(RP), r]	a_L	:	Program memory address low; 4 bits
r	:	General register address low (column address); 4 bits	CY	:	Carry flag
RP	:	General register pointer	CMP	:	Compare flag
PC	:	Program counter	s	:	Stop release condition
SP	:	Stack pointer	h	:	Halt release condition
STACK	:	Stack specified by (SP)	[ ]	:	Address of M, R
i	:	Immediate data; 4 bits	( )	:	Contents of M, R

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immmediate data to memory with carry	R← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r, m	Subtract memory from register	R← (R) − (M)	00001	m_H	m_L	i
		m, #i	Subtract immediate data from memory	M← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M← (M) − i − (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M–i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M–i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M–i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M–i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M← (M) OR (M)	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load memory of register	R← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M)← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M← i	11001	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP← 0 skip if Mn = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP← 0 skip if Mn = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP← (SP) −1, STACK ← ((PC)+1), PC← ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC← (STACK), SP← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC← (STACK), SP← (SP) +1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} +0.3	V
			Note 2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, or P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, or P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin plastic shrink DIP	400	mW
			24-pin plastic SOP	250	

Note 1. When a built-in pull-up resistor is mask-selected.

2. When a built-in pull-up resistor is not mask-selected.

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT.	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz
Input/Output Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.8 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT.	CONDITION	
High-level Input Voltaged	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0C, P0D	
	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	Note 1
	V_{IH4}	0.8 V_{DD}		9	V	P0B	Note 2
Low-Level Input Voltage	V_{IL1}	0		0.25 V_{DD}	V	P0A, P0C, P0D	
	V_{IL2}	0		0.15 V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.15 V_{DD}	V	P0B	
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0			V	P0A, P0C, P0D I_{OH} = -200 μA	
Low-Level Output Voltage	V_{OL}			0.5	V	P0A, P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0A, P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} Note 1
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V Note 2
Low-Level Input Leakage Current	I_{LIL1}			-5	μA	P0A, P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			-5	μA	P0A, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0A, P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} Note 1
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V Note 2
Low-Level Output Leakage Current	I_{LOL}			-5	μA	P0A, P0B, P0C, P0D, V_{OUT} = 0 A	
Pull-Up Resistor Provided for $\overline{RESET}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current Note 3	I_{DD1}		500	900	μA	Operation mode	V_{DD} = 3 V ±10% f_{CC} = 2 MHz
	I_{DD2}		400	700	μA	HALT mode	V_{DD} = 3 V ±10% f_{CC} = 2 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 3 V ±10%

Note 1. When a built-in pull-up resistor is mask-selected.

2. When a built-in pull-up resistor is not mask-selected.

3. This current excludes the current which flows through the built-in pull-up resistors.

DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS ON LOW SUPPLY VOLTAGE
(T_a = –40 to +85 °C)

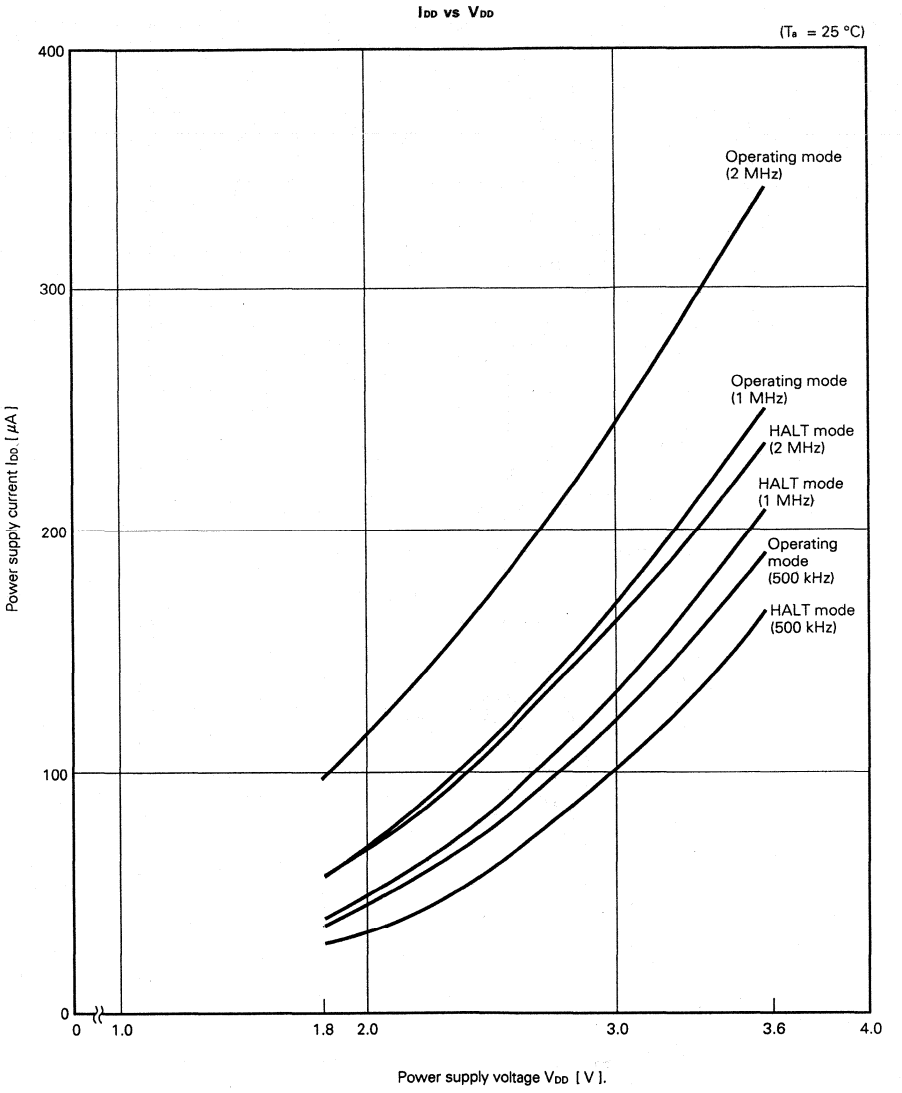
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT.	CONDITION
Data Retention Supply Voltage	V_{DDDR}	1.5		3.6	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 1.5 V
Release Signal Set Time	t_{SREL}	0			μs	

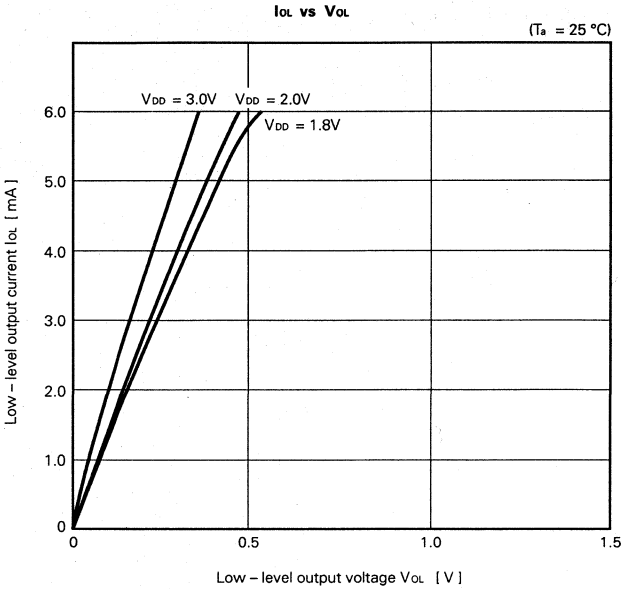
AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 1.8 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT.	CONDITION
Internal Clock Cycle Time	t_{CY}	7.6		33	μs	
High/Low Level Width on POB_0 and POB_1	t_{PBH} t_{PBL}	100			μs	
High/Low Level Width on $\overline{RESET}$	t_{RSH} t_{RSL}	100			μs	

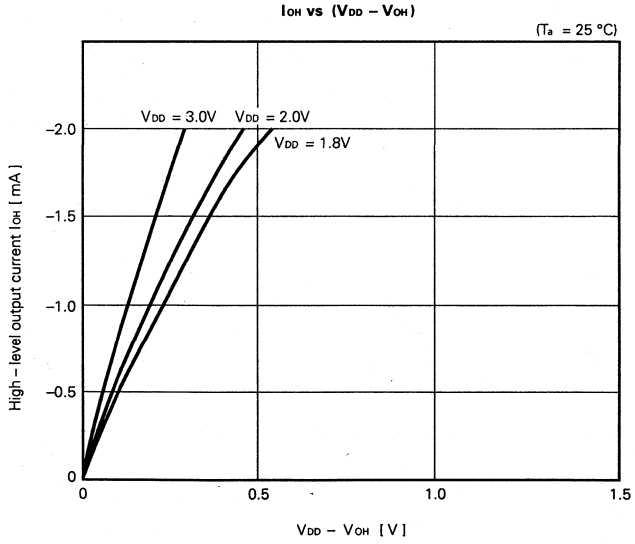
Remark t_{CY} = 16/fcc (fcc: System clock oscillation frequency)

12. CHARACTERISTICS CURVE





Caution The absolute maximum rated current is 30 mA per pin.

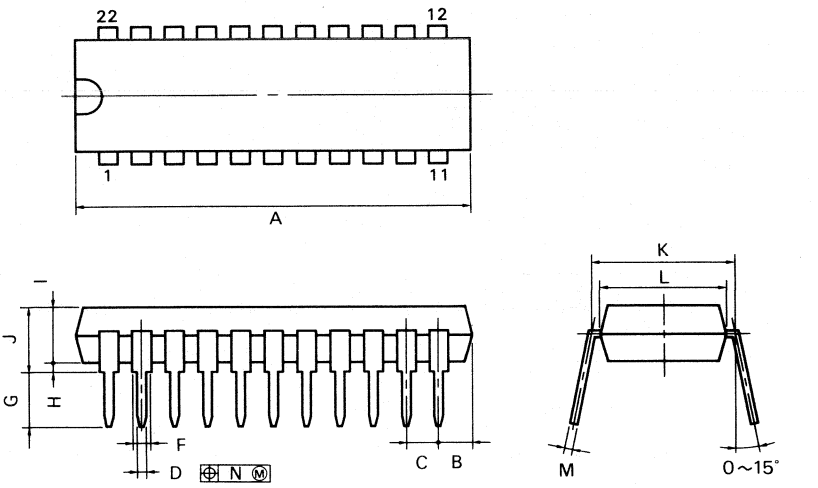


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values.

13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-300B

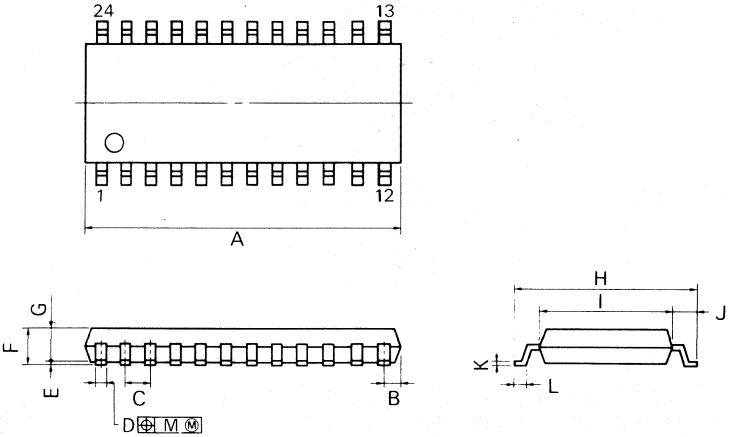
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm0.3}$	$0.126^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



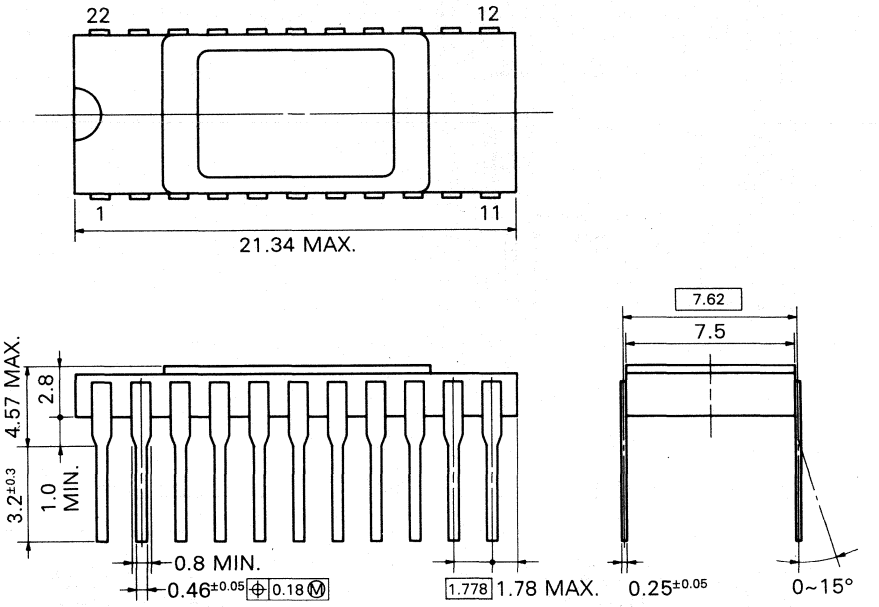
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

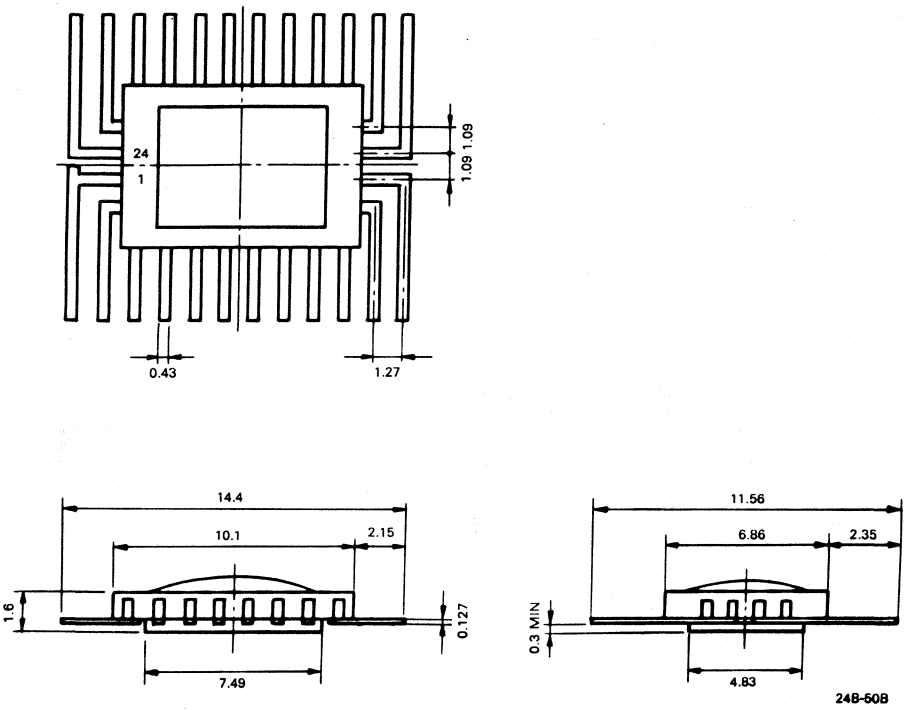
ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{-0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	$0.6^{+0.2}$	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

Package dimensions of the 22-pin ceramic shrink DIP for ES (reference) (units: mm)



P22D-70-300B

Package dimensions of the 24-pin ceramic SOP for ES (reference) (Unit: mm)



14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17104L.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17104LCS-xxx	22-pin plastic shrink DIP (300 mil)	• Wave soldering • Partial heating method
μPD17104LGS-xxx	24-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions for surface mount type products, refer to our document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 x 16 bits							
RAM size	16 x 4 bits							
Number of input/output port pins*	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the number of input/output port pins selectable between N-ch open-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P103 is a tiny microcontrollers consisting of a 1K-byte ROM, 16-word RAM, and 11 input/output ports. It is a one-time PROM version of the μPD17103, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P103 models are available: μPD17P103CX, which allows a program to be written only once, and μPD17P103GS. They are suitable for evaluation of μPD17103 and for small-scale production.

The μPD17000 architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17103
- Program memory (one-time PROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 11 ports (including three N-ch open-drain outputs)
- Instruction execution time: 2 μs (with 8-MHz crystal or ceramic resonator connected)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

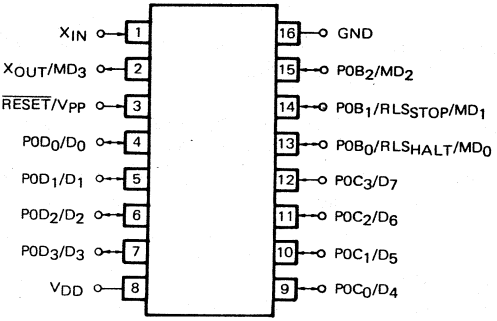
- Controlling electric appliances or toys
- Providing general-purpose logic ICs in one chip

ORDERING INFORMATION

Order Code	Package
μPD17P103CX	16-pin plastic DIP (300 mil)
μPD17P103GS	16-pin plastic SOP (300 mil)

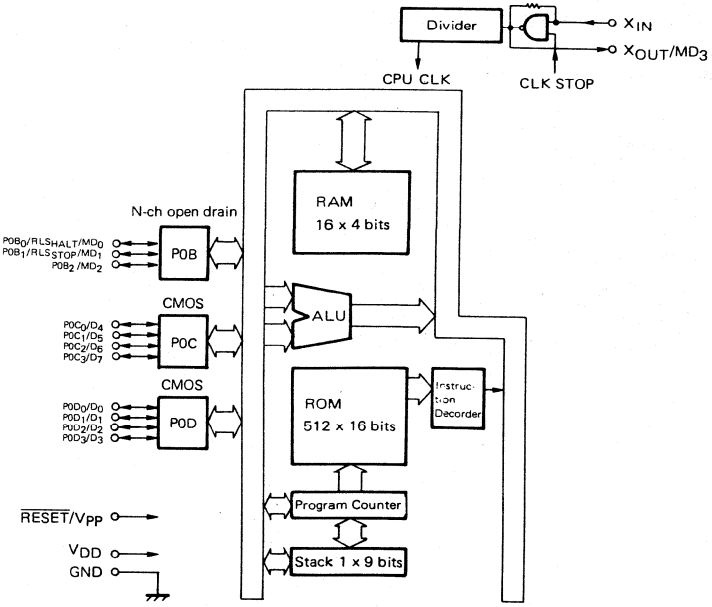
PIN CONFIGURATION (Top View)

μPD17P103CX/μPD17P103GS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN		FUNCTION		When writing to program memory or verifying its contents	WHEN RESET
$P0B_0$	Input/ output	RLS_{HALT}	MD_0	• N-ch open-drain 4-bit input/ output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP}	MD_1		For the STOP mode releasing		
$P0B_2$		MD_2					
$P0C_0$	Input/ output	D_4		• CMOS (push-pull) 4-bit input/output port (port 0C)		8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5					
$P0C_2$		D_6					
$P0C_3$		D_7					
$P0D_0$	Input/ output	D_0		• CMOS (push-pull) 4-bit input/output port (port 0D)		8-bit data input/ output pin (low-order 4-bits)	High impedance (input mode)
$P0D_1$		D_1					
$P0D_2$		D_2					
$P0D_3$		D_3					

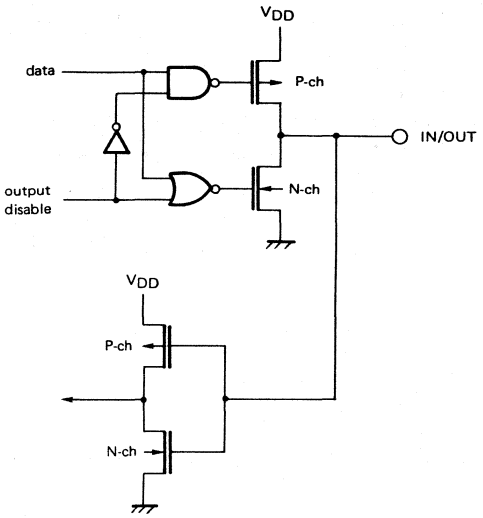
- Non-port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN	FUNCTION	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
X_{IN}			Pins to be connected to the system clock resonator	Program memory address update
X_{OUT}		MD_3	Pins to be connected to the system clock resonator	Mode selection pin

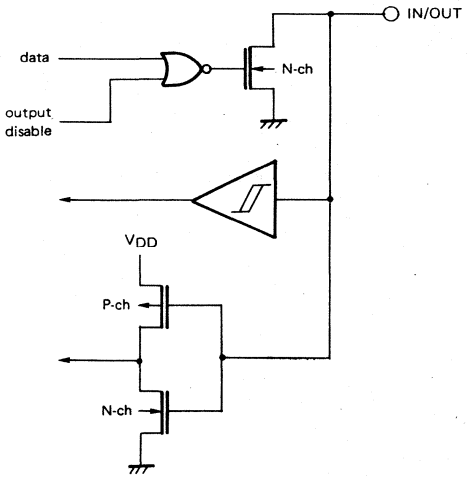
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17P103.

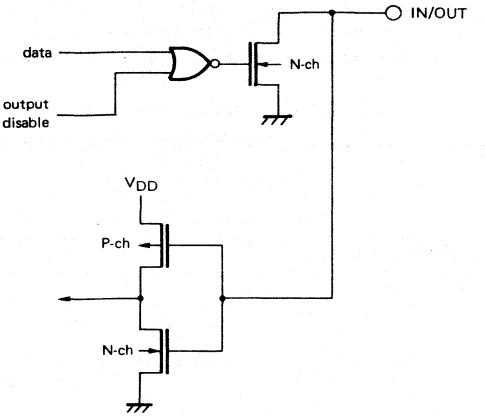
(1) P0C and P0D



(2) $P0B_0$ and $P0B_1$



(3) $P0B_2$



(4) $\overline{RESET}$

9. DIFFERENCES BETWEEN THE μPD17P103 AND μPD17103

The μPD17P103 is a one-time PROM version of the μPD17103, in which the internal mask ROM is replaced with a one-time PROM. The μPD17P103 has the same CPU functions and internal hardwares as those of μPD17103 except for its program memory and mask option. Table 9-1 lists the differences between them.

Table 9-1 Differences between μPD17P103 and μPD17103

ITEM	μPD17P103	μPD17103
ROM	One-time PROM 512 x 16 bits	Mask ROM 512 x 16 bits
Pull-up resistors of pins POB_0 to POB_2	None	Mask option
Pull-up resistors of $\overline{RESET}$ pin	None	Mask option
Connection pin	V_{PP} pin and operation mode selection pins are provided.	V_{PP} pin and operation mode selection pins are not provided.
Power supply	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)	
Package	16-pin DIP 16-pin SOP	

10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P103's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X_{IN} pin.

PIN NAME	FUNCTION
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
X_{IN}	Input pin for address update clock used when writing to program memory or verifying its contents.
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 Program Memory Write/Verify Modes

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P103 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L (low) or H (high)

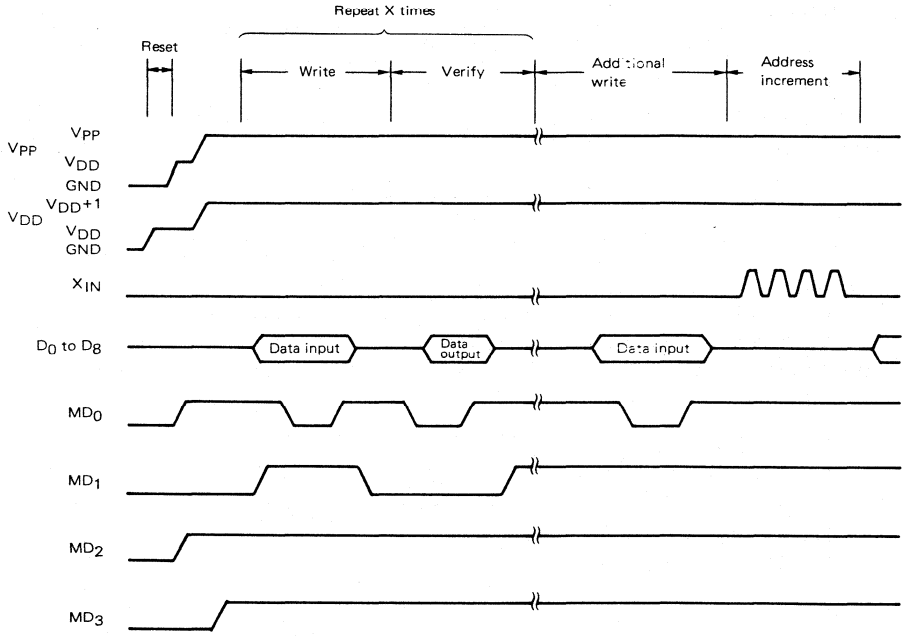
10.2 Writing to Program Memory

The procedure for writing to program memory is described below: high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) x 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the X_{IN} pin.

(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

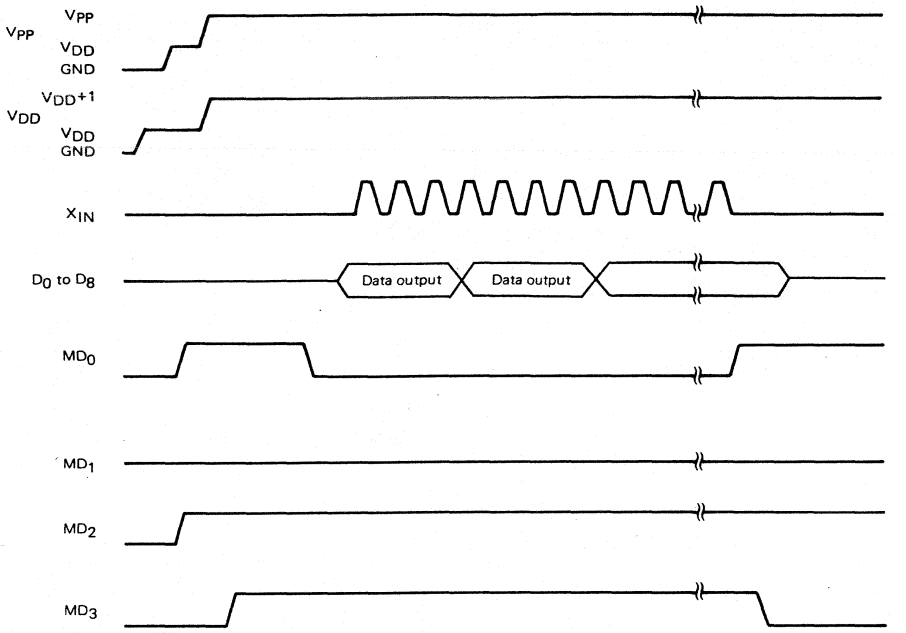
The timing for steps (2) to (12) is shown below.



10.3 Reading Program Memory

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the X_{IN} pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



13. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C, P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_stg			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	16-pin DIP	400	mW
			16-pin SOP	190	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	f=1 MHz
I/O(*) Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

*: Input/Output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B	(*)
	V_{IH4}	V_{DD}-0.5		V_{DD}	V	X_{IN}	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	X_{IN}	
High-Level Output Voltage on P0C and P0D	V_{OH}	V_{DD}-2.0			V	V_{DD}=4.5 to 6.0 V, I_{OH}=−2 mA	
		V_{DD}-1.0			V	I_{OH}=−200 μA	
Low-Level Output Voltage on P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD}=4.5 to 6.0 V, I_{OL}=15 mA	
				0.5	V	I_{OL}=600 μA	
High-Level Input Leakage Current on P0B, P0C, and P0D	I_{LIH1}			5	μA	V_{IN}=V_{DD}	
	I_{LIH2}			10	μA	V_{IN}=9 V	(*)
Low-Level Input Leakage Current on P0B, P0C, and P0D	I_{LIL}			−5	μA	V_{IN}=0 V	
High-Level Output Leakage Current on P0B, P0C, and P0D	I_{LOH1}			5	μA	V_{OUT}=V_{DD}	
	I_{LOH2}			10	μA	V_{OUT}=9 V	(*)
Low-Level Output Leakage Current on P0B, P0C, and P0D	I_{LOL}			−5	μA	V_{OUT}=0 V	
Power Supply Current	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD}=5.0 V ±10 %, f_{CC}=8.0 MHz
			250	750	μA		V_{DD}=3.0 V ±10 %, f_{CC}=2.0 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD}=5.0 V ±10 %, f_{CC}=8.0 MHz
			200	600	μA		V_{DD}=3.0 V ±10 %, f_{CC}=2.0 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD}=5.0 V ±10 %,
			0.1	5	μA		V_{DD}=3.0 V ±10 %

*: When N-ch open-drain input/output is selected.

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7-V_{DD}		V_{DD}	V	Except X_{IN}
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	X_{IN}
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except X_{IN}
	V_{IL2}	0		0.4	V	X_{IN}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1: V_{PP} must be under +13.5 V including overshoot.

2: V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

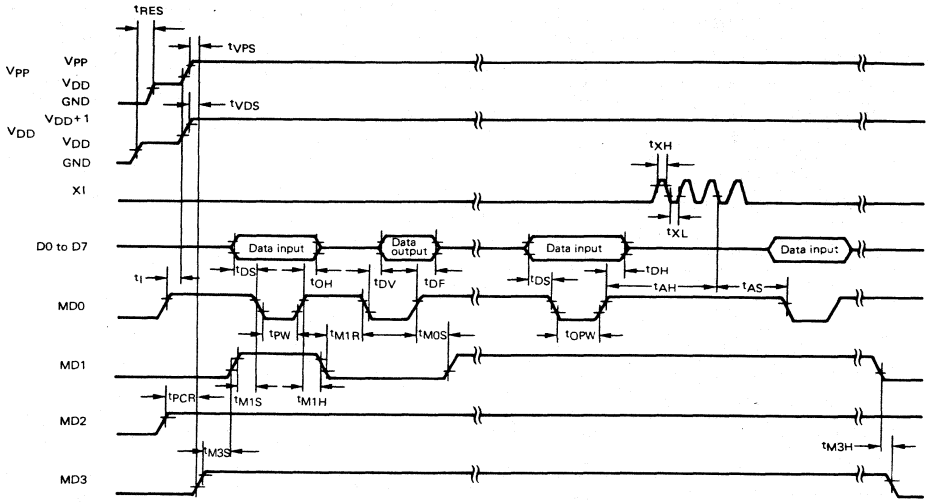
AC PROGRAMMING CHARACTERISTICS
(T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time(*2) to MD0 ↓	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0 ↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time(*2) to MD0 ↑	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time From MD0 ↑→	t_{DF}	t_{DF}	0		130	ns	
Vpp Setup Time to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1 ↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time From MD0 ↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time to MD0 ↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
X_{IN} Input High, Low Level Range	t_{XH}, t_{XL}	–	0.125			μs	
X_{IN} Input Frequency	f_X	–			4.19	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1 ↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1 ↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0 ↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time From Address(*2)	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time From Address(*2)	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0 ↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time From MD3 ↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

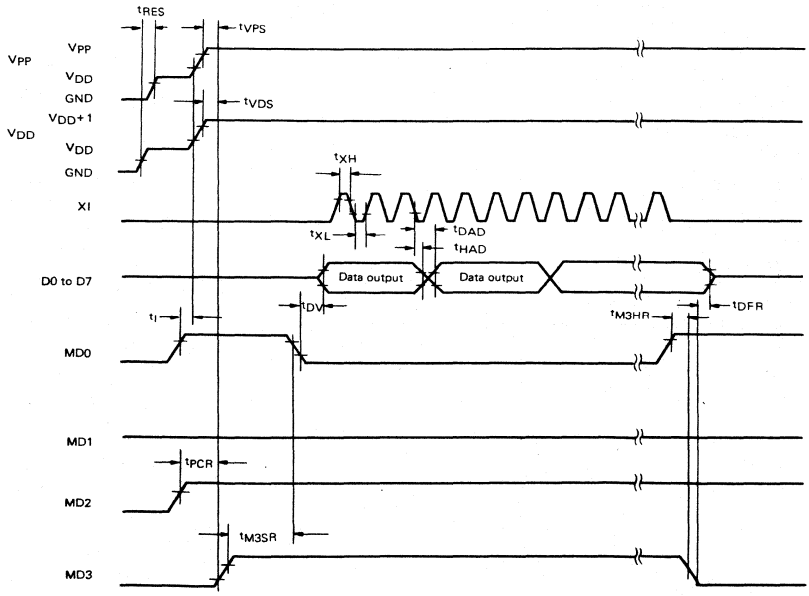
*1: Symbols for corresponding μPD27C256.

*2: Internal address signal is incremented by one at the falling edge of the third X_{IN} input, and it is not connected to the pin.

Write program memory timing

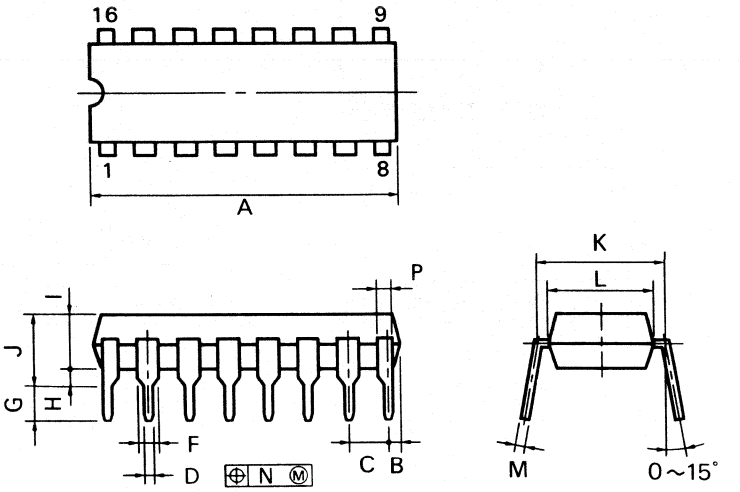


Read program memory timing



13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

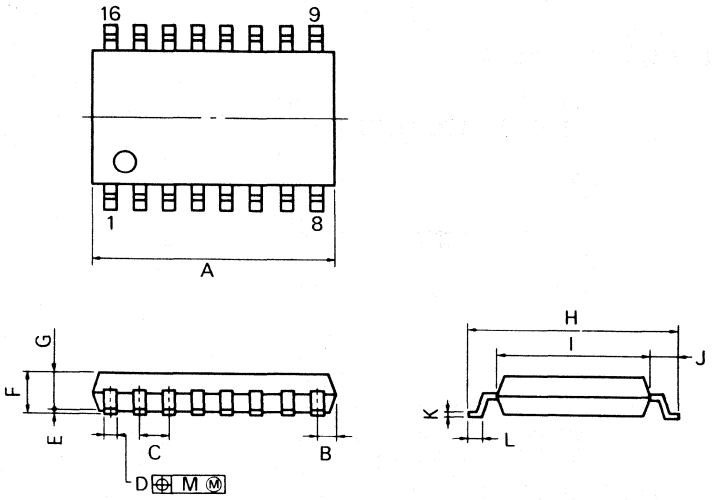
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{+0.3}$	$0.138^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



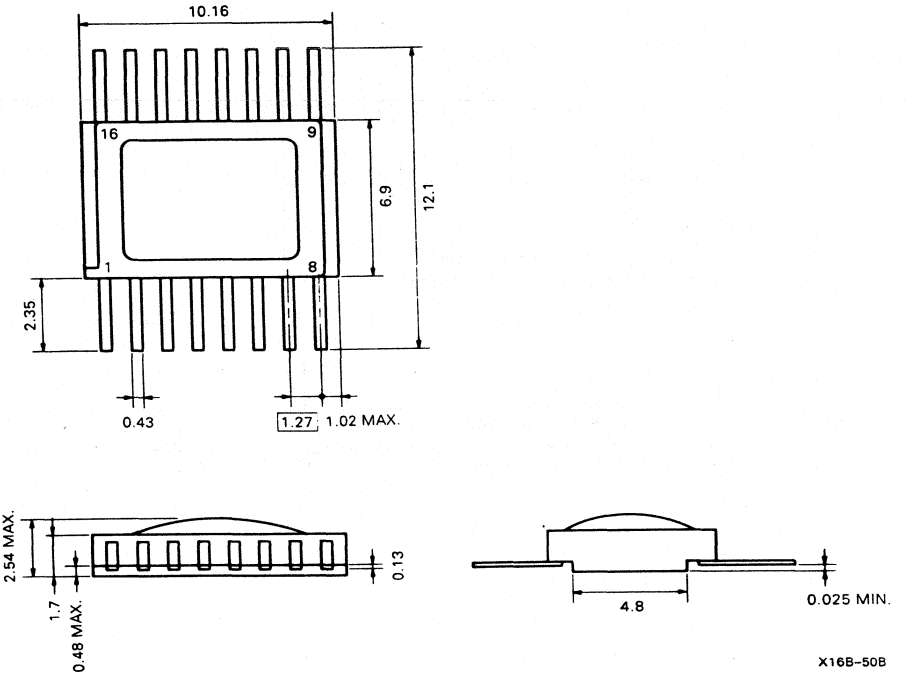
P16GM-50-300B-1

NOTE

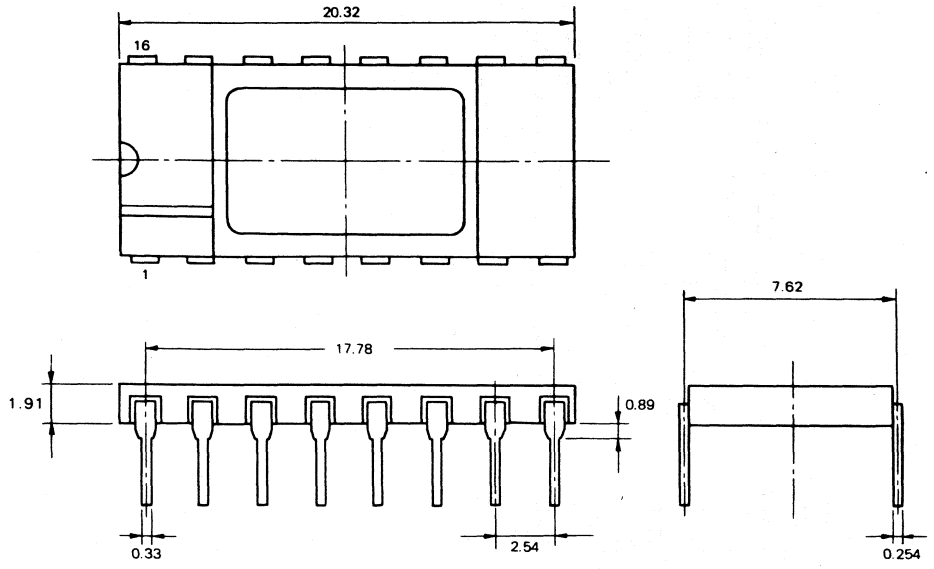
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

PACKAGE DIMENSIONS OF THE 16-PIN CERAMIC SOP FOR ES (reference) (Unite: mm)



PACKAGE DIMENSIONS OF THE 16-PIN CERAMIC DIP FOR ES (reference) (Unite: mm)



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P104 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17104, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P104 models are available: μPD17P104CS and μPD17P104GS, which allow a program to be written only once. They are suitable for evaluation of μPD17104 and for small-scale production.

The μPD17000 architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17104
- Program memory (one-time PROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 16 ports (including four N-ch open-drain outputs)
- Instruction execution time: 2 μs (with 8 MHz crystal or ceramic resonator connected)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
  4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

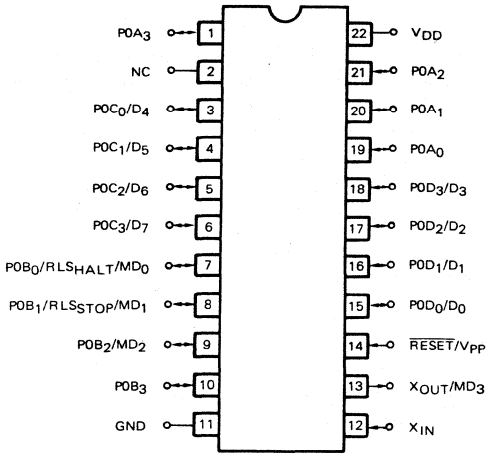
- Controlling electric appliances or toys
- Providing general-purpose logic ICs in one chip

ORDERING INFORMATION

Order Code	Package
μPD17P104CS	22-pin plastic shrink DIP (300 mil)
μPD17P104GS	24-pin plastic SOP (300 mil)

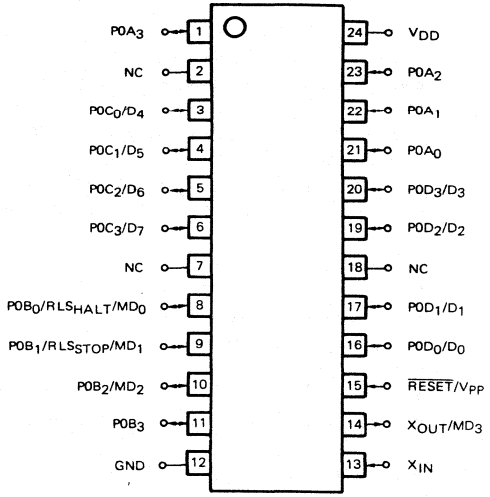
PIN CONFIGURATION (Top View)

μPD17P104CS



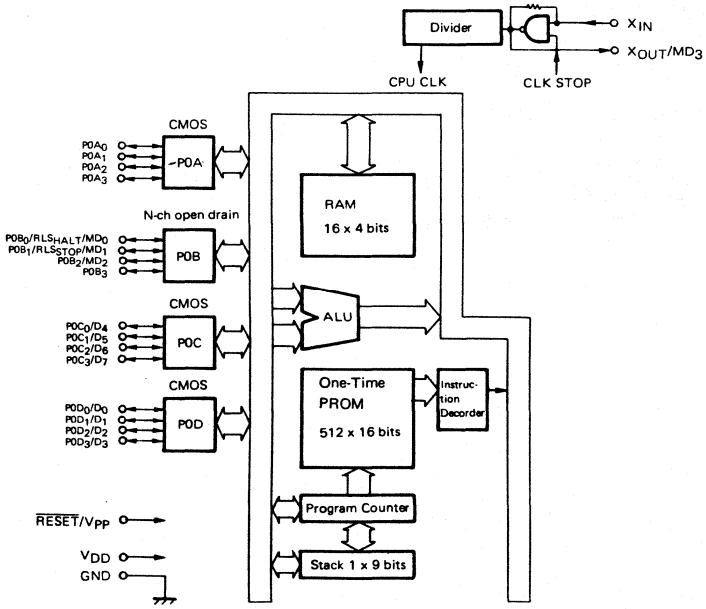
22-pin plastic shrink DIP

μPD17P104GS



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

- Port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN		FUNCTION		When writing to program memory or verifying its contents	WHEN RESET
$P0A_0$	Input/output			• CMOS (push-pull) 4-bit input/ output port (port 0A)		Pull down	High impedance (input mode)
$P0A_1$							
$P0A_2$							
$P0A_3$							
$P0B_0$	Input/output	RLS_{HALT}	MD_0	• N-ch open-drain 4-bit input/ output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP}	MD_1		For the STOP mode releasing		
$P0B_2$		MD_2					
$P0B_3$						Pull down	
$P0C_0$	Input/output	D_4		• CMOS (push-pull) 4-bit input/ output port (port 0C)		8-bit data input/output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5					
$P0C_2$		D_6					
$P0C_3$		D_7					
$P0D_0$	Input/output	D_0		• CMOS (push-pull) 4-bit input/ output port (port 0D)		8-bit data input/output pin (low-order 4-bits)	High impedance (input mode)
$P0D_1$		D_1					
$P0D_2$		D_2					
$P0D_3$		D_3					

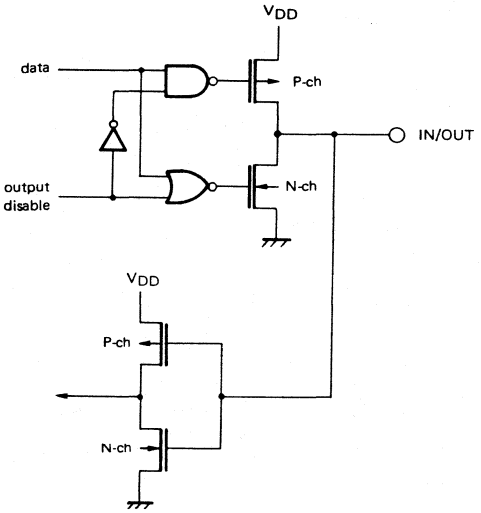
- Non-port pins

PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN	FUNCTION	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
X_{IN}			Pins to be connected to the system clock resonator	Program memory address update
X_{OUT}		MD_3	Pins to be connected to the system clock resonator	Mode selection pin
NC			NC pin is not connected internally.	

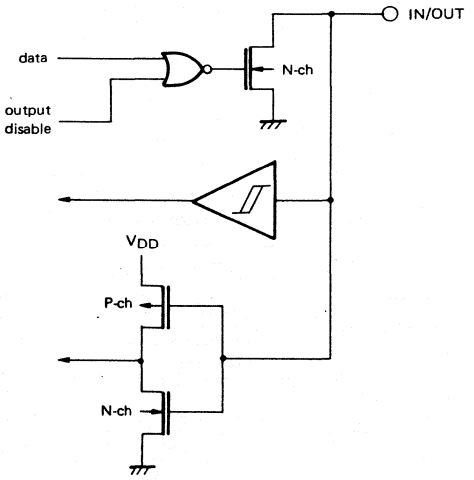
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17P104.

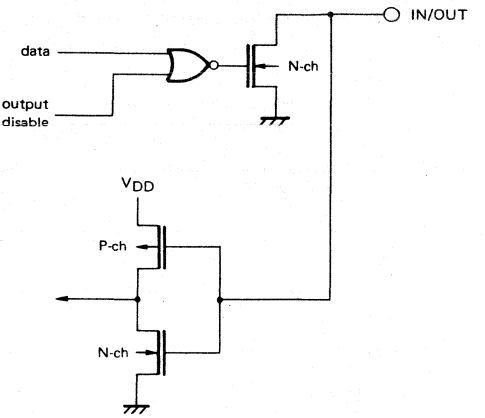
(1) P0C and P0D



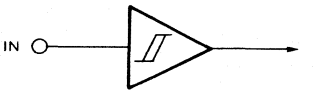
(2) $P0B_0$ and $P0B_1$



(3) POB_2 and POB_3



(4) $\overline{RESET}$



9. DIFFERENCES BETWEEN THE μPD17P104 AND μPD17104

The μPD17P104 is a one-time PROM version of the μPD17104, in which the internal mask ROM is replaced with a one-time PROM. The μPD17P104 has the same CPU functions and internal hardwares as those of μPD17104 except for its program memory and mask option. Table 9-1 lists the differences between them.

Table 9-1 Differences between μPD17P104 and μPD17104

ITEM	μPD17P104	μPD17104
ROM	One-time PROM 512 x 16 bits	Mask ROM 512 x 16 bits
Pull-up resistors of pins $P0B_0$ to $P0B_3$	None	Mask option
Pull-up resistors of $\overline{RESET}$ pin	None	Mask option
Connection pin	V_{PP} pin and operation mode selection pins are provided.	V_{PP} pin and operation mode selection pins are not provided.
Power supply	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)	
Package	22-pin plastic shrink DIP 24-pin plastic SOP	
Waiting time for the operation mode	16 clock pulses	8 clock pulses

10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P104's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X_{IN} pin.

PIN NAME	FUNCTION
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
X_{IN}	Input pin for address update clock used when writing to program memory or verifying its contents
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P104 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

OPERATING MODE SPECIFICATION						OPERATING MODE
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L (low) or H (high)

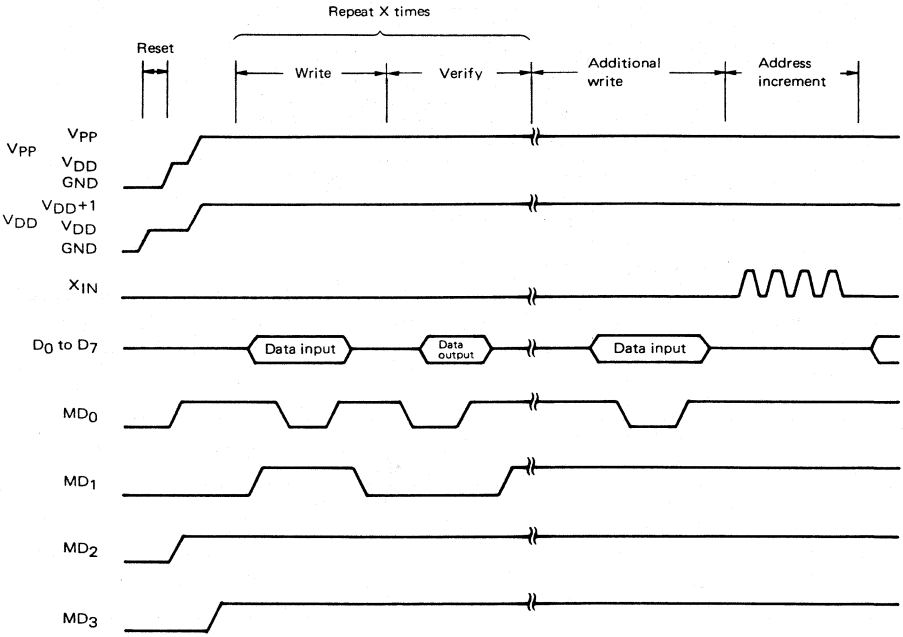
10.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) x 1 ms.
(11) Select program inhibit mode.

(12) Increment the program memory address by one on reception of four pulses on the X_{IN} pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

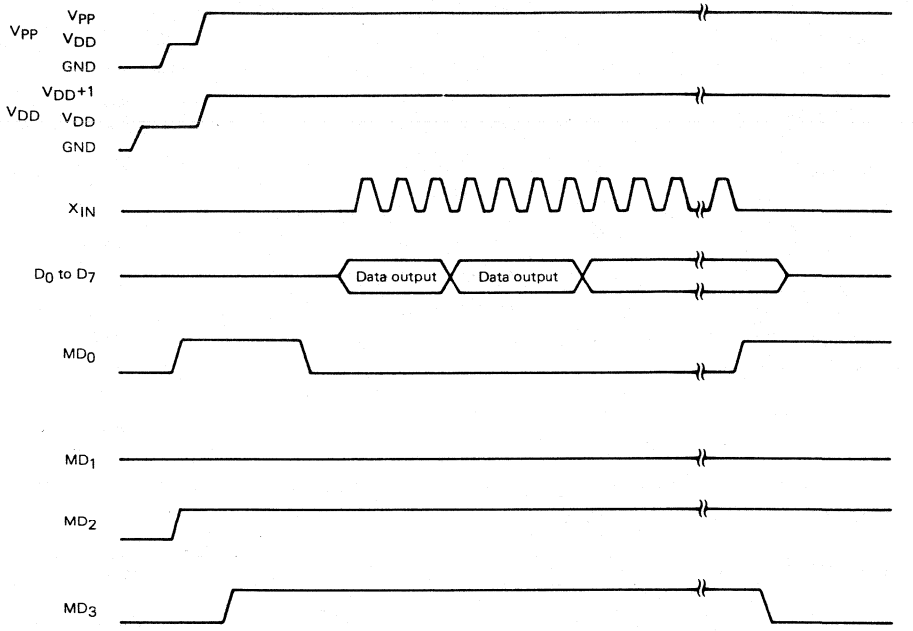
The timing for steps (2) to (12) is shown below.



10.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring X_{IN} to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the X_{IN} pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



13. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0A, P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin shrink DIP	400	mW
			24-pin SOP	250	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
I/O(*) Capacitance	C_{IO}			15	pF	

* Input/output

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B	(*)
	V_{IH4}	V_{DD}-0.5		V_{DD}	V	X_{IN}	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	X_{IN}	
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	V_{DD}-2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
		V_{DD}-1.0			V	I_{OH} = −200 μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V	(*)
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			−5	μA	V_{IN} = 0 V	
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V	(*)
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			−5	μA	V_{OUT} = 0 V	
Power Supply Current	I_{DD1}		1.5	4.5	mA	Operation mode	V_{DD} = 5 V ±10 %, f_{CC} = 8.0 MHz
			250	750	μA		V_{DD} = 3 V ±10 %, f_{CC} = 2.0 MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	V_{DD} = 5 V ±10 %, f_{CC} = 8.0 MHz
			200	600	μA		V_{DD} = 3 V ±10 %, f_{CC} = 2.0 MHz
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10 %
			0.1	5	μA		V_{DD} = 3 V ±10 %

* When N-ch open-drain input/output is selected

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Internal Clock Cycle Time	T_{CY}	1.9		33	μs	V_{DD} = 4.5 to 6.0 V
		7.6		33	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except X_{IN}
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	X_{IN}
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except X_{IN}
	V_{IL2}	0		0.4	V	X_{IN}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

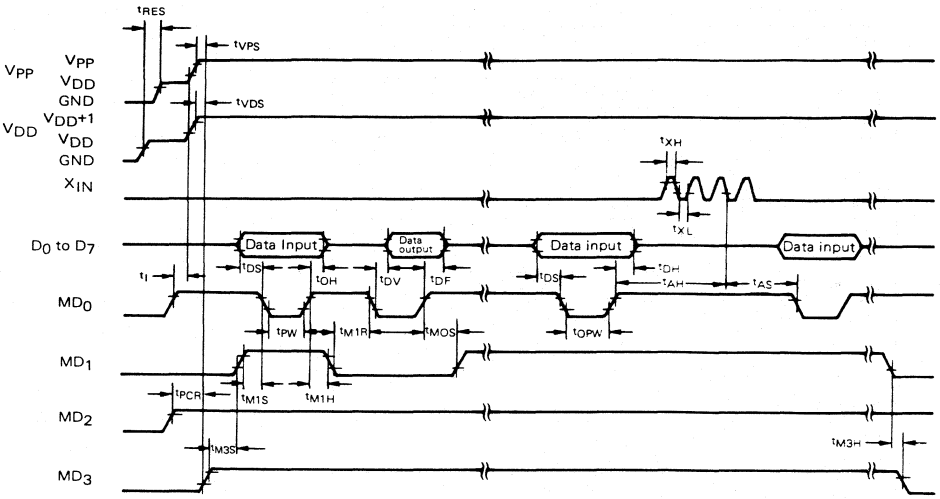
AC CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time(*2) to MD0↓	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time(*2) to MD0↑	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
X_{IN} Input High, Low Level Range	t_{XH}, t_{XL}	–	0.063			μs	
X_{IN} Input Frequency	f_X	–			8	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time from Address(*2)	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time from Address(*2)	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time from MD3↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

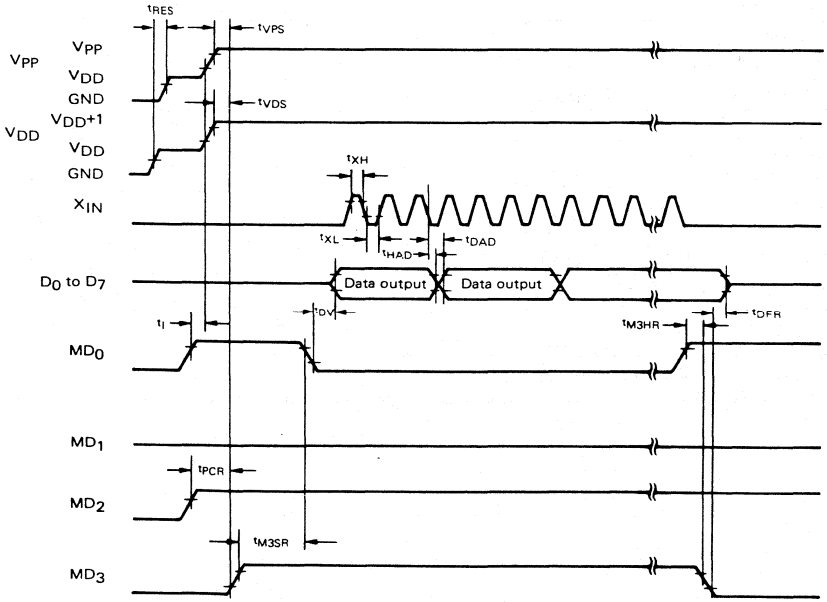
*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third X_{IN} input, and it is not connected to the pin.

WRITE PROGRAM MEMORY TIMING

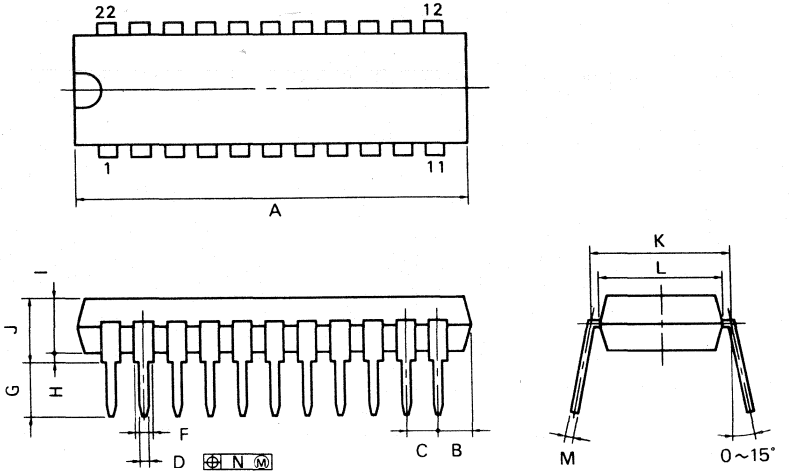


READ PROGRAM MEMORY TIMING



13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-300B

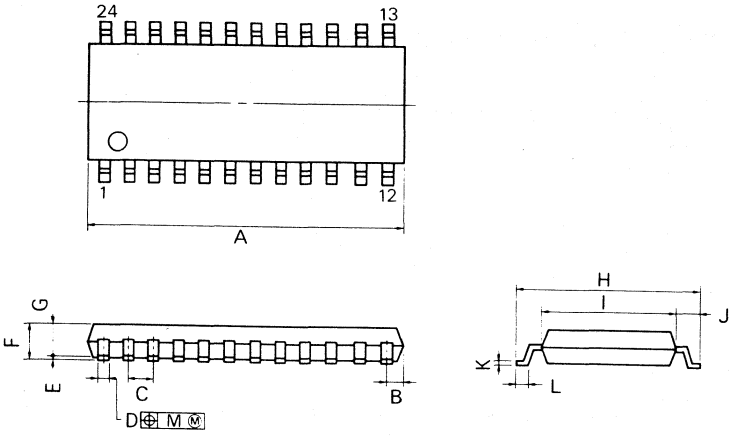
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



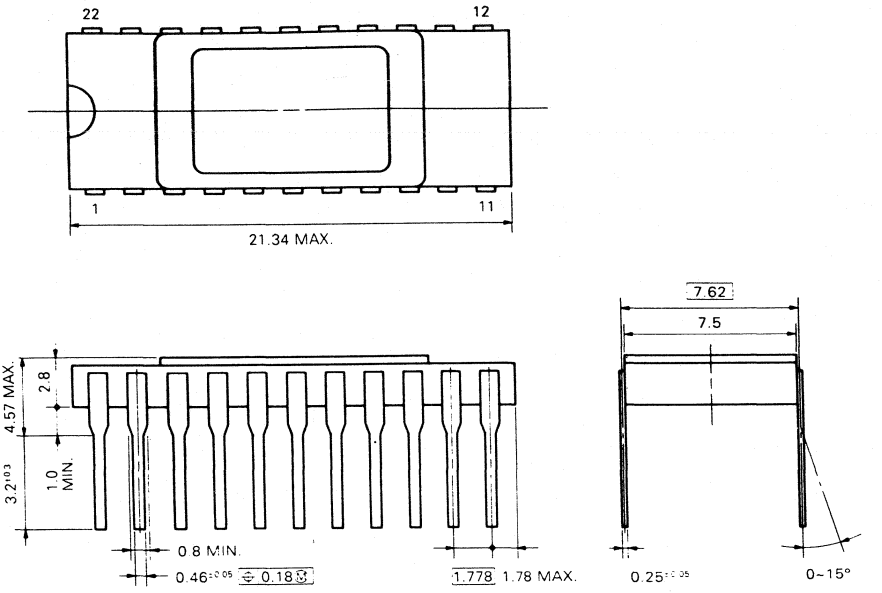
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

Package dimensions of the 22-pin ceramic of shrink DIP for ES (300 mil) (Unit: mm)



P22D-70-300B

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17107 is a tiny microcontroller consistings of ROM (512 x 16 bits), RAM (16 x 4 bit), and 11 input/output ports.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- 17 K architecture (using general resisters)
- Program memory (ROM) : 512 × 16 bits
- Data memory (RAM) : 16 × 4 bits
- Input/ output ports : 11 ports (including three N-ch open-drain outputs)
- Instruction execution time
  (recommended) : 128 μs (for 62.5 kHz) to 8 μs (for 1 MHz)
  (guaranteed) : 160 μs (for 50 kHz) to 6.6 μs (for 1.2 MHz) (Eight system clock pulses are needed to execute one instruction.)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function is supported (HALT/STOP).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An RC oscillator for the system clock:
  Capacitor built-in type (only resistor for external circuit)
- Operating supply voltage : 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

- Controlling electric appliances or toys electronically

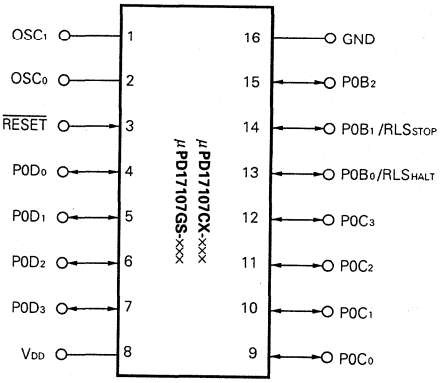
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17107CX-xxx	16-pin plastic DIP (300 mil)	Standard
μPD17107GS-xxx	16-pin plastic SOP (300 mil)	Standard

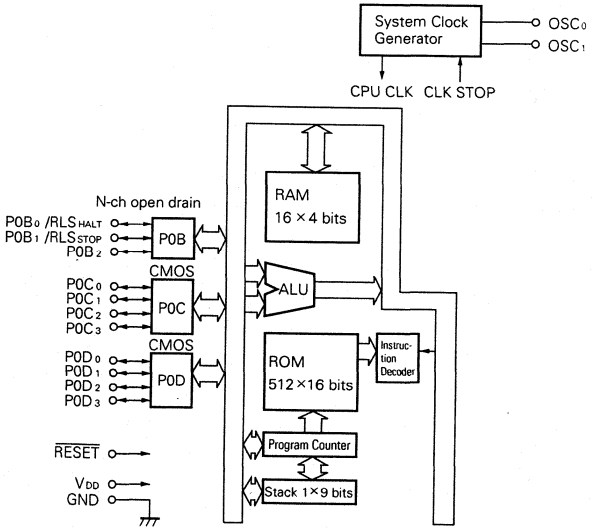
PIN CONFIGURATION (Top View)

μPD17107CX/μPD17107GS

16-pin plastic DIP
16-pin plastic SOP



BLOCK DIAGRAM of μPD17107



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

Pin name	I/O	Function	Reset
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0C_0$ to $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ to $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

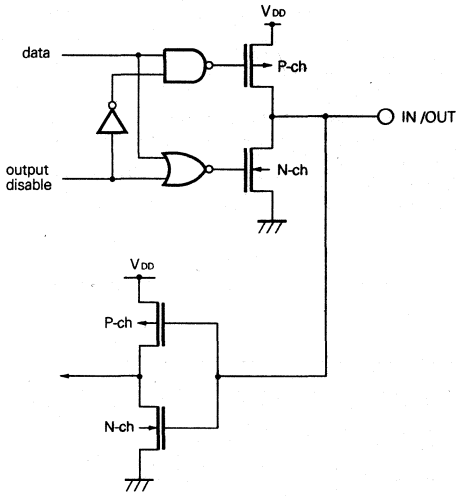
Pin name	I/O	Function	Reset
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).	
V_{DD}		• Positive power supply pin	
GND		• GND potential pin	
OSC_0, OSC_1		• Pins through which a resistor is connected to the system clock resonator	

I/O: Input/output

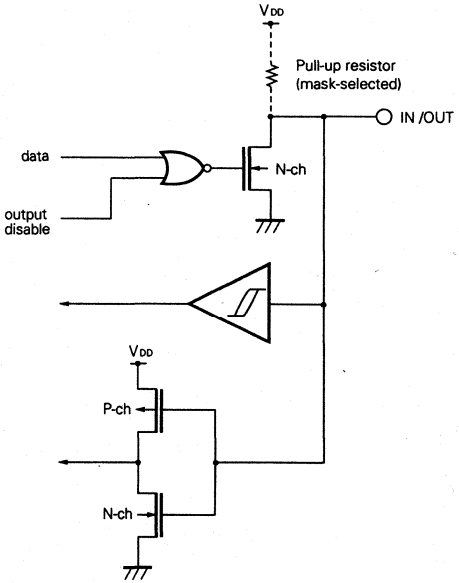
Pin Input/Output Circuits

Following are schematics of the input/output circuits of the pins of the μPD17107.

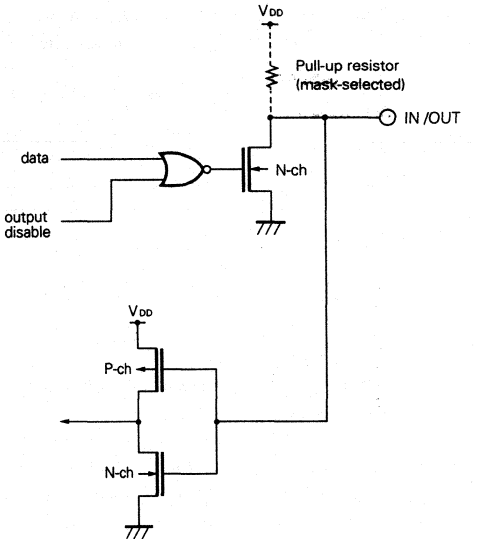
(1) P0C and P0D



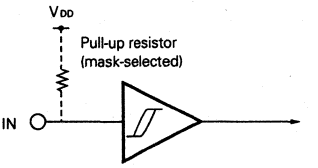
(2) P0B0 and P0B1



(3) $P0B_2$



(4) $\overline{\text{RESET}}$

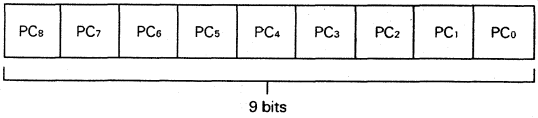


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

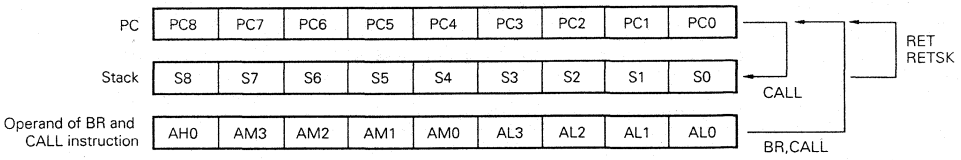
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17107 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

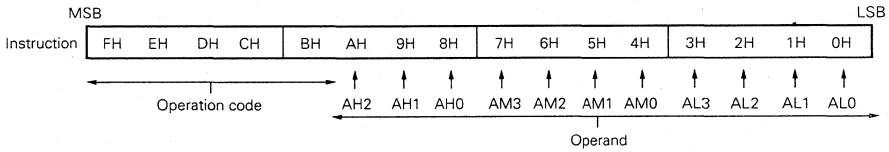
Fig. 2-1 shows the relationship between PC, stack and instructions.

Fig. 2-1 Relationship between PC, Stack, and Operands of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn (n = 0 to 3) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn (n = 0 to 8) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

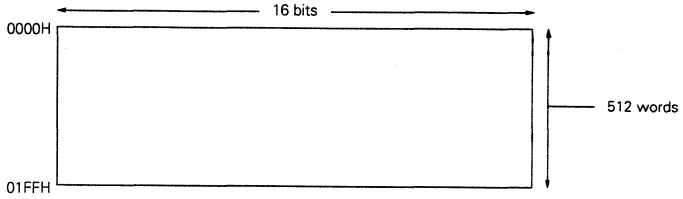
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory.

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

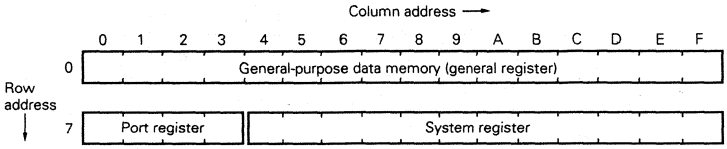
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of four bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, arithmetic operations, comparison, evaluation, and transfer between 4-bit data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17107 register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

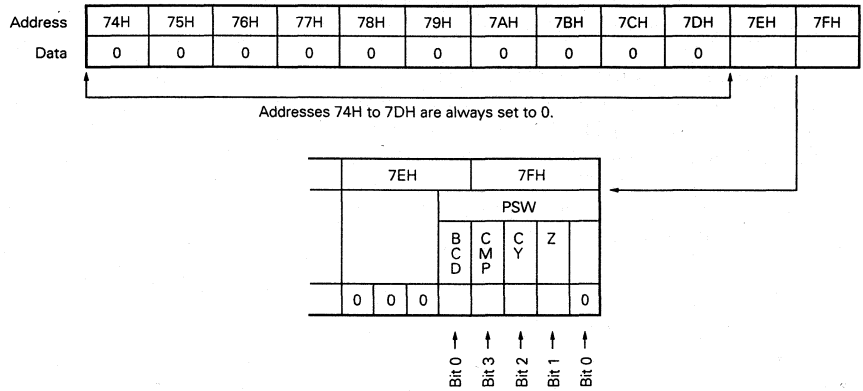
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. (The output mode is maintained until the system is reset.) Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17107.

Fig. 4-2 System Register Map

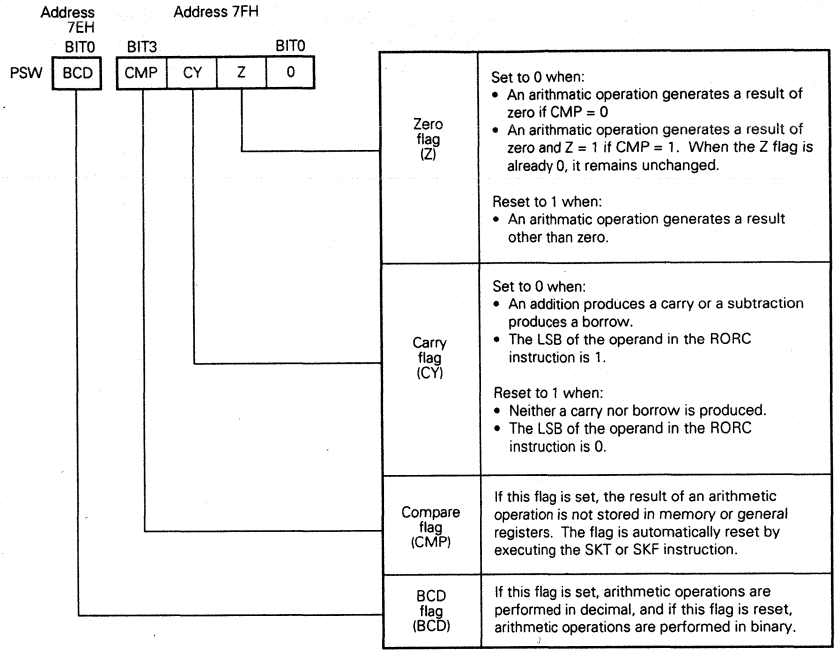


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the CY flag is mapped in bit 2 at address 7FH, and the Z flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Comparison instructions (SKE, SKNE, SKGE, and SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Z_{n-1}: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the CY flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the Z flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0B ($P0B_0$/RLS_{HALT}, $P0B_1$/RLS_{STOP}, $P0B_2$)

Port 0B is a 3-bit input/output port. Only N-ch opendrain outputs appear on the pins of port 0B. The N-ch opendrain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port 0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

An N-ch open-drain output pin which output 1 can be used for input because it enters high-impedance mode when 1 is written to the port register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port 0B consists of 4 bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17107 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to Section 7.)

6.2 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.3 PORT 0D ($P0D_0$ to $P0D_3$)

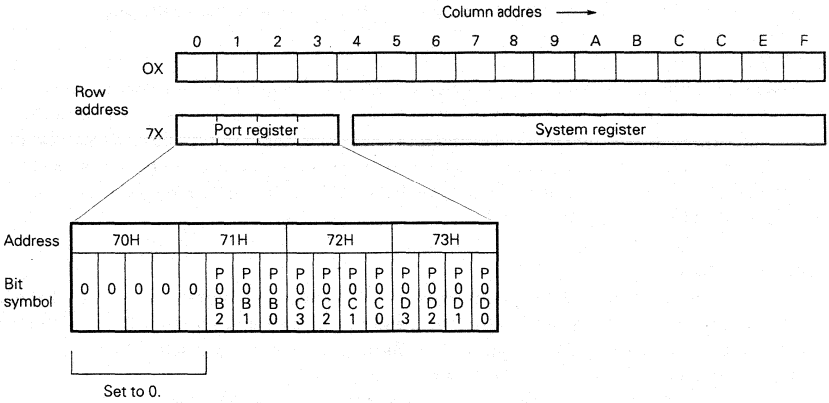
Port 0D is a 4-bit input/output port. CMOS (push-pull) output appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.4 RECOMMENDED CONDITIONS FOR UNUSED μPD17107 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports 0B to 0D	Connect to V_{DD} or GND.
Output mode	CMOS port (ports 0C and 0D)	Open
	N-ch open-drain port (port 0B)	Open after 0 is output to the port

7. STANDBY FUNCTIONS

The μPD17107 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instructions after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released on the rising edge of a signal input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000X B ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_0$ pin status is 0, executing the HALT instruction enters the HALT mode. If $P0B_0$ pin status is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

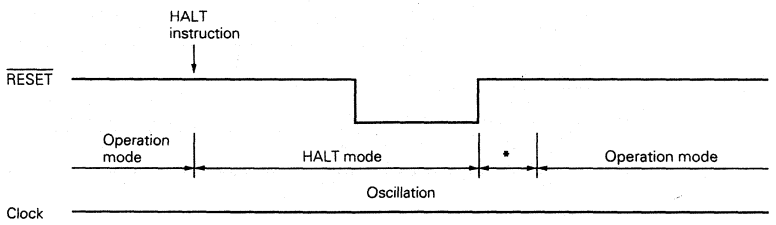
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_1$ pin status is 0, executing the STOP instruction enters the STOP mode. If $P0B_1$ pin status is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{RESET}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 Timing for Releasing the Standby Modes

Fig. 7-1 Releasing the HALT Mode by $\overline{RESET}$ Input



When the $\overline{RESET}$ signal is applied to release the HALT mode, the $\overline{RESET}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
  At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

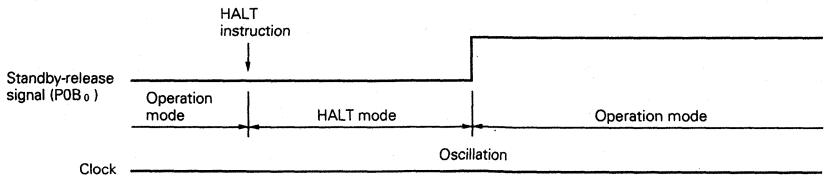
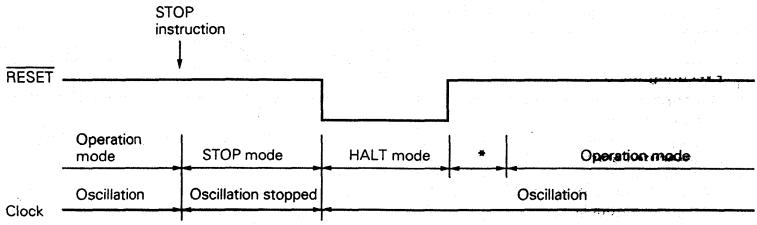


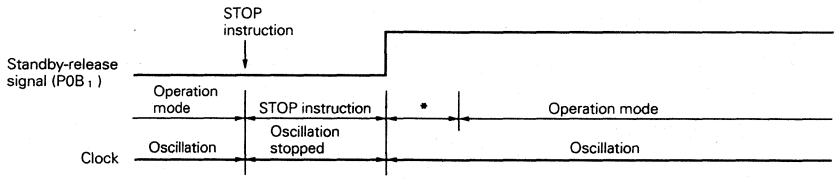
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin release the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	00H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0B to 0D	71H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17107 must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17107. OPT file in AS17107 (device file for the μPD17107) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instruction listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTION		[; comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_2$ to $P0B_0$	OPTP0B	3	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTP0B	($P0B_2$), ($P0B_1$), ($P0B_0$)	[; comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTRES	($\overline{\text{RESET}}$)	[; comment]

Example To set the following mask options in a μPD17107 source file to be assembled:

$P0B_2$:	Pull-up	$P0B_1$:	Open
$P0B_0$:	Open	$\overline{\text{RESET}}$:	Pull-up

```
                    ⋮
; 17107
  Setting mask options:  OPTION
                         OPTP0B P0BPLUP, OPEN, OPEN
                         OPTRES RESPLUP
                         ENDOP
                    ⋮
```

9.2 RESERVED WORDS

Table 9-2 lists the reserved words defined in the μPD17107 device file (AS17107).

Table 9-2 Reserved Words

Name	Attribute	Value	Read/write	Description
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3 *	FLG	0.71H.3	Read	Set to 0.
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

* Although there is no pin corresponding to P0B3 in the μPD17107, it is defined as a read-only flag so that it is treated as a dummy bit when a built-in macro is used.

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b14 – b11 \ b15		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M : One of data memory
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (row address) ; 3 bits
m_L : Data memory address low (column address) ; 4 bits
R : One of general register specified by [(RP), r]
r : General register address low (column address); 4 bits
RP : General register pointer
PC : Program counter
SP : Stack pointer
STACK: Stack specified by (SP)
i : Immediate data; 4 bits
n : Bit position; 4 bits
addr : One of program memory address; 11 bits
a_H : Program memory address high; 3 bits
a_M : Program memory address middle ; 4 bits
a_L : Program memory address low ; 4 bits
CY : Carry flag
CMP : Compare flag
s : Stop release condition
h : Halt release condition
[ ] : Address of M, R
( ) : Contents of M, R

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to resister	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r, m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M–i skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M–i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M–i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M–i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) −1, STACK ← ((PC) + 1), PC ← ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note1**	−0.3 to V_{DD} + 0.3	
			Note2	−0.3 to +11	
Output Voltage	V_O	P0C, P0D		−0.3 to V_{DD} + 0.3	V
		P0B	**Note1**	−0.3 to V_{DD} + 0.3	
			Note2	−0.3 to +11	
High-Level Output Current	I_{OH}	Each of P0B, P0C, and P0D		−5	mA
		Total of all pins		−15	
Low-Level Output Current	I_{OL}	Each of P0B, P0C, and P0D		30	mA
		Total of all pins		100	
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C	16-pin plastic DIP	400	mW
			16-pin plastic SOP	190	

Note 1. When a built-in pull-up resistor is selected as mask option
2. When a built-in pull-up resistor is not selected as mask option.

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
Input Output Capacitance	C_{IO}			15	pF	

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
System Clock Oscillation Frequency	f_{CC}	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 24 kΩ	800	1000	1200	kHz
		V_{DD} = 2.7 to 3.3 V, R_{OSC} = 100 kΩ	200	250	300	kHz
		V_{DD} = 2.5 to 6.0 V, R_{OSC} = 100 kΩ	150	250	300	kHz

Note The above conditions do not allow a resistance error.

DC CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note3**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note 4**
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0C, P0D	
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.2 V_{DD}	V	P0B	
High-Level Output Voltage	V_{OH}	V_{DD} −2.0			V	P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
		V_{DD} −1.0			V	P0C, P0D I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL}			2.0	V	P0B, P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 3**
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V **Note 4**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0C, P0C, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V **Note 4**	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 3**
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V **Note 4**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0B, P0C, P0D, V_{OUT} = 0. V	
Pull -Up Resistor Provided for $\overline{RESET}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note 5**	I_{DD1}		0.4	1.2	mA	Operation mode	V_{DD} = 5 V ± 10 %, f_{CC} = 1.0 MHz ± 20 %
			50	150	μA	Operation mode	V_{DD} = 3 V ± 10 % f_{CC} = 250 kHz ± 20 %
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ± 10 % f_{CC} = 1.0 MHz ± 20 %
			40	120	μA	HALT mode	V_{DD} = 3 V ± 10 % f_{CC} = 250 kHz ± 20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ± 10 %
			0.1	5	μA	STOP mode	V_{DD} = 3 V ± 10 %

Note 3. When a built-in pull-up resistor is selected as mask option

4. When a built-in pull-up resistor is not selected as mask option

5. This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS of DATA MEMORY for HOLDING DATA on LOW SUPPLY VOLTAGE in the STOP MODE
(T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data hold supply voltage	V_{DDDR}	2.0		6.0	V	
Data hold supply current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V

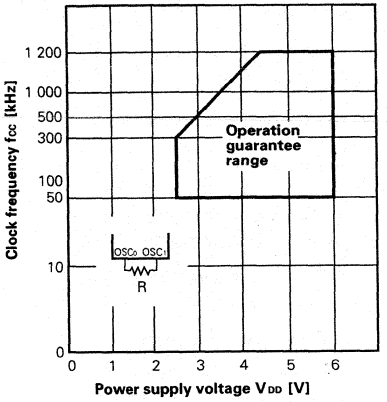
AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Level Width on P0B0 and P0B1	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{\text{RESET}}$	T_{RSH} T_{RSL}	10			μs	

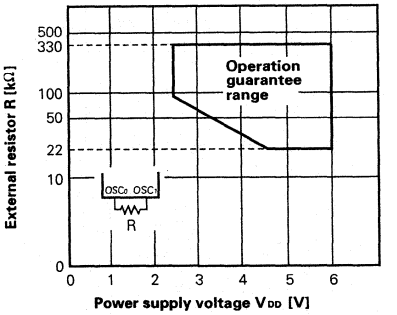
Remark tcy/fcc (fcc: System clock oscillator frequency)

12. CHARACTERISTICS CURVE

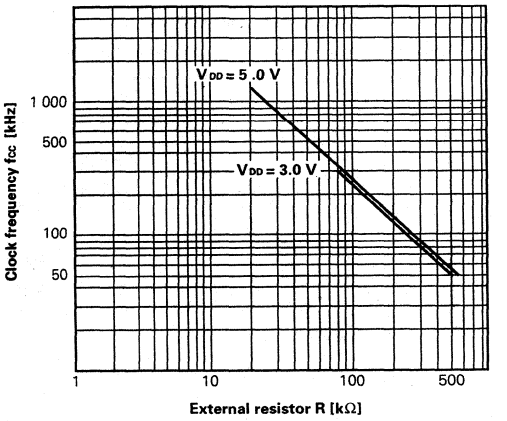
f_{CC} vs. V_{DD} operation guarantee range (T_a = –40 to +85 °C)



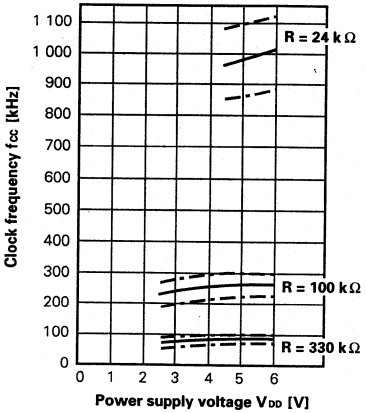
R vs. V_{DD} operation guarantee range (T_a = –40 to +85 °C)



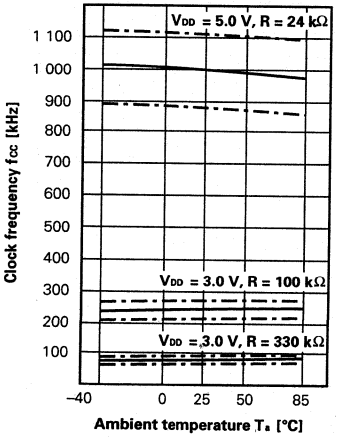
Example of f_{CC} vs. R characteristics (T_a = 25 °C)



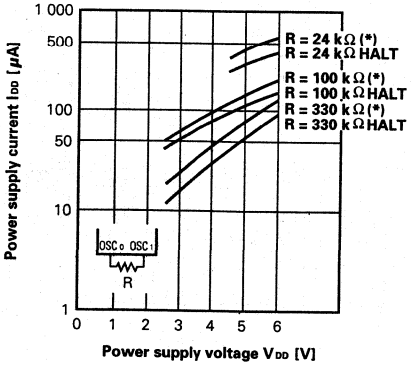
Example of f_{CC} vs. V_{DD} characteristics (T_a = –40 to + 85 °C)



Example of f_{CC} vs. T_a characteristics



Example of I_{DD} vs. V_{DD} characteristics (T_a = 25 °C)

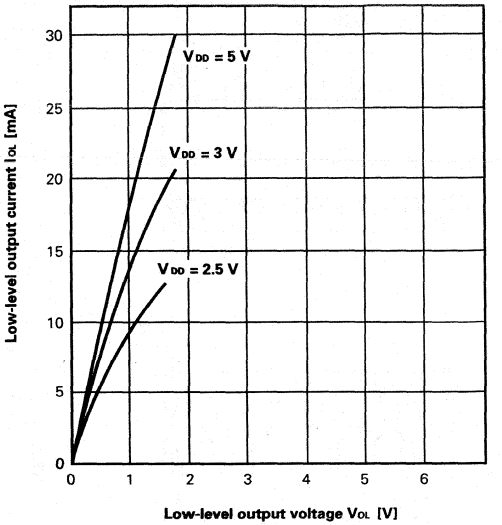


* Operation

Remark

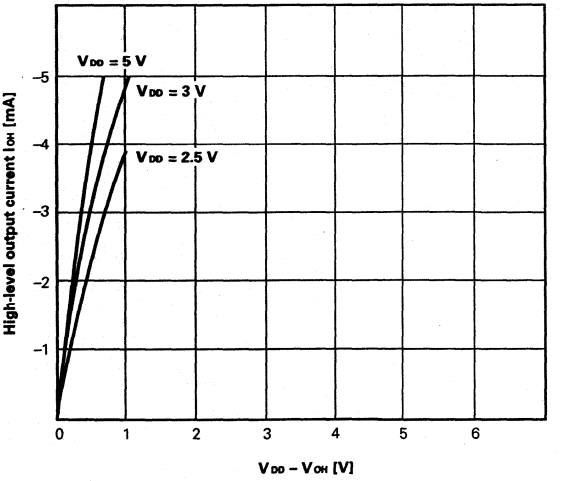
The characteristics curves are reference values unless otherwise indicated as "guarantee range."

Example of I_{OL} vs. V_{OL} characteristics (T_a = 25 °C)



Caution The absolute maximum rated current is 30 mA per pin.

Example of I_{OH} vs. V_{OH} characteristics (T_a = 25 °C)

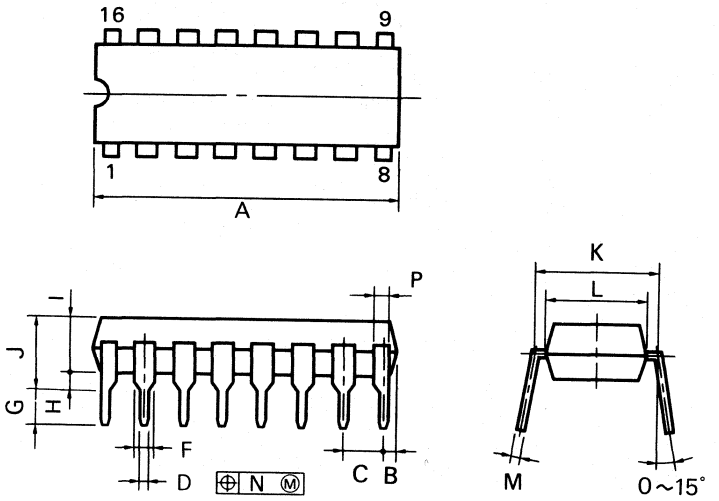


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values unless otherwise indicated as "guarantee range."

13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

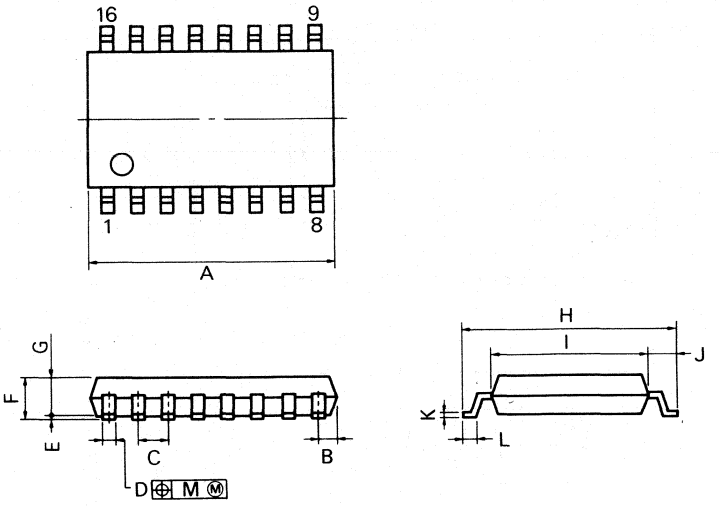
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{+0.3}$	$0.138^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



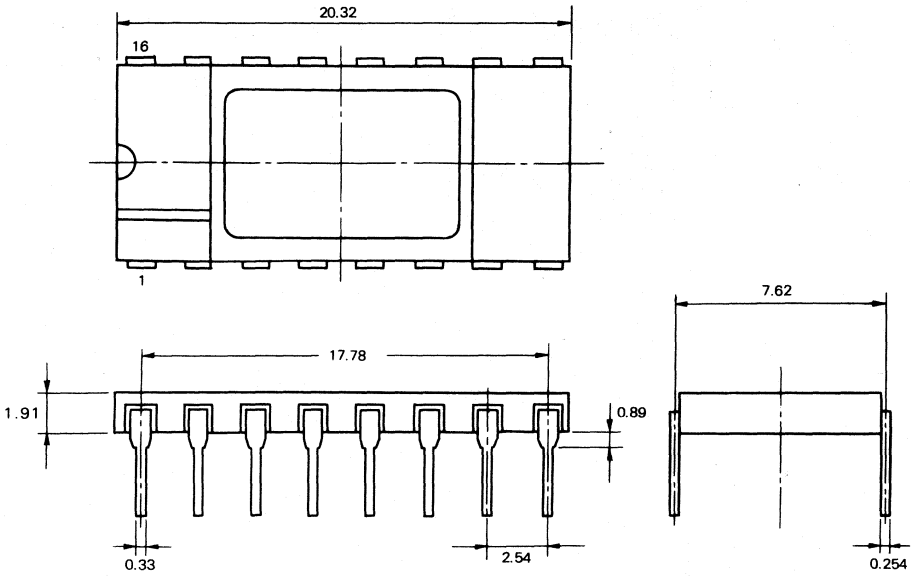
P16GM-50-300B-1

NOTE

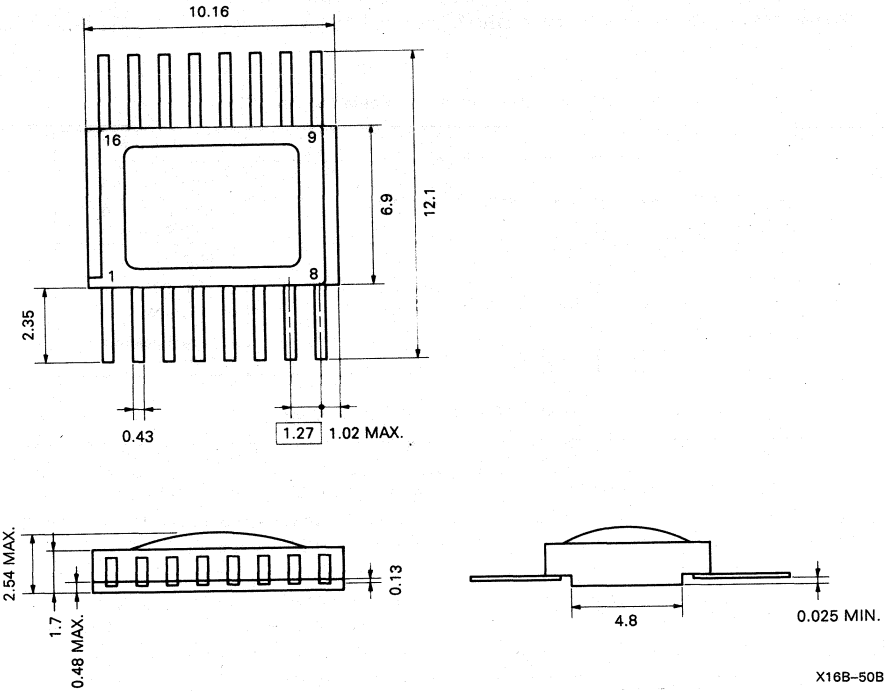
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

PACKAGE DIMENSION FOR ENGINEERING SAMPLE 16-PIN CERAMIC DIP (for reference) (Unit: mm)



PACKAGE DIMENSION FOR ENGINEERING SAMPLE 16-PIN CERAMIC SOP (for reference) (Unit: mm)



X16B-50B

14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17107.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17107CX-xxx	16-pin plastic DIP (300 mil)	• Wave soldering • Partial heating method
μPD17107GS-xxx	16-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below Number of flow process: 1
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions, refer to our document "SMT MANUAL" (IEI-1207).

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	[redacted]	μPD17108	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of input/output port pins Note	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0V (at 2MHz) 4.5 to 6.0V (at 8MHz)		1.8 to 3.6V (at 2MHz)		2.5 to 6.0V (at 250kHz) 4.5 to 6.0V (at 1MHz)		1.5 to 3.6V (at 200kHz)	
Package	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP	•16-pin DIP •16-pin SOP	•22-pin shrink DIP •24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

Note A number in parentheses indicates the number of the N-ch opendrain outputs for each of which a pull-up resistor may or may not be provided depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17108 is a tiny microcontroller consistings of ROM (512 × 16 bits), RAM (16 × 4 bits), and 16 input/output ports.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- 17K architecture (using general registers)
- Program memory (ROM) : 512 × 16 bits
- Data memory (RAM) : 16 × 4 bits
- Input/ output ports : 16 ports (including four N-ch open-drain outputs)
- Instruction execution time
  (recommended) : 128 μs (for 62.5 kHz) to 8 μs (for 1 MHz)
  (guaranteed) : 160 μs (for 50 kHz) to 6.6 μs (for 1.2 MHz) (Eight system clock pulses are needed to execute one instruction.)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function is supported (HALT/STOP).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An RC oscillator for the system clock:
  Capacitor built-in type (only resistor for external circuit)
- Operating supply voltage : 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

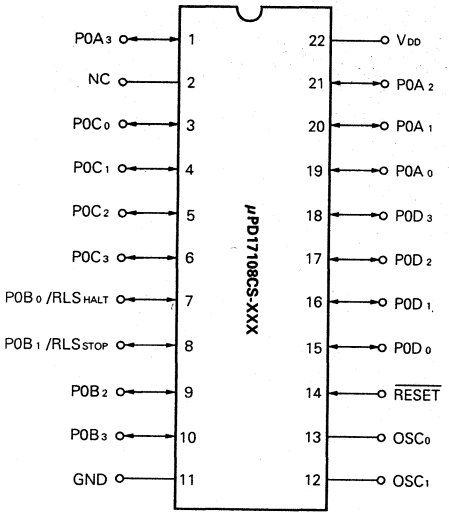
- Controlling electric appliances or toys electronically

ORDERING INFORMATION

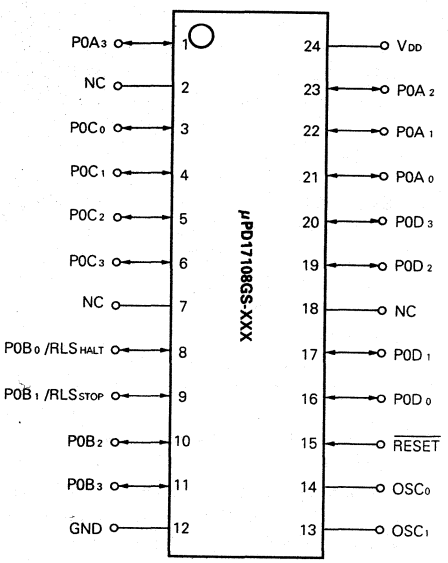
Order Code	Package	Quality Grade
μPD17108CS–xxx	22-pin plastic shrink DIP (300 mil)	Standard
μPD17108GS-xxx	24-pin plastic SOP (300 mil)	Standard

PIN CONFIGURATION (Top View)

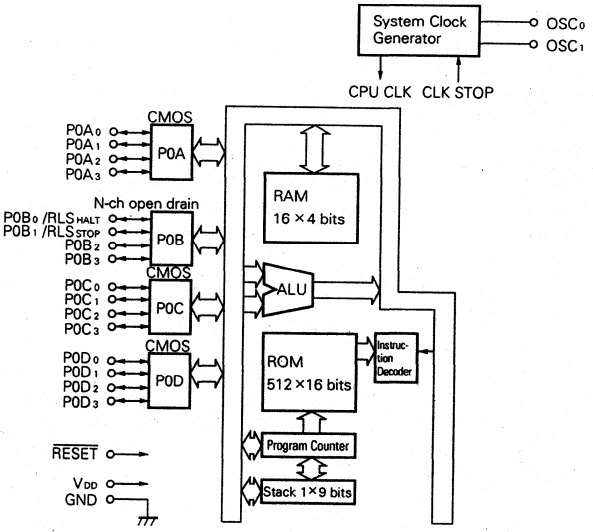
22-pin plastic shrink DIP



24-pin plastic SOP



BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTIONS

- Port pins

Pin name	I/O	Function	Reset
$P0A_0$ to $P0A_3$	I/O	• CMOS (push-pull) 4-bit I/O port (port 0A)	High impedance (input mode)
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0B_3$			
$P0C_0$ to $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ to $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

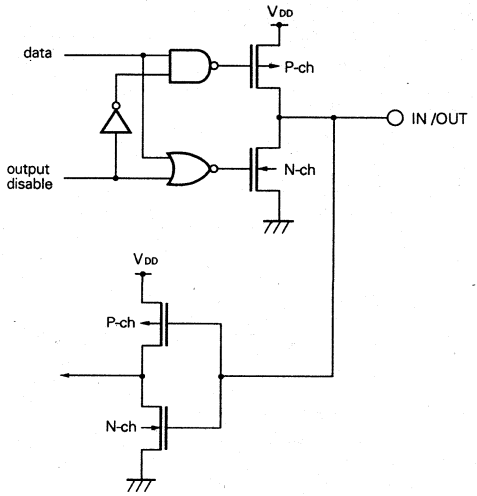
Pin name	I/O	Function	Reset
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).	
V_{DD}		• Positive power supply pin	
GND		• GND potential pin	
OSC_0, OSC_1		• Pins through which resister is connected to the system clock resonator	

I/O: Input /output

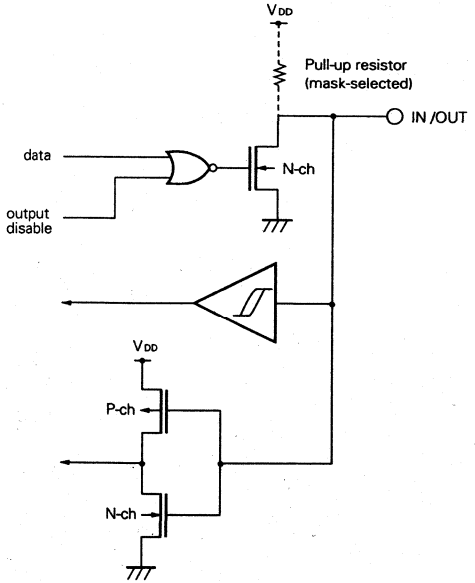
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/output circuits of the pins of the μPD17108.

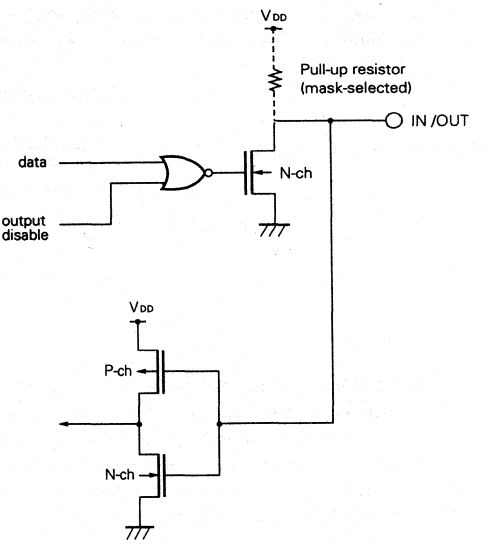
(1) P0A, P0C and P0D



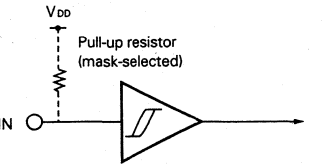
(2) P0B0 and P0B1



(3) $P0B_2$ and $P0B_3$



(4) $\overline{\text{RESET}}$

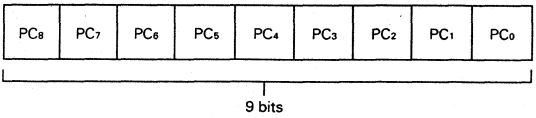


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

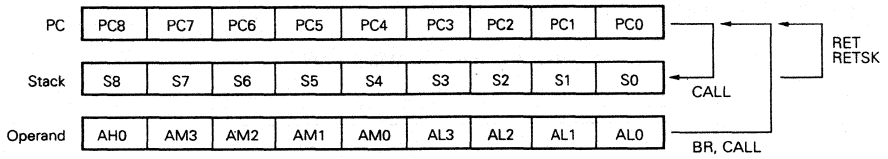
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17108 is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

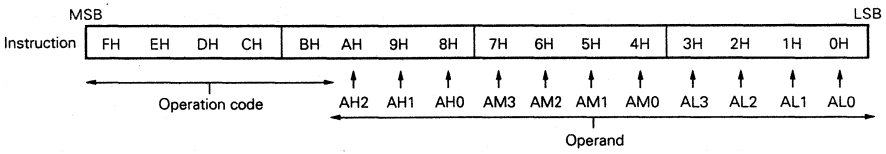
Fig. 2-1 shows the relationship between PC, stack and instructions.

Fig. 2-1 Relationship between PC, Stack, and Instructions



In Fig. 2-1, AHn, AMn, and ALn (n = 0 to 3) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn (n = 0 to 8) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

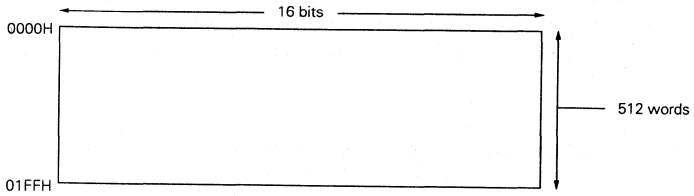
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory.

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

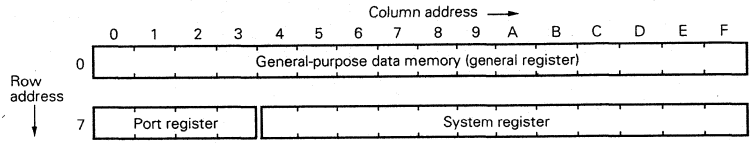
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, arithmetic operations, comparison, evaluation, and transfer between 4-bit data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17108 register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

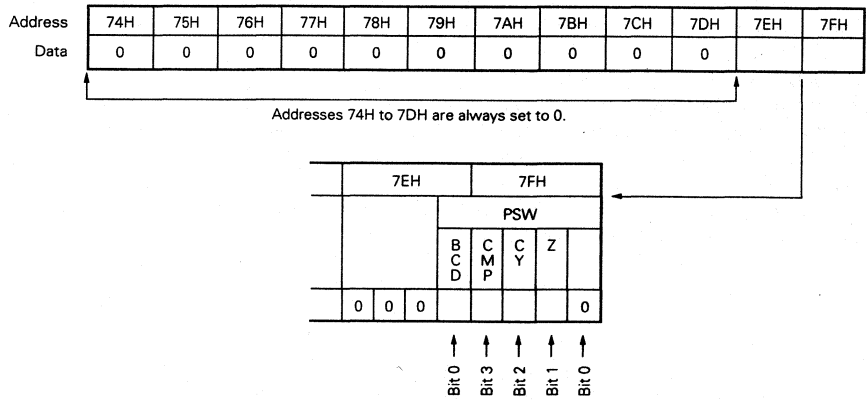
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17108.

Fig. 4-2 System Register Map

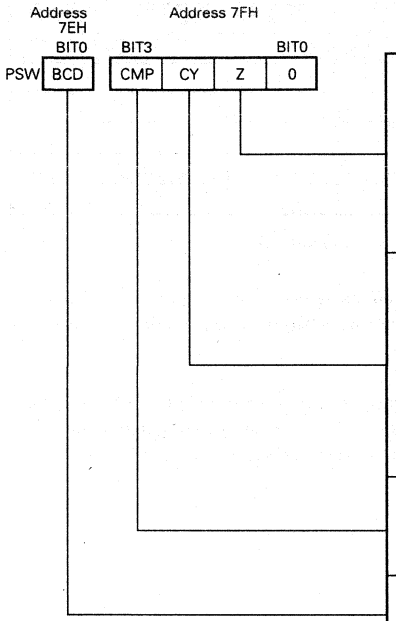


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the CY flag is mapped in bit 2 at address 7FH, and the Z flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, and SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Remark Z_{n-1}: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the CY flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero Z flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0A ($P0A_0$ to $P0A_3$)

Port 0A is 4-bit input/output port. CMOS (push-pull) output appear on those pins.

Input and output are set in units of nibbles. The input mode is set are reset, and the output mode is set by writing data to the port register in address 70H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0A are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.2 PORT 0B ($P0B_0$/RLS_{HALT}, $P0B_1$/RLS_{STOP}, $P0B_2$, $P0B_3$)

Port 0B is a 4-bit input/output port. Only N-ch opendrain outputs appear on the pins of port 0B. The N-ch opendrain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port 0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

An N-ch open-drain output pin which outputs 1 can be used for input because it enters high-impedance mode when 1 is written to the port register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

When the μPD17108 is in the HALT or STOP mode, $P0B_0$ and $P0B_1$ function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to Section 7.)

6.3 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.4 PORT 0D ($P0D_0$ to $P0D_3$)

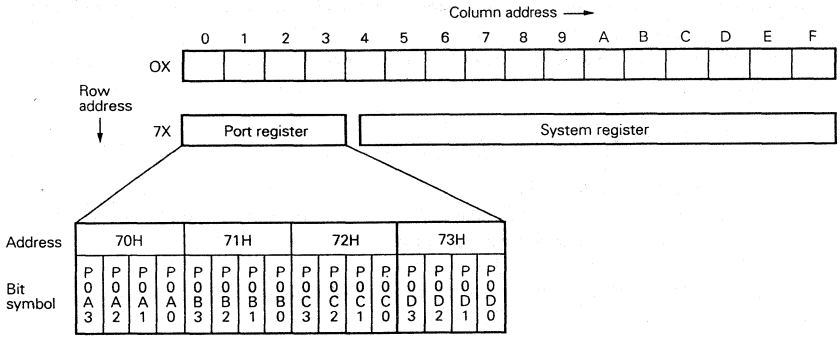
Port 0D is a 4-bit input/output port. CMOS (push-pull) output appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.5 RECOMMENDED CONDITIONS FOR UNUSED μPD17108 PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports 0A to 0D	Connect to V_{DD} or GND.
Output mode	CMOS port (ports 0A, 0C, and 0D)	Open
	N-ch open-drain port (port B)	Open after 0 is output to the port

7. STANDBY FUNCTIONS

The μPD17108 provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released on the rising edge of a signal input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting/releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_0$ pin status is 0, executing the HALT instruction enters the HALT mode. If $P0B_0$ pin status is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

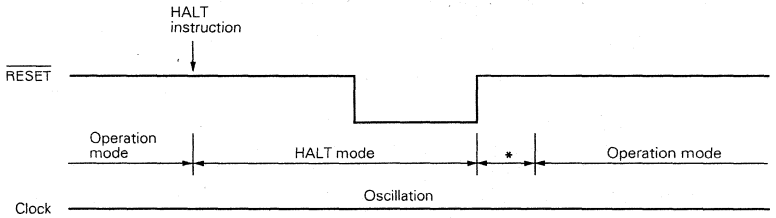
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

STOP 000X B ← 4-bit data in the operand

X	Conditions for setting/releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If $P0B_1$ pin status is 0, executing the STOP instruction enters the STOP mode. If $P0B_1$ pin status is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the $P0B_1$ pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

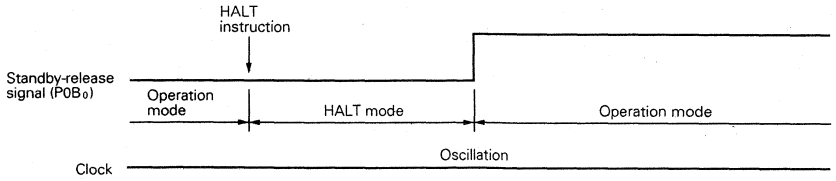
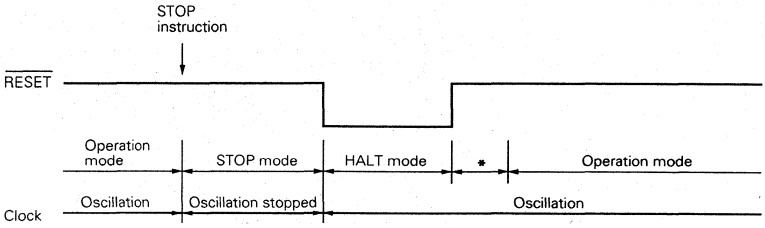


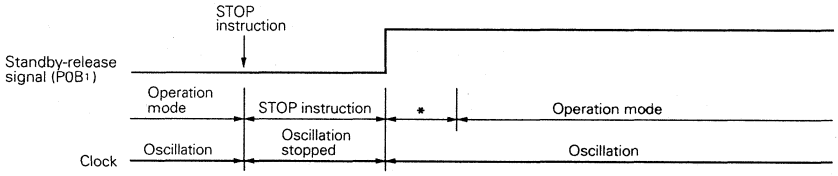
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin release the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	00H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bits 3 to 1 at 7FH	All 0s
Ports 0A to 0D	70H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17108 must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17108. OPT file in AS17108 (device file for the μPD17108) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instruction listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTION		[; comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_2$ to $P0B_0$	OPTP0B	4	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_3$, $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTP0B	($P0B_3$), ($P0B_2$), ($P0B_1$), ($P0B_0$)	[; comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTRES	($\overline{\text{RESET}}$)	[; comment]

Example To set the following mask options in a μPD17108 source file to be assembled:

$P0B_3$:	Pull-up	$P0B_2$:	Pull-up
$P0B_1$:	Open	$P0B_0$:	Open
$\overline{\text{RESET}}$:	Pull-up		

```
                    ⋮
; 17108
  Setting mask options:   OPTION
                          OPTP0B P0BPLUP, P0BPLUP, OPEN, OPEN
                          OPTRES RESPLUP
                          ENDOP
                    ⋮
```

9.2 RESERVED WORDS

Table 9-2 lists the reserved words defined in the μPD17108 device file (AS17108).

Table 9-2 Reserved Words

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b14 – b11 \ b15		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M : One of data memory
m : Data memory address specified by [m_H, m_L] of each bank
m_H : Data memory address high (row address) ; 3 bits
m_L : Data memory address low (column address) ; 4 bits
R : One of general register specified by [(RP), r]
r : General register address low (column address); 4 bits
RP : General register pointer
PC : Program counter
SP : Stack pointer
STACK: Stack specified by (SP)
i : Immediate data; 4 bits
n : Bit position; 4 bits
addr : One of program memory address; 11 bits
a_H : Program memory address high; 3 bits
a_M : Program memory address middle ; 4 bits
a_L : Program memory address low ; 4 bits
CY : Carry flag
CMP : Compare flag
s : Stop release condition
h : Halt release condition
[ ] : Address of M, R
( ) : Contents of M, R

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to resister	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r, m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M–i skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M–i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M–i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M–i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) −1, STACK ← ((PC) + 1), PC ← ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, and P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, and P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C	22-pin plastic shrink DIP	400	mW
			24-pin plastic SOP	250	

Note 1. When a built-in pull-up resistor is selected as mask option

2. When a built-in pull-up resistor is not selected as mask option

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
Input Output Capacitance	C_{IO}			15	pF	

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
System Clock Oscillation Frequency	f_{CC}	800	1000	1200	kHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 24 kΩ
		200	250	300	kHz	V_{DD} = 2.7 to 3.3 V, R_{OSC} = 100 kΩ
		150	250	300	kHz	V_{DD} = 2.5 to 6.0 V, R_{OSC} = 100 kΩ

Note The above conditions do not allow a resistance error.

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note 3**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note 4**
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0C, P0D	
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.2 V_{DD}	V	P0B	
High-Level Output Voltage	V_{OH}	V_{DD} −2.0			V	P0A, P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
		V_{DD} −1.0			V	P0A, P0C, P0D I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL}			2.0	V	P0A, P0B, P0C, P0D V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	P0A, P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0A, P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 3**
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V **Note 4**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0A, P0C, P0C, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V **Note 4**	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0A, P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 3**
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V **Note 4**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, V_{OUT} = 0 V	
Pull -Up Resistor Provided for $\overline{RESET}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note 5**	I_{DD1}		0.4	1.2	mA	Operation mode	V_{DD} = 5 V ± 10 %, f_{CC} = 1.0 MHz ± 20 %
			50	150	μA	Operation mode	V_{DD} = 3 V ± 10 % f_{CC} = 250 kHz ± 20 %
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ± 10 % f_{CC} = 1.0 MHz ± 20 %
			40	120	μA	HALT mode	V_{DD} = 3 V ± 10 % f_{CC} = 250 kHz ± 20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ± 10 %
			0.1	5	μA	STOP mode	V_{DD} = 3 V ± 10 %

Note 3. When a built-in pull-up resistor is selected as mask option

4. When a built-in pull-up resistor is not selected as mask option

5. This current excludes the current which flows through the built-in pull-up resistors.

CHARACTERISTICS of DATA MEMORY for HOLDING DATA on LOW SUPPLY VOLTAGE in the STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data hold supply voltage	V_{DDDR}	2.0		6.0	V	
Data hold supply current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V

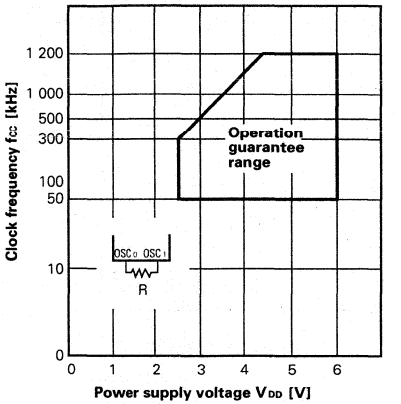
AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Lavel Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

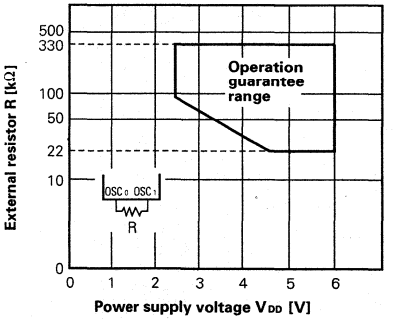
Remark t_{CY} = 8/fcc (fcc: System clock oscillator frequency)

12. CHARACTERISTICS CURVE

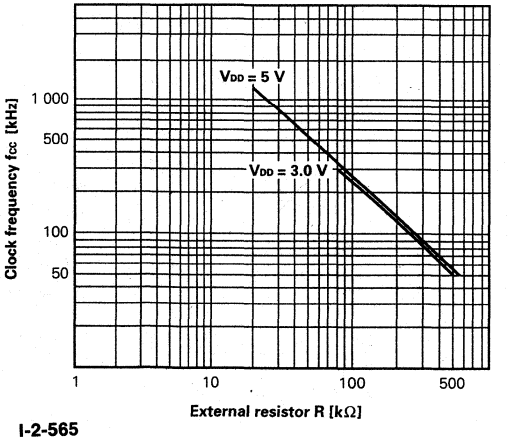
f_{CC} vs. V_{DD} operation guarantee range (T_a = −40 to +85 °C)



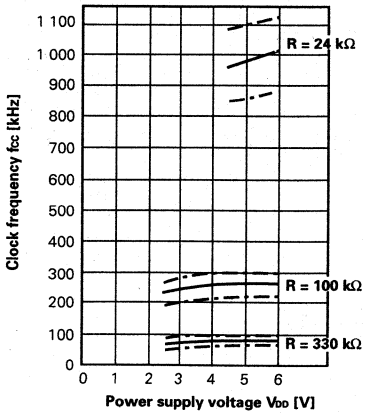
R vs. V_{DD} operation guarantee range (T_a = −40 to +85 °C)



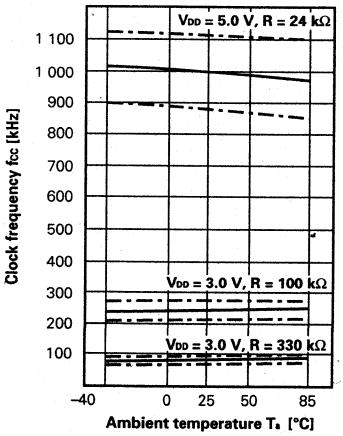
Example of f_{CC} vs. R characteristics (T_a = 25 °C)



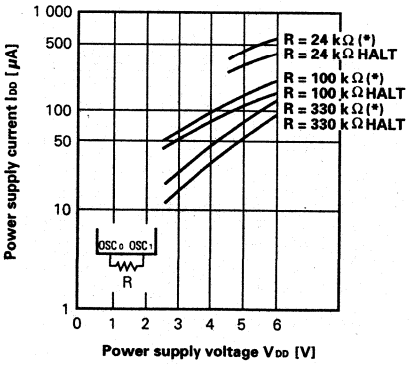
Example of f_{CC} vs. V_{DD} characteristics (T_a = −40 to + 85 °C)



Example of f_{CC} vs. T_a characteristics



Example of I_{DD} vs. V_{DD} characteristics (T_a = 25 °C)

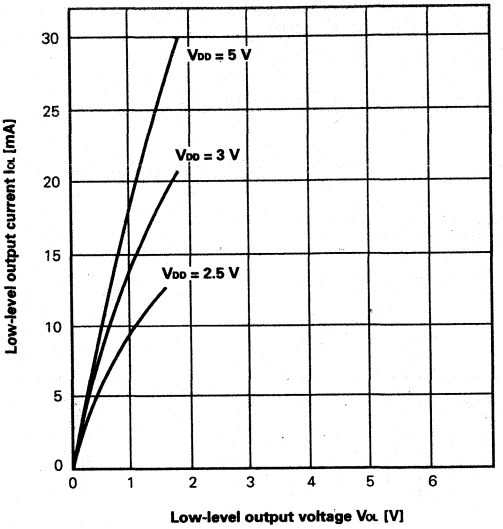


* Operation

Remark

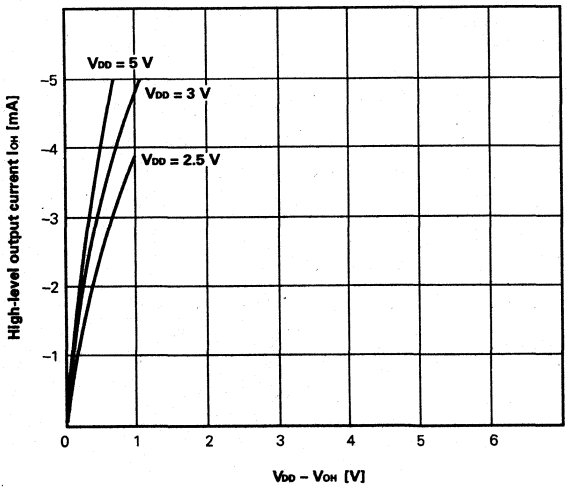
The characteristics curves are reference values unless otherwise indicated as "guarantee range."

Example of I_{OL} vs. V_{OL} characteristics (T_a = 25 °C)



Caution The absolute maximum rated current is 30 mA per pin.

Example of I_{OH} vs. V_{OH} characteristics (T_a = 25 °C)

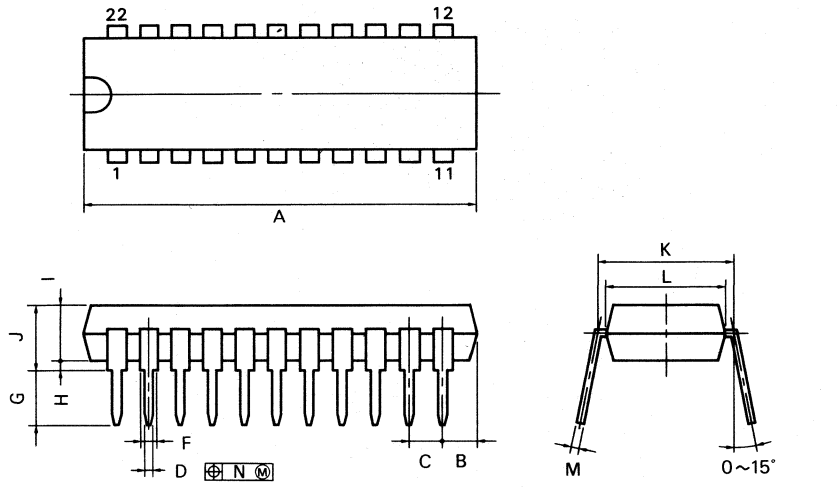


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values unless otherwise indicated as "guarantee range."

13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-300B

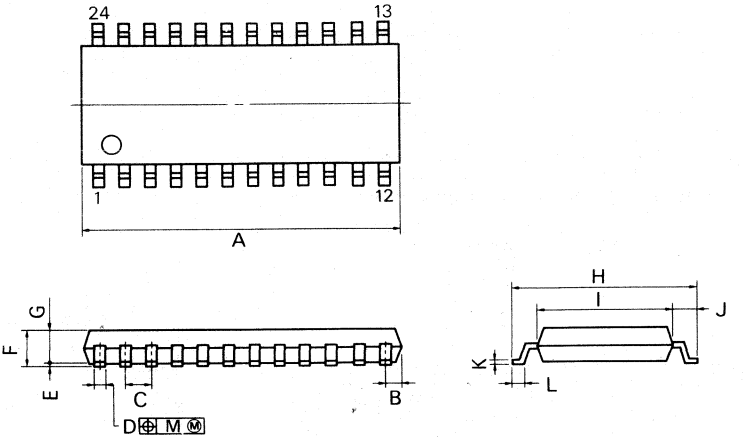
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



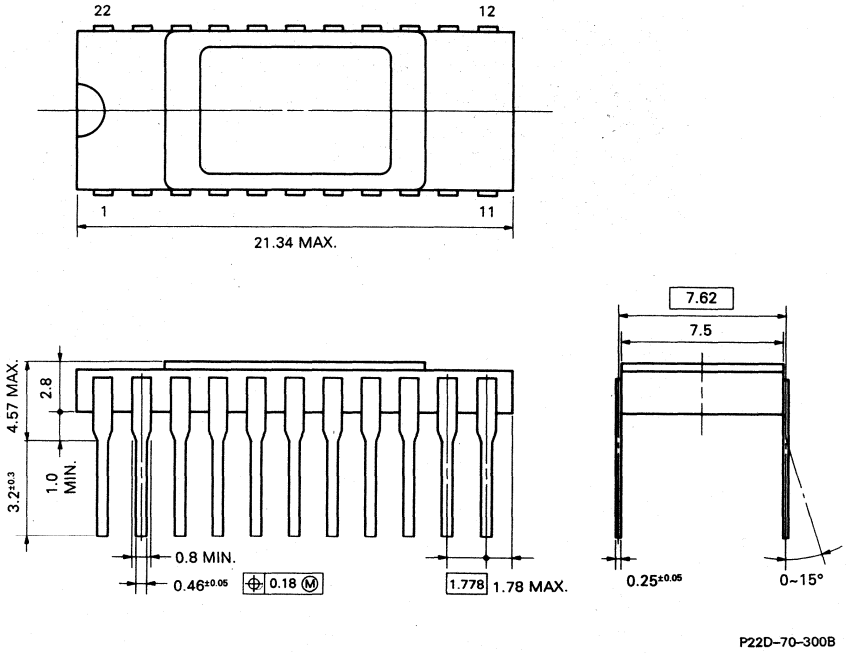
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

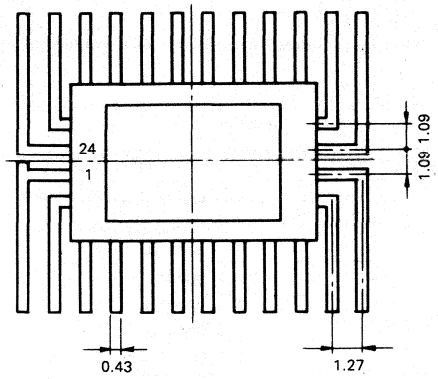
ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

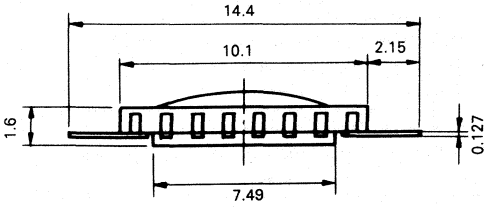
PACKAGE DIMENSIONS OF THE 22-PIN CERAMIC SHRINK DIP FOR ES (reference) (Unit: mm)

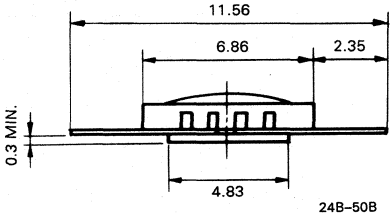


P22D-70-300B

PACKAGE DIMENSION FOR ENGINEERING SAMPLE 24 PIN CERAMIC SOP (for reference) (Unit: mm)







14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17108.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17108CS-xxx	22-pin plastic shrink DIP (300 mil)	• Wave soldering • Partial heating method
μPD17108GS-xxx	24-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below Number of flow process: 1
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution **Do not apply more than a single process at once, except for "Partial heating method."**

Remark For details of the recommended soldering conditions for surface mount type products, refer to our document "SMT MANUAL" (IEI-1207).

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	[redacted]	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of input/output port pins Note	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

Note A number in parentheses indicates the number of the N-ch opendrain outputs for each of which a pull-up resistor may or may not be provided depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17107L is a tiny microcontroller consisting of a ROM (512 × 16 bits), RAM (16 × 4 bits), and 11 input/output ports. The functions and pins of the μPD17107L are compatible with those of the μPD17107.

The μPD17107L can operate at the low voltage (1.5 V min.). It can be used for wide variety of products controlled by one lithium battery or two dry cells.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM) : 512 words × 16 bits
- Data memory (RAM) : 16 × 4 bits
- Input/output ports : 11 ports (including 3 N-ch open-drain outputs)
- Instruction execution time : 40 μs (with 200 kHz RC resonator used)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function : STOP and HALT modes
- Data memory can retain data on low voltage (1.5 V min.)
- An RC oscillator for the system clock:
  Capacitor built-in type (only resistor for external circuit)
- Operating supply voltage : 1.5 to 3.6 V (at 200 kHz)

APPLICATIONS

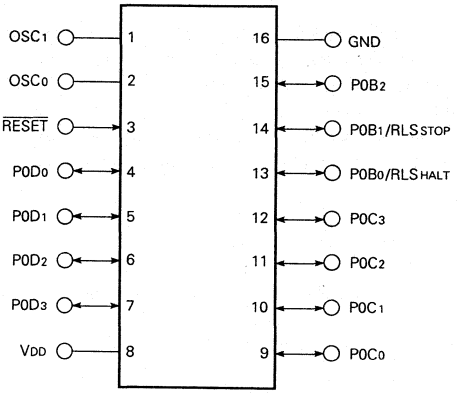
- Controlling electric appliances or toys

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17107LCX-xxx	16-pin plastic DIP (300 mil)	Standard
μPD17107LGS-xxx	16-pin plastic SOP (300 mil)	Standard

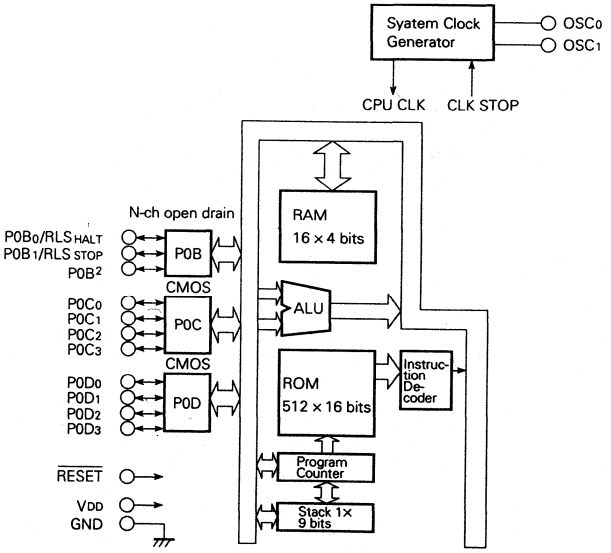
PIN CONFIGURATION (Top View)

μPD17107LCX, μPD17107LGS



16-pin plastic DIP
16-pin plastic SOP

BLOCK DIAGRAM of μPD17107L



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	I/O	Function	Reset
$P0B_0$/RLS$_{HALT}$	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS$_{STOP}$		For releasing the STOP mode	
$P0B_2$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0C_0$ - $P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$ - $P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

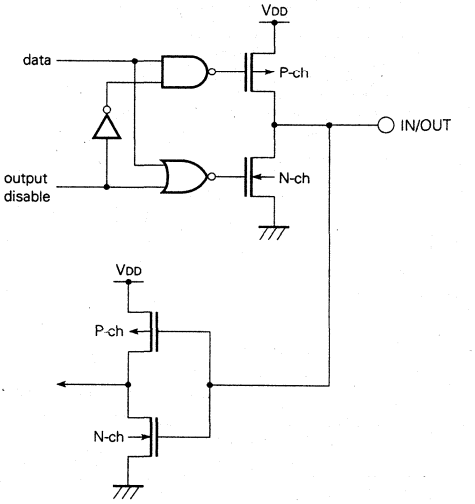
Pin name	I/O	Function
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).
V_{DD}		• Positive power supply pin
GND		• GND pin
OSC_0, OSC_1		• Pins to be connected to the system clock resonator

I/O: Input/output

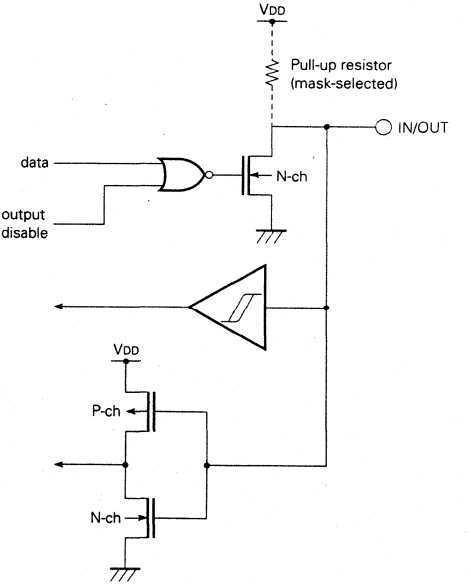
PIN EQUIVALENT CIRCUITS

Following are schematics of the equivalent circuits of the pins of the μPD17107L.

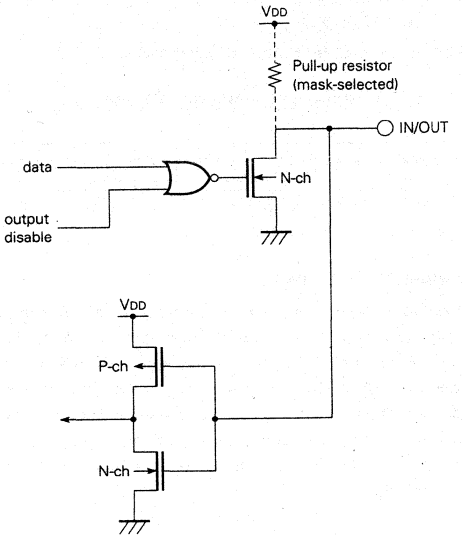
(1) P0C and P0D



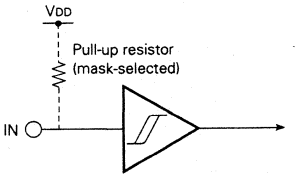
(2) P0B0 and P0B1



(3) P0B2



(4) $\overline{\text{RESET}}$

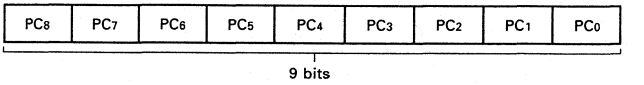


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

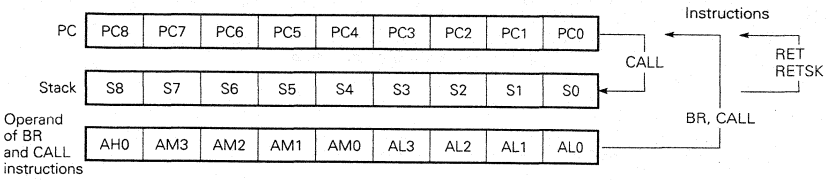
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17107L is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

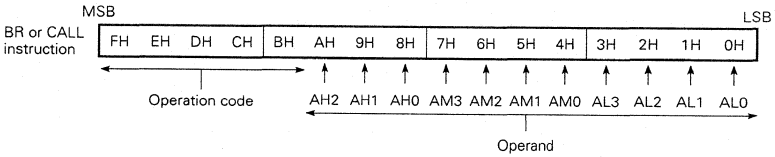
Fig. 2-1 shows the relationship between PC, stack, and operands of BR and CALL instructions.

Fig. 2-1 Relationship between PC, Stack, and Operands of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leq n \leq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leq n \leq 8$) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

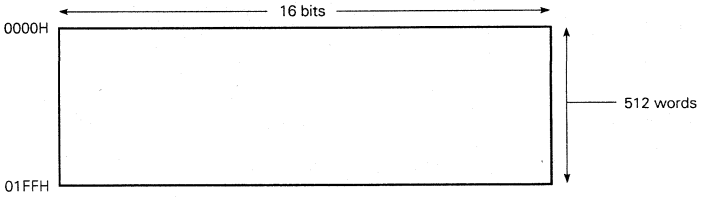
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory (ROM).

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory (RAM) stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

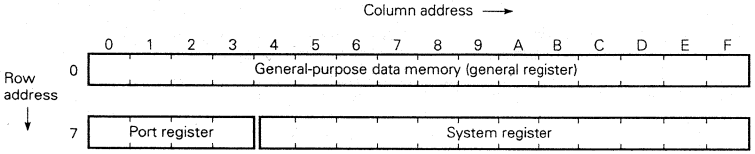
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation, comparison, evaluation, or transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17107L register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

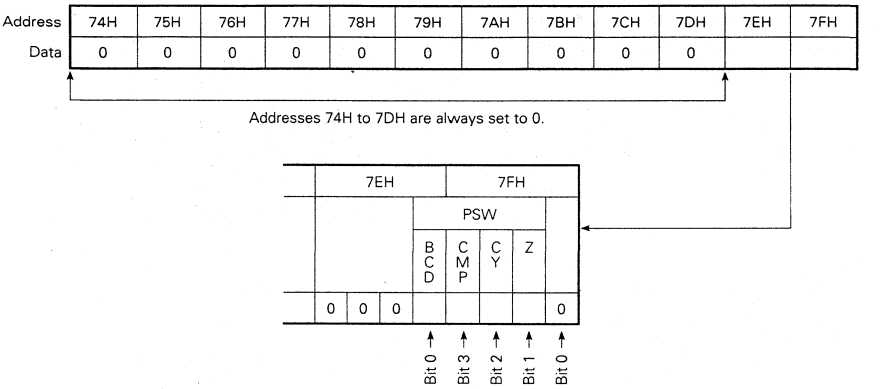
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17107L.

Fig. 4-2 System Register Map

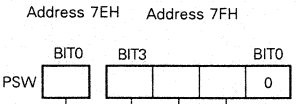


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7FH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction is 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Remark Z_{n-1}: The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0B (P0B0/RLSHALT, P0B1/RLSSTOP, P0B2)

Port 0B is a 3-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

The port register for port B consists of 4 bits but its highest bit is always set to 0. This means that if an attempt is made to write data to the highest bit of 71H, the data is invalidated and if an attempt is made to read it, 0 is always returned.

When the μPD17107L is in the HALT or STOP mode, P0B0 and P0B1 function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to **7. STANDBY FUNCTIONS**.)

6.2 PORT 0C (P0C0 to P0C3)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.3 PORT 0D (P0D0 to P0D3)

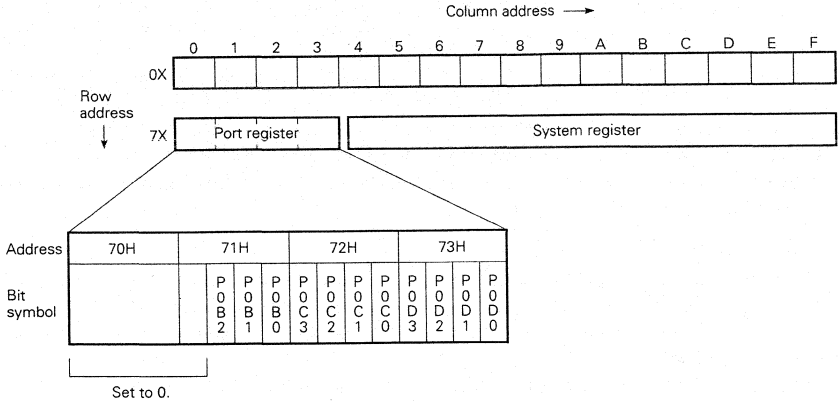
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.4 RECOMMENDED CONDITIONS FOR UNUSED μPD17107L PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output mode	Port	Recommended connection
Input mode	Ports B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports C and D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17107L provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{RESET}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{RESET}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting and releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{RESET}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{RESET}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the POB_0 pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

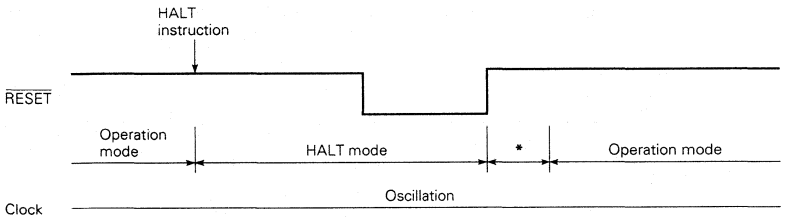
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← 4-bit data in the operand

X	Conditions for setting and releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instruction are executed starting at address 0H. The rising edge of the signal applied to the P0B1 pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the OSC1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

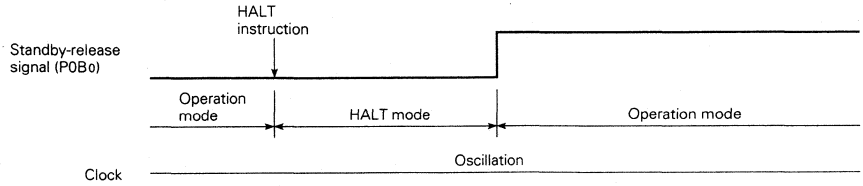
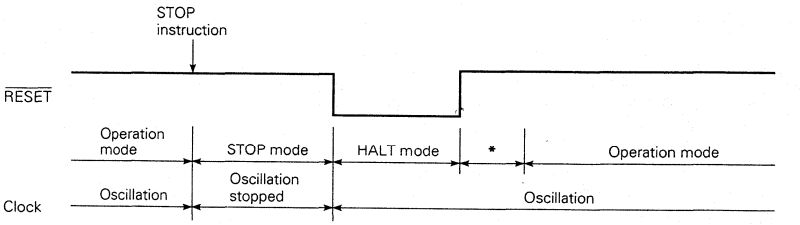


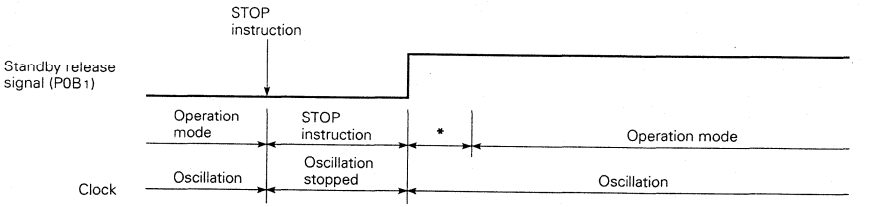
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bit 3 to bit 1 at 7FH	All 0s
Ports 0B to 0D	71H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17107L must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17107L.OPT file in AS17107L (device file for the μPD17107L) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instructions listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_2$ to $P0B_0$	OPTP0B	3	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0B	($P0B_2$), ($P0B_1$), ($P0B_0$)	[;comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	($\overline{\text{RESET}}$)	[;comment]

Example To set the following mask option in a μPD17107L source file to be assembled:

P0B2 : Pull-up P0B1 : Open
P0B0 : Open $\overline{\text{RESET}}$: Pull-up

```
                    ⋮
;17107L
 Setting mask options:  OPTION
                        OPTP0B  P0BPLUP, OPEN, OPEN
                        OPTRES  RESPLUP
                        ENDOP
                    ⋮
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17107L device file (AS17107L).

Table 9-2 Reserved Symbols

Name	Attribute	Value	Read/write	Description
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3*	FLG	0.71H.3	Read	Set to 0.
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

* Although P0B3 does not exist in the μPD17107L, it is defined as a read-only flag so that it is treated as a dummy bit when a built-in macro is used.

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14} - b_{11} (BIN)	HEX	b_{15} = 0		b_{15} = 1	
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M	: One of data memory	STACK	: Stack specified by (SP)
m	: Data memory address specified by [m_H, m_L] of each bank	i	: Immediate data; 4 bits
		n	: Bit position; 4 bits
m_H	: Data memory address high (row address); 3 bits	addr	: One of program memory address; 11 bits
		a_H	: Program memory address high; 3 bits
m_L	: Data memory address low (column address); 4 bits	a_M	: Program memory address middle; 4 bits
		a_L	: Program memory address low; 4 bits
R	: One of general register specified by [(RP), r]	CY	: Carry flag
		CMP	: Compare flag
r	: General register address low (column address); 4 bits	s	: Stop release condition
		h	: Halt release condition
RP	: General register pointer	[ ]	: Address of M, R
PC	: Program counter	( )	: Contents of M, R
SP	: Stack pointer		

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r, m	Add memory to register	R ← (R) + (M)	00000	m_H	m_L	r
		m, #i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	Add memory to resister with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r ,m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	M – i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	M – i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	M – i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	M – i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r, m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r, m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r, m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Transfer	LD	r, m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m, r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) – 1, STACK ← ((PC)+1), PC ←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP)+1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP)+1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No Operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0C, P0D, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		−0.3 to V_{DD} + 0.3	V
		P0B	**Note 1**	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0B, P0C, or P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0B, P0C, or P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	16-pin plastic DIP	400	mW
			16-pin plastic SOP	190	

Note 1. When a built-in pull-up resistor is mask-selected

2. When a built-in pull-up resistor is not mask-selected

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
Input/output capacitance	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.5 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note 1**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note 2**
Low-Level Input Voltage	V_{IL1}	0		0.25 V_{DD}	V	R0C, P0D	
	V_{IL2}	0		0.15 V_{DD}	V	$\overline{\text{RESET}}$	
	V_{IL3}	0		0.15 V_{DD}	V	P0B	
High-Lovel Output Voltage	V_{OH}	V_{DD} − 1.0			V	P0C, P0D, I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL}			0.5	V	P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 1**
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V **Note 2**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 1**
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V **Note 2**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0B, P0C, P0D, V_{OUT} = 0 V	
Pull-Up Resistor Provided for $\overline{\text{RESET}}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note 3**	I_{DD1}		65	150	μA	Operation mode	V_{DD} = 3 V ±10 %, f_{CC} = 200 kHz ±20 %
	I_{DD2}		55	130	μA	HALT mode	V_{DD} = 3 V ±10 %, f_{CC} = 200 kHz ±20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 3 V ±10 %

Note 1. When a built-in pull-up resistor is mask-selected

2. When a built-in pull-up resistor is not mask-selected

3. This current excludes the current which flows through the built-in pull-up resistors.

DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS ON LOW SUPPLY VOLTAGE
(T_a = −40 to +85 °C)

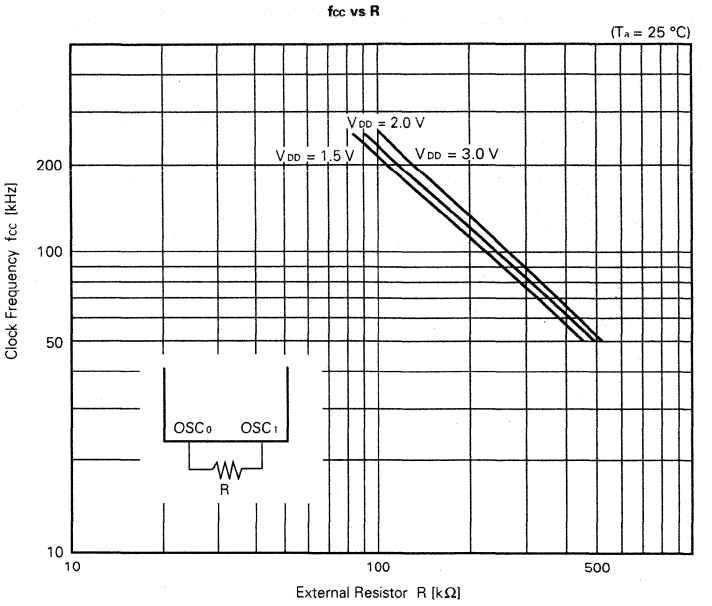
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Retention Supply Voltage	V_{DDDR}	1.5		3.6	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 1.5 V
Release Signal Set Time	t_{SREL}	0			μs	

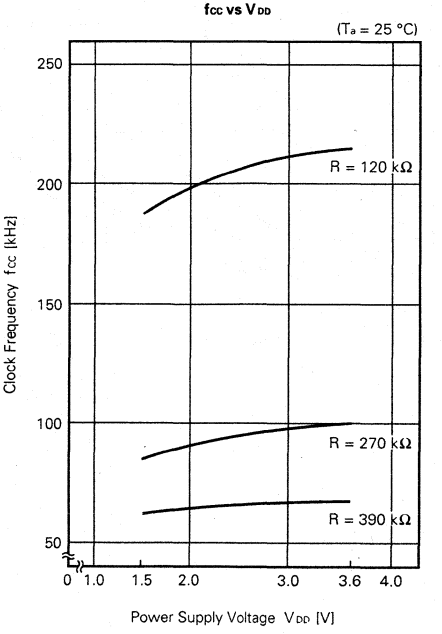
AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.5 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	t_{CY}	32		160	μs	
High/low Level Width on P0B0 and P0B1	t_{PBH} t_{PBL}	100			μs	
High/Low Level Width on $\overline{\text{RESET}}$	t_{RSH} t_{RSL}	100			μs	

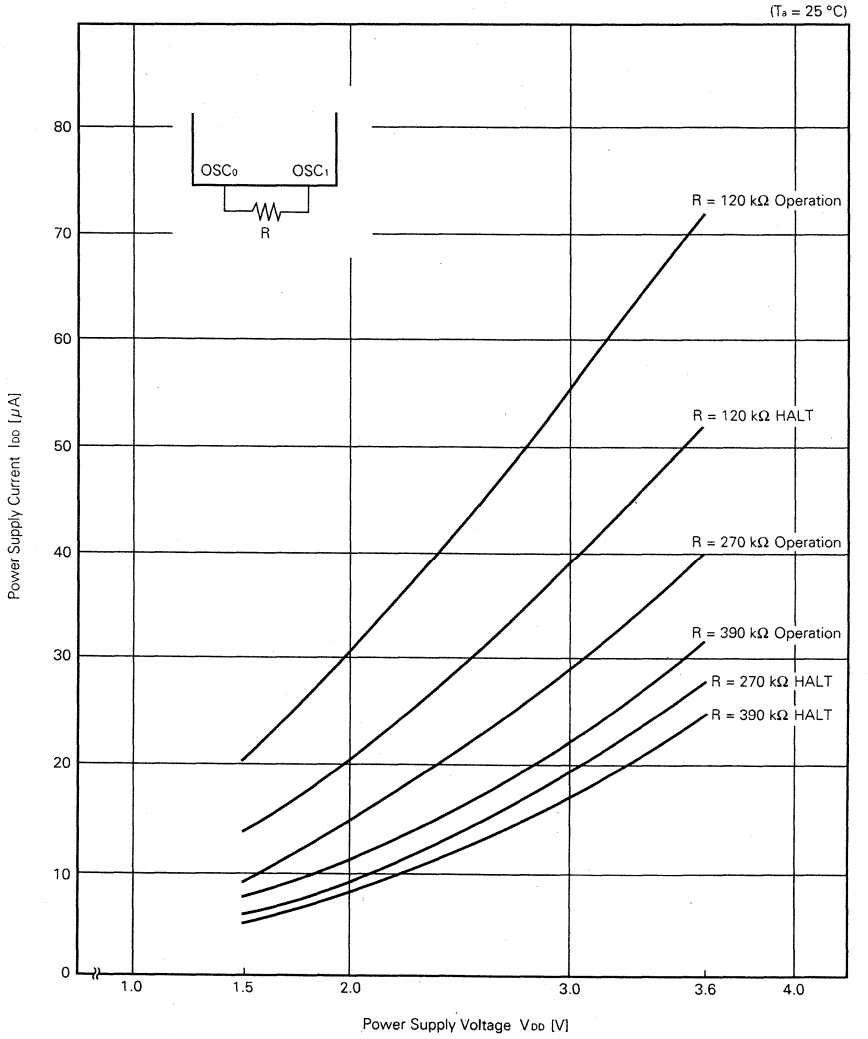
Remark $t_{CY} = 8/f_{CC}$ (f_{CC}: system clock oscillation frequency)

12. CHARACTERISTICS CURVE

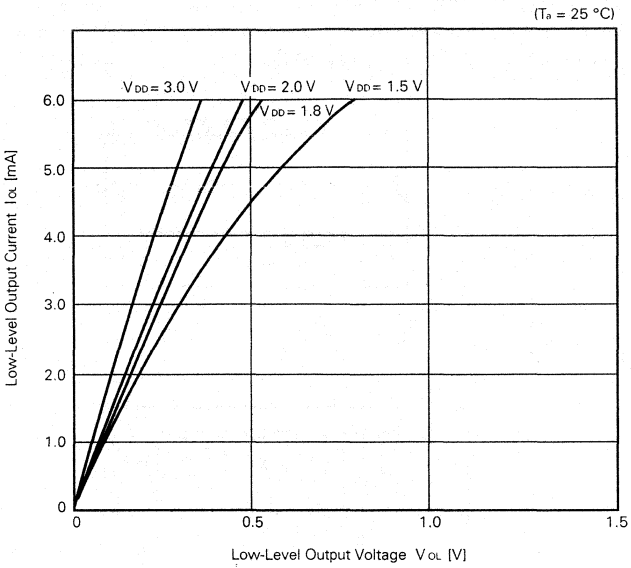




I_{DD} vs V_{DD}

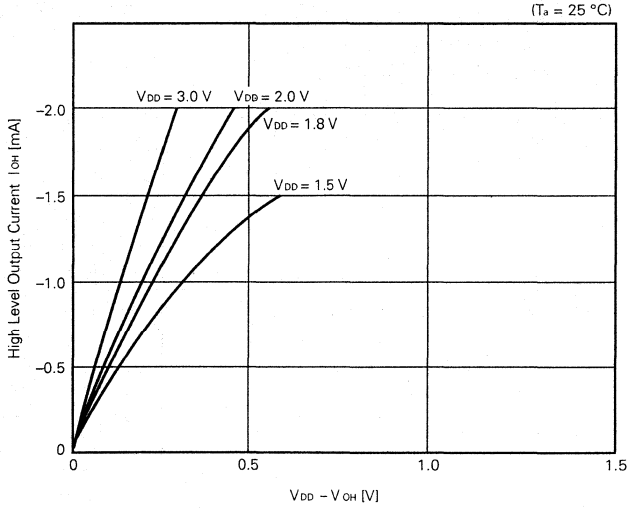

(Ta = 25 °C)
OSC0
OSC1
R
R = 120 kΩ Operation
R = 120 kΩ HALT
R = 270 kΩ Operation
R = 390 kΩ Operation
R = 270 kΩ HALT
R = 390 kΩ HALT
Power Supply Current IDD [μA]
0
10
20
30
40
50
60
70
80
1.0
1.5
2.0
3.0
3.6
4.0
Power Supply Voltage VDD [V]

I_{OL} vs V_{OL}



Caution The absolute maximum rated current is 30 mA per pin.

I_{OH} vs (V_{DD} – V_{OH})

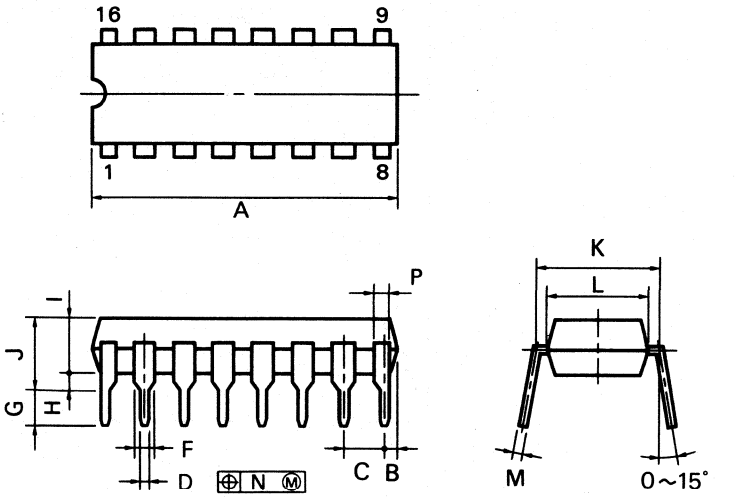


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values.

13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

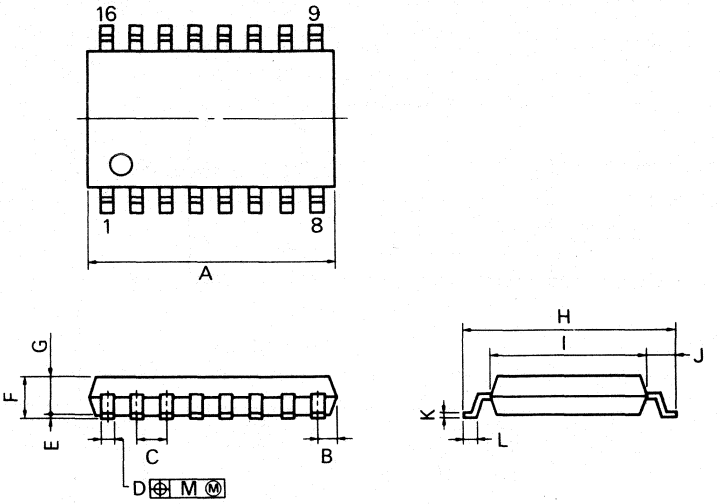
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



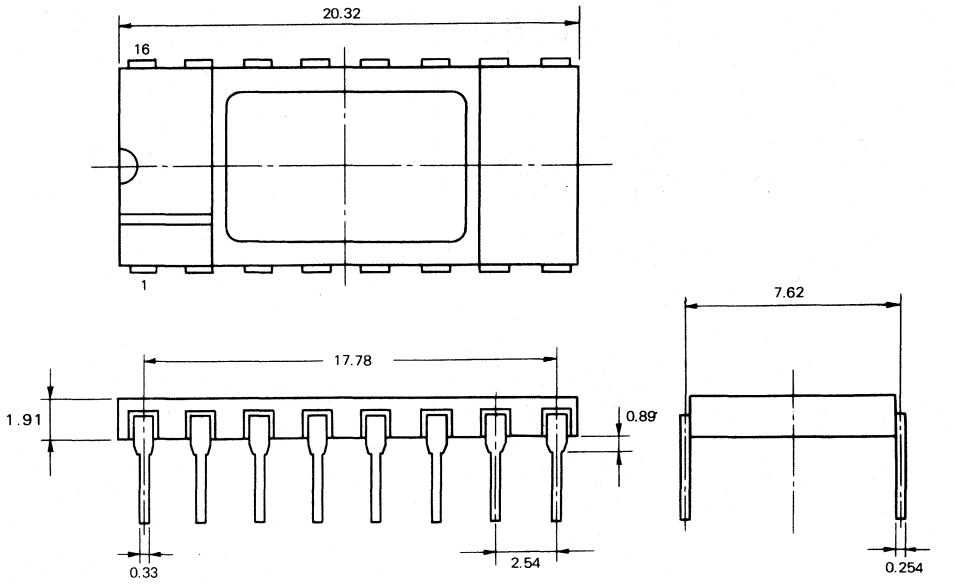
P16GM-50-300B-1

NOTE

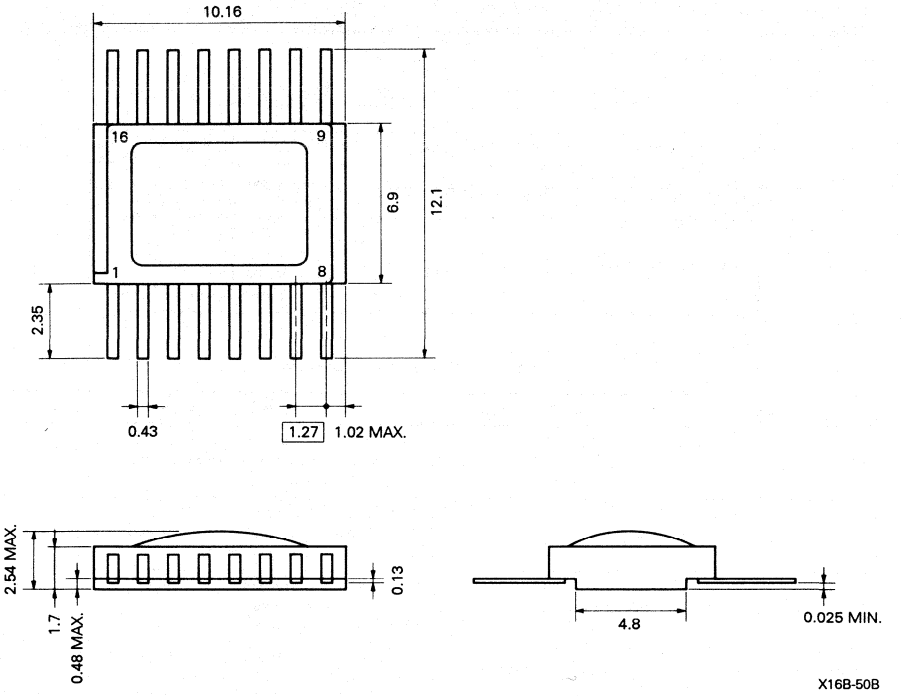
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

Package dimensions of the 16-pin ceramic DIP for ES (reference) (Unit: mm)



Package dimensions of the 16-pin ceramic SOP for ES (reference) (Unit: mm)



X16B-50B

14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17107L.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17107LCX-xxx	16-pin plastic DIP (300 mil)	• Wave soldering • Partial heating method
μPD17107LGS-xxx	16-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heatingl method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions for surface mount type products, refer to our document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17104L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 × 16 bits							
RAM size	16 × 4 bits							
Number of input/ output port pins*	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the number of input/output port pins selectable between N-ch open-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17108L is a tiny microcontroller consisting of a ROM (512 × 16 bits), RAM (16 × 4 bits), and 16 input/output ports.

The μPD17108L can operate at the low voltage (1.5 V min.). It can be used for wide variety of products controlled by one lithium battery or two dry cells.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Program memory (ROM): 512 words × 16 bits
- Data memory (RAM): 16 × 4 bits
- Input/output ports: 16 ports (including 4 N-ch open-drain outputs)
- Instruction execution time: 40 μs (at 200 kHz)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function: STOP and HALT modes
- Data memory can retain data on low voltage (1.5 V min.).
- An RC oscillator for the system clock: Capacitor built-in type (only resistor for external circuit)
- Operating supply voltage: 1.5 to 3.6 V (at 200 kHz)

APPLICATIONS

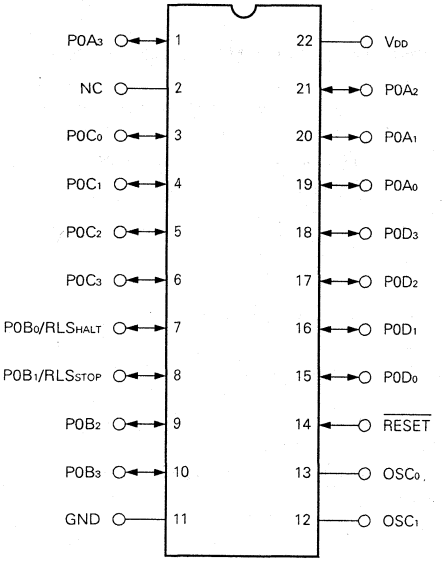
- Controlling electric appliances or toys

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17108LCS-xxx	22-pin plastic shrink DIP (300 mil)	Standard
μPD17108LGS-xxx	24-pin plastic SOP (300 mil)	Standard

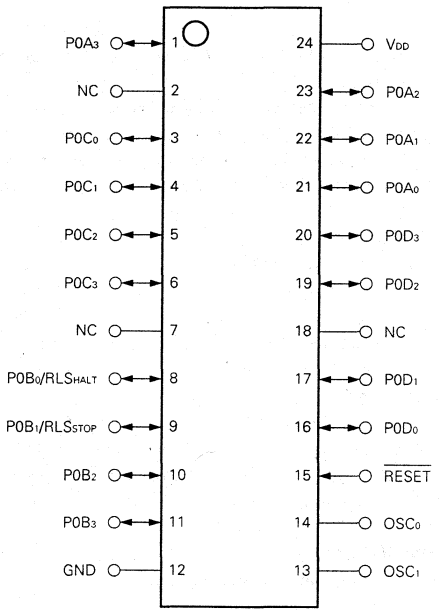
PIN CONFIGURATION (Top View)

μPD17108LCS



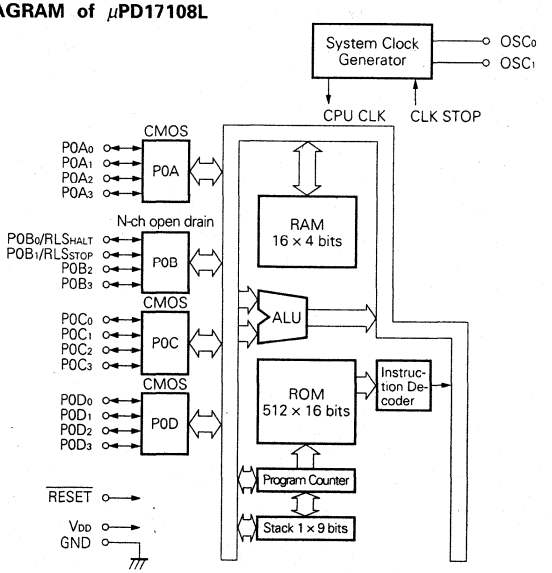
22-pin plastic shrink DIP

μPD17108LGS



24-pin plastic SOP

BLOCK DIAGRAM of μPD17108L



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	I/O	Function	Reset
$P0A_0$-$P0A_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0A)	High impedance (input mode)
$P0B_0$/RLS_{HALT}	I/O	For releasing the HALT mode	• Open-drain: High impedance (input mode) • With pull-up resistor provided: High level (input mode)
$P0B_1$/RLS_{STOP}		For releasing the STOP mode	
$P0B_2$, $P0B_3$		• N-ch open-drain 4-bit I/O port (port 0B) • A pull-up resistor can be provided bit by bit (mask-selected). • 9 V in open-drain mode	
$P0C_0$-$P0C_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0C)	High impedance (input mode)
$P0D_0$-$P0D_3$	I/O	CMOS (push-pull) 4-bit I/O port (port 0D)	High impedance (input mode)

- Non-port pins

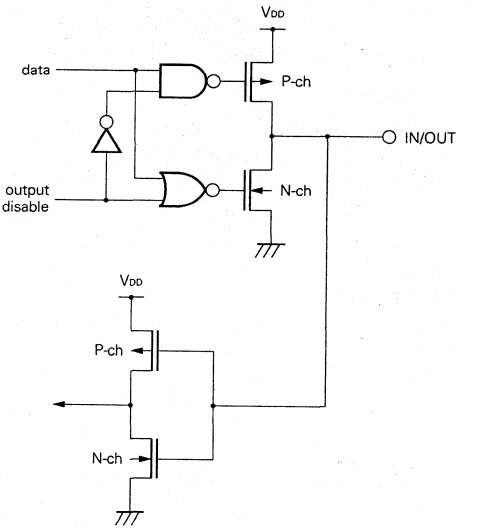
Pin name	I/O	Function
$\overline{RESET}$	Input	• System reset input pin • A built-in pull-up resistor can be provided bit by bit (mask-selected).
V_{DD}		• Positive power supply pin
G_{ND}		• GND pin
OSC_0, OSC_1		• Pins to be connected to the system clock resonator

I/O: Input/output

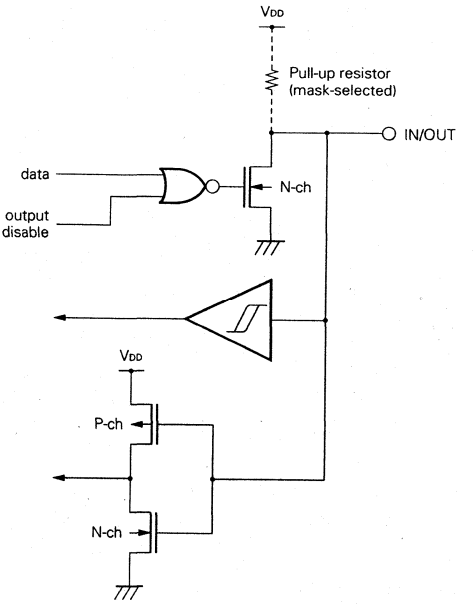
PIN EQUIVALENT CIRCUITS

Following are schematics of the equivalent circuits of the pins of the μPD17108L.

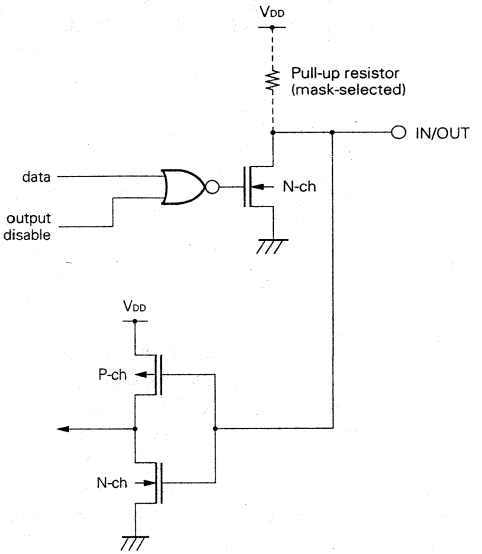
(1) P0A, P0C, and P0D



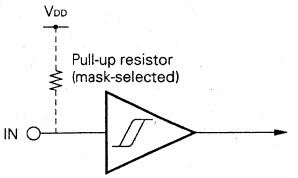
(2) P0B0 and P0B1



(3) $P0B_2$ and $P0B_3$



(4) $\overline{\text{RESET}}$

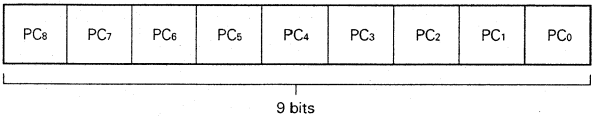


1. PROGRAM COUNTER (PC)

1.1 FORMAT OF THE PROGRAM COUNTER (PC)

The program counter is a 9-bit binary counter formatted as shown in Fig. 1-1.

Fig. 1-1 Format of the Program Counter



1.2 FUNCTIONS OF THE PROGRAM COUNTER (PC)

The program counter specifies the address of a program memory (ROM) or a program.

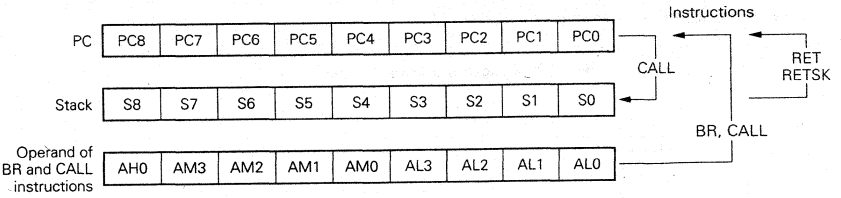
Usually, every time an instruction is executed, the program counter is incremented by one. When a branch instruction (BR), a subroutine call instruction (CALL), or a return instruction (RET) is executed, the address specified in the operand is loaded in the PC. Then the instruction in the address is executed. When a skip instruction is executed, the address of the instruction next to the skip instruction is specified irrespective of the contents of the skip instruction. If the skip conditions are satisfied, the instruction next to the skip instruction is regarded as a No Operation (NOP) instruction. So, the NOP instruction is executed and the address of the next instruction is specified.

2. STACK

Stack of the μPD17108L is a register in which the return address of a program is saved when a subroutine call instruction is executed. One level of address stack is provided.

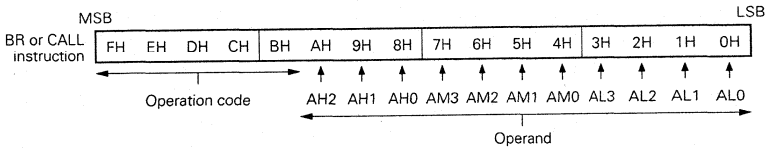
Fig. 2-1 shows the relationship between PC, stack, and operands of BR and CALL instructions.

Fig. 2-1 Relationship between PC, Stack, and Operands of BR and CALL Instructions



In Fig. 2-1, AHn, AMn, and ALn ($0 \leqq n \leqq 3$) indicate bit positions in a 16-bit instruction as follows:

Fig. 2-2 Format of a 16-bit Instruction



When the assembler (AS17K) is not used and a BR or CALL instruction is used, AH2 and AH1 must be set to 0.

Sn ($0 \leqq n \leqq 8$) denotes a stack.

$\overline{\text{RESET}}$ signal input clears all bits of the program counter to 0.

3. PROGRAM MEMORY (ROM)

Fig. 3-1 shows the configuration of program memory (ROM).

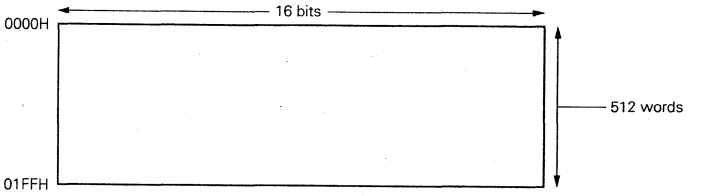
The program memory consists of 512 words by 16 bits.

The program memory is addressed in units of 16 bits and it ranges from addresses 0000H to 01FFH. Each address is specified by the program counter (PC).

Since an instruction consists of 16 bits (one word), the instruction is stored at one address of the program memory (ROM).

Address 0000H is assigned to a reset start address.

Fig. 3-1 Program Memory Map



4. DATA MEMORY (RAM)

The data memory (RAM) stores data of arithmetic/logic and control operations. Data can be always written to or read from it by means of instructions.

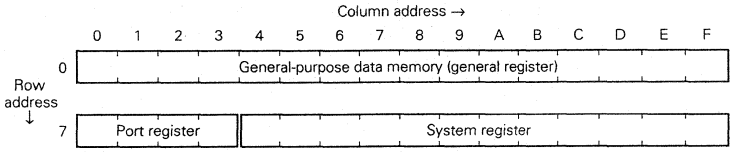
4.1 FORMAT OF THE DATA MEMORY (RAM)

Fig. 4-1 shows the format of the data memory (RAM).

The data memory is configured in units of 4 bits, or "one nibble," and an address is assigned to each 4 bits of data. The 3 high-order bits are called the "row address," and the 4 low-order bits are called the "column address."

According to its functions, the data memory is divided into three blocks as shown below: general-purpose data memory, port register, and system register.

Fig. 4-1 Data Memory Map



4.1.1 Functions of the General-Purpose Data Memory

The general-purpose data memory is a part of the data memory from which the system register (SYSREG) and port register are excluded. By executing a data memory manipulation instruction, a 4-bit arithmetic operation, comparison, evaluation, or transfer between data on data memory and any immediate data can be executed with a single operation.

4.1.2 Functions of the General Register

The general register indicates any identical row address (16 nibbles) in the data memory specified in the register pointer (RP) in the system register. Since the μPD17108L register pointer is always set to 0, the general-purpose data memory is also used as a general register. The general register can operate or transfer data to and from the data memory.

4.1.3 Functions of the Port Register

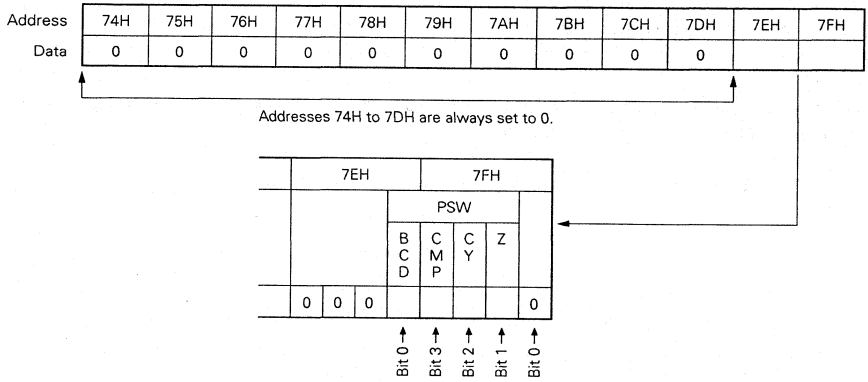
The port register is used to set output data or to read the input data of input/output ports.

Once data is written to the port register corresponding to a port, the port is set as an output port and continues to output the value unless the value is rewritten. Whenever a read instruction is executed for a port register, the read data indicates the states of the pins, not the value of the port register, regardless of whether the pins are in the input or output mode.

4.1.4 Functions of the System Register

The system register controls the CPU. The program status word (PSW) is the only system register existing in the μPD17108L.

Fig. 4-2 System Register Map

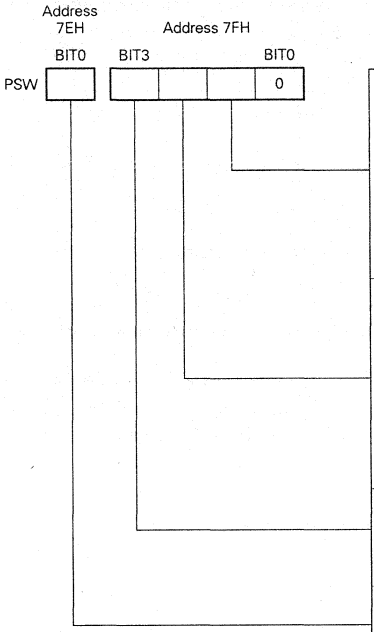


Bit 0 at address 7EH and the high-order 3 bits at address 7FH are assigned to the program status word.

The BCD flag is mapped in bit 0 at address 7EH, the CMP flag is mapped in bit 3 at address 7FH, the carry (CY) flag is mapped in bit 2 at address 7FH, and the zero (Z) flag is mapped in bit 1 at address 7FH.

The high-order 3 bits at address 7EH and bit 0 at address 7FH are always set to 0.

Fig. 4-3 Format of the Program Status Word



Zero flag (Z)	Set to 0 when: • An arithmetic operation generates a result of zero if CMP = 0. • An arithmetic operation generates a result of zero and Z = 1 if CMP = 1. When the Z flag is already 0, it remains unchanged. Reset to 1 when: • An arithmetic operation generates a result other than zero.
Carry flag (CY)	Set to 0 when: • An addition produces a carry or a subtraction produces a borrow. • The LSB of the operand in the RORC instruction is 1. Reset to 1 when: • Neither a carry nor borrow is produced. • The LSB of the operand in the RORC instruction 0.
Compare flag (CMP)	If this flag is set, the result of an arithmetic operation is not stored in memory or general registers. The flag is automatically reset by executing the SKT or SKF instruction.
BCD flag (BCD)	If this flag is set, arithmetic operations are performed in decimal, and if this flag is reset, arithmetic operations are performed in binary.

Comparison instructions (SKE, SKNE, SKGE, or SKLT) do not change the state of the CY flag, but an arithmetic operation may affect the CY flag according to the result even if the CMP flag is set.

Each bit of the program status word is initialized to 0 when a reset signal is applied.

The Z flag in the program status word changes according to the set value of the CMP flag as listed in Table 4-1.

Table 4-1 Change in Z Flag

Condition	Z flag value	
	CMP = 0	CMP = 1
Reset	0	—
Memory manipulation sets the Z flag to 0.	0	0
Memory manipulation sets the Z flag to 1.	1	1
Arithmetic operation results in a non-zero value.	0	0
Arithmetic operation results in 0.	1	Z_{n-1}

Remark Z_{n-1} : The Z flag value present immediately before arithmetic operation

While CMP is 1, if an arithmetic operation results in 0H when the value of the Z flag is 1, the Z flag does not change. If an arithmetic operation results in other than 0H, the Z flag is reset to 0 and remains intact even when a second arithmetic operation results in 0H.

After the CMP and Z flags are set to 1, subtraction and comparison are performed several times. Then, if the Z flag still indicates 1, all of the comparison operations showed a match, resulting in 0. If the Z flag is 0 after the comparison operations, a mismatch occurred in at least one comparison operation.

5. ARITHMETIC AND LOGIC UNIT (ALU)

The arithmetic and logic unit (ALU) performs arithmetic operations, logical operations, bit tests, comparisons, and rotations on 4-bit data.

5.1 ARITHMETIC OPERATIONS

Arithmetic operations are performed on binary or decimal data. If the BCD flag in the program status word is 1, the ALU operates on decimal data, and if the flag is 0, it operates on binary data.

If an addition produces a carry or if a subtraction produces a borrow, the carry (CY) flag is set to 1. If neither a carry nor borrow is produced, the flag is reset to 0.

If an arithmetic operation results in zero, the zero (Z) flag is set to 1. Otherwise, the flag is reset to 0.

(1) Binary operation

If the result of a binary arithmetic operation is greater than 15 (1111B), a carry is produced. If it is less than zero, a borrow is produced. In either case, the CY flag is set to 1.

(2) Decimal operation

If the result of a decimal arithmetic operation is greater than 9 (1001B), a carry is produced. If it is less than 0, a borrow is produced. In either case, the CY flag is set to 1.

Decimal operations are allowed if one of the following results is generated. If the result of a decimal operation does not fall into these ranges, the CY flag is set to 1, and a result greater than or equal to 10 (1010B) is produced.

1. Addition must generate a result from 0 to 19.
2. Subtraction must generate a result from 0 to 9 or −10 to −1.

5.2 LOGICAL OPERATIONS

Logical operations include ANDing, ORing, and XORing.

5.3 OTHER OPERATIONS

The ALU enables bit testing, comparison, and data rotation.

6. PORTS

6.1 PORT 0A ($P0A_0$ to $P0A_3$)

Port 0A is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 70H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0A are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.2 PORT 0B ($P0B_0/RLS_{HALT}$, $P0B_1/RLS_{STOP}$, $P0B_2$, $P0B_3$)

Port 0B is a 4-bit input/output port. Only N-ch open-drain outputs appear on the pins of port 0B. The N-ch open-drain output mode allows application of 9 V, so it can be used for interfacing with a circuit operating on a different power supply voltage.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 71H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of port P0B are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

When the μPD17108L is in the HALT or STOP mode, P0B0 and P0B1 function as pseudo interrupt pins to release the HALT and STOP modes. (Refer to **7. STANDBY FUNCTIONS**)

6.3 PORT 0C ($P0C_0$ to $P0C_3$)

Port 0C is a 4-bit input/output port. CMOS (push-pull) outputs appear on those pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 72H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port P0C are placed in the output mode to continue to output written data. The data is retained unless new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

6.4 PORT 0D (P0D0 to P0D3)

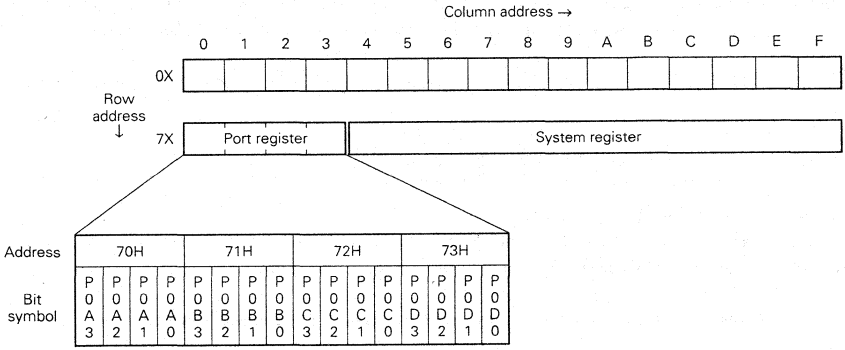
Port 0D is a 4-bit input/output port. CMOS (push-pull) outputs appear on these pins.

Input and output are set in units of nibbles. The input mode is set at reset, and the output mode is set by writing data to the port register in address 73H of the data memory. The output mode is maintained until the system is reset.

Output to the port is executed via the port register. Once data is written to the port register, all pins of the port 0D are placed in the output mode to continue to output written data. The data is retained until new data is written to the register.

Whenever the port register is read, the read data indicates the states of the pins, not the contents of the port register, regardless of whether the pins are in the input or output mode. In this case, the contents of the port register remain unchanged.

Fig. 6-1 Port Register Map



6.5 RECOMMENDED CONDITIONS FOR UNUSED μPD17108L PINS

To prevent malfunction, process unused input/output pins as shown below.

Table 6-1 Recommended Conditions for Unused Pins

Input/output	Port	Recommended connection
Input mode	Ports A, B, C, and D	Connect to V_{DD} or GND.
Output mode	CMOS ports (ports A, C, and D)	Open
	N-ch open-drain port (port B)	

7. STANDBY FUNCTIONS

The μPD17108L provides two standby modes, the HALT mode and the STOP mode.

7.1 HALT MODE

The HALT mode stops the program counter (PC) while allowing the system clock to continue operating. The HALT mode can be entered with the HALT instruction, and can be released by a reset signal ($\overline{\text{RESET}}$) or input to the $P0B_0$ pin. When the HALT mode is released by input to the $P0B_0$ pin, the next instruction after the HALT instruction is executed without waiting for stable oscillation of the system clock.

When the HALT mode is released forcibly by the reset signal ($\overline{\text{RESET}}$), normal system reset occurs, and execution starts at address 0H.

7.2 STOP MODE

The STOP mode stops oscillation of the system clock so that data can be retained at low voltage. The STOP mode can be entered with the STOP instruction, and can be released by a reset signal ($\overline{\text{RESET}}$) or input to the $P0B_1$ pin. When the mode is released by input to the $P0B_1$ pin, execution starts with the next instruction after the STOP instruction.

When the STOP mode is released forcibly by the reset signal ($\overline{\text{RESET}}$), normal system reset occurs, and execution starts at address 0H.

7.3 SETTING AND RELEASING THE STANDBY MODES

(1) Setting and releasing the HALT mode

The conditions for releasing the HALT mode can be selected with the least significant bit of the operand in the HALT instruction. The high-order 3 bits of the operand must be set to 0.

Table 7-1 Setting and Releasing Conditions Specified in the HALT Instruction

HALT 000XB ← 4-bit data in the operand

X	Conditions for setting and releasing the HALT mode
0	Executing the HALT instruction enters the HALT mode unconditionally. The mode can be released only by the reset signal ($\overline{\text{RESET}}$). After the mode is released, instructions are executed starting at address 0H.
1	If P0B0 is 0, executing the HALT instruction enters the HALT mode. If P0B0 is 1, executing the HALT instruction does not enter the HALT mode. Application of the reset signal ($\overline{\text{RESET}}$) releases the HALT mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of an input signal on the $P0B_0$ pin also releases the HALT mode. In this case, execution starts with the next instruction after the HALT instruction.

(2) Setting and releasing the STOP mode

Conditions to release the STOP mode can be selected with the least significant bit of the operand in the STOP instruction. The high-order 3 bits of the operand must be set to 0.

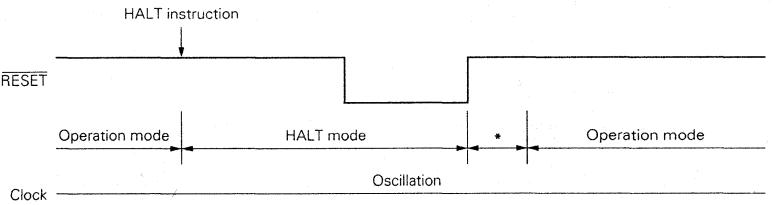
Table 7-2 Setting and Releasing Conditions Specified in the STOP Instruction

STOP 000XB ← bit data in the operand

X	Conditions for setting and releasing the STOP mode
0	Executing the STOP instruction enters the STOP mode unconditionally. All peripheral circuits are placed in the same initial state as when the system is reset, then they stop operating. Only the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H.
1	If P0B1 is 0, executing the STOP instruction enters the STOP mode. If P0B1 is 1, executing the STOP instruction does not enter the STOP mode. Application of the reset signal ($\overline{\text{RESET}}$) can release the STOP mode. After the mode is released, instructions are executed starting at address 0H. The rising edge of the signal applied to the P0B1 pin can also release the mode. In this case, execution starts with the next instruction after the STOP instruction.

7.4 TIMING FOR RELEASING THE STANDBY MODES

Fig. 7-1 Releasing the HALT Mode by $\overline{\text{RESET}}$ Input



When the $\overline{\text{RESET}}$ signal is applied to release the HALT mode, the $\overline{\text{RESET}}$ input makes a transition from low to high, then an operation mode is entered.

* The HALT mode remains effective in this period, waiting for the operation mode.
At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-2 Releasing the HALT Mode by Interrupt

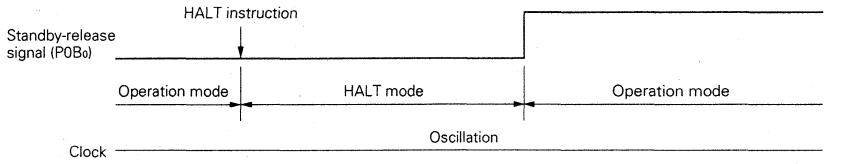
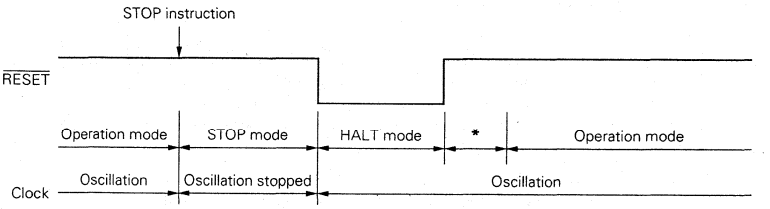


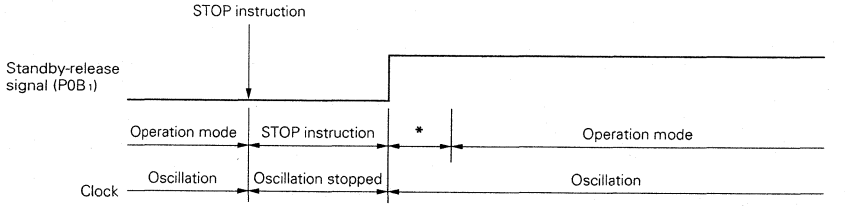
Fig. 7-3 Releasing the STOP Mode by $\overline{\text{RESET}}$ Input



As soon as the $\overline{\text{RESET}}$ input makes a transition from high to low in the STOP mode, the system clock starts generating clock pulses.

* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

Fig. 7-4 Releasing the STOP Mode by Interrupt



* The HALT mode remains effective in this period, waiting for the generation of clock pulses to stabilize. At least eight clock pulses on the OSC_1 pin cause operation to start.

8. RESET FUNCTION

8.1 HARDWARE STATE AT RESET

A low-active reset signal applied to the $\overline{\text{RESET}}$ pin sets the hardware states as listed below. A transition from low to high on the $\overline{\text{RESET}}$ pin releases the reset state.

Table 8-1 Hardware after Reset

Name	Location in memory space	Set value
Program counter		0000H
RAM	0H to 0FH	Data present before reset is retained.
Program status word (PSW)	Bit 0 at 7EH Bit 3 to bit 1 at 7FH	All 0s
Ports 0A to 0D	70H to 73H	Data present before reset is retained. All pins are placed in the input mode.

9. ASSEMBLER RESERVED WORDS

9.1 MASK OPTION PSEUDO INSTRUCTIONS

Source programs in the assembly language for the μPD17108L must include mask option pseudo instructions to select pin options.

To do this, be sure to catalog the D17108L.OPT file in AS17108L (device file for the μPD17108L) into the current directory beforehand.

Options must be mask-selected for the following pins:

- $P0B_0$
- $P0B_1$
- $P0B_2$
- $P0B_3$
- $\overline{RESET}$

9.1.1 OPTION and ENDOP Pseudo Instructions

The part starting with the OPTION pseudo instruction and ending with the ENDOP pseudo instruction is referred to as a mask option definition block. The coding format of the mask option definition block is shown on the next page.

Within this block, the mask option definition pseudo instructions listed in Table 9-1 can be coded.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTION		[; comment]
	⋮		
	ENDOP		

9.1.2 Mask Option Definition Pseudo Instructions

Table 9-1 lists the mask option definition pseudo instructions corresponding to each pin.

Table 9-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Operand name
$P0B_3$ to $P0B_0$	OPTP0B	4	P0BPLUP (with pull-up resistor) OPEN (without pull-up resistor)
$\overline{RESET}$	OPTRES	1	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)

The coding format of OPTP0B is shown below. The operands $P0B_3$, $P0B_2$, $P0B_1$, and $P0B_0$ are defined in this order.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTP0B	($P0B_3$), ($P0B_2$), ($P0B_1$), $P0B_0$)	[; comment]

The coding format of OPTRES is shown below.

Format

Symbol	Mnemonic	Operand	Comment
[label :]	OPTRES	(RESET)	[; comment]

Example To set the the following mask options in a μPD17108L source file to be assembled:

P0B3: Pull-up
P0B2: Pull-up
P0B0: Open
P0B1: Open
RESET: Pull-up

```
                    ⋮
; 17108L
  Setting mask options :  OPTION
                          OPTP0B      P0BPLUP, P0BPLUP, OPEN, OPEN
                          OPTRES      RESPLUP
                          ENDOP
                    ⋮
```

9.2 RESERVED SYMBOLS

Table 9-2 lists the reserved symbols defined in the μPD17108L device file (AS17108L).

Table 9-2 Reserved symbols

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

10. INSTRUCTION SET

10.1 INSTRUCTION SET LIST

b_{14} - b_{11} \ b_{15}		0		1	
BIN	HEX				
0 0 0 0	0	ADD	r,m	ADD	m, #i
0 0 0 1	1	SUB	r,m	SUB	m, #i
0 0 1 0	2	ADDC	r,m	ADDC	m, #i
0 0 1 1	3	SUBC	r,m	SUBC	m, #i
0 1 0 0	4	AND	r,m	AND	m, #i
0 1 0 1	5	XOR	r,m	XOR	m, #i
0 1 1 0	6	OR	r,m	OR	m, #i
0 1 1 1	7	RET RETSK RORC STOP HALT NOP	 r s h 		
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

10.2 INSTRUCTIONS

Legend

M		: One of data memory	n		: Bit position; 4 bits
	m	: Data memory address specified by [m_H, m_L] of each bank	addr		: One of program memory address; 11 bits
				a_H	: Program memory address high; 3 bits
	m_H	: Data memory address high (row address); 3 bits		a_M	: Program memory address middle; 4 bits
	m_L	: Data memory address low (column address); 4 bits		a_L	: Program memory address low; 4 bits
R		: One of general register specified by [(RP), r]	CY		: Carry flag
r		: General register address low (column address); 4 bits	CMP		: Compare flag
			s		: Stop release condition
	RP	: General register pointer	h		: Halt release condition
PC		: Program counter	[ ]		: Address of M, R
SP		: Stack pointer	( )		: Contents of M, R
STACK		: Stack specified by (SP)			
i		: Immediate data; 4 bits			

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r,m	Add memory to register	R ← (R) + (M)	00000	m_H	m_L	r
		m,#i	Add immediate data to memory	M ← (M) + i	10000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	R ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m,#i	Add immediate data to memory with carry	R ← (M) + i + (CY)	10010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	R ← (R) – (M)	00001	m_H	m_L	r
		m,#i	Subtract immediate data from memory	M ← (M) – i	10001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	R ← (R) – (M) – (CY)	00011	m_H	m_L	r
		m,#i	Subtract immediate data from memory with borrow	M ← (M) – i – (CY)	10011	m_H	m_L	i
Compare	SKE	m,#i	Skip if memory equal to immediate data	M–i, skip if zero	01001	m_H	m_L	i
	SKGE	m,#i	Skip if memory greater than or equal to immediate data	M–i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m,#i	Skip if memory less than immediate data	M–i, skip if borrow	11011	m_H	m_L	i
	SKNE	m,#i	Skip if memory not equal to immediate data	M–i, skip if not zero	01011	m_H	m_L	i
Logical operation	AND	m,#i	Logical AND of memory and immediate data	M ← (M) AND i	10100	m_H	m_L	i
		r,m	Logical AND of register and memory	R ← (R) AND (M)	00100	m_H	m_L	r
	OR	m,#i	Logical OR of memory and immediate data	M ← (M) OR i	10110	m_H	m_L	i
		r,m	Logical OR of register and memory	R ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m,#i	Logical XOR of memory and immediate data	M ← (M) XOR i	10101	m_H	m_L	i
		r,m	Logical XOR of register and memory	R ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r,m	Load memory of register	R ← (M)	01000	m_H	m_L	r
	ST	m,r	Store register to memory	(M) ← R	11000	m_H	m_L	r
	MOV	m,#i	Move immediate data to memory	M ← i	11101	m_H	m_L	i
Test	SKT	m,#n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M_n = all "1"	11110	m_H	m_L	n
	SKF	m,#n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M_n = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Branch	BR	addr	Jump to the address	PC←ADDR	01100	a_H	a_M	a_L
Shift	RORC	r	Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP←(SP) −1 STACK←((PC) + 1), PC←ADDR	11100	a_H	a_M	a_L
	RET		Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP		No operation	No operation	00111	100	1111	0000

11. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0C, P0D, $\overline{\text{RESET}}$		−0.3 to V_{DD}+0.3	V
		P0B	Note1	−0.3 to V_{DD}+0.3	V
			Note2	−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D		−0.3 to V_{DD}+0.3	V
		P0B	Note1	−0.3 to V_{DD}+0.3	V
			Note2	−0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, or P0D		−5	mA
		Total of all pins		−15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, or P0D		30	mA
		Total of all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C	22-pin plastic shrink DIP	400	mW
			24-pin plastic SOP	250	

Note 1. When a built-in pull-up resistor is mask-selected

2. When a built-in pull-up resistor is not mask-selected

CAPACITANCE (T_a = 25 °C, V_{DD} + 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz 0 V for pins other than pins to be measured
Input/Output Capacitance	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.5 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0C, P0D	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	P0B	**Note1**
	V_{IH4}	0.8 V_{DD}		9	V	P0B	**Note2**
Low-Level Input Voltage	V_{IL1}	0		0.25V_{DD}	V	P0A, P0C, P0D	
	V_{IL2}	0		0.15V_{DD}	V	$\overline{RESET}$	
	V_{IL3}	0		0.15V_{DD}	V	P0B	
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0			V	P0A, P0C, P0D I_{OH} = −200 μA	
Low-Level Output Voltage	V_{OL}			0.5	V	P0A, P0B, P0C, P0D I_{OL} = 600 μA	
High-Level Input Leakage Current	I_{LIH1}			5	μA	P0A, P0C, P0D, V_{IN} = V_{DD}	
	I_{LIH2}			5	μA	P0B	V_{IN} = V_{DD} **Note 1**
	I_{LIH3}			10	μA	P0B	V_{IN} = 9 V **Note 2**
Low-Level Input Leakage Current	I_{LIL1}			−5	μA	P0A, P0C, P0D, V_{IN} = 0 V	
	I_{LIL2}			−5	μA	P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			5	μA	P0A, P0C, P0D, V_{OUT} = V_{DD}	
	I_{LOH2}			5	μA	P0B	V_{OUT} = V_{DD} **Note 1**
	I_{LOH3}			10	μA	P0B	V_{OUT} = 9 V **Note 2**
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, V_{OUT} = 0 V	
Pull-Up Resistor Provided for $\overline{RESET}$ Pin	R_{RES}	20	47	95	kΩ		
Pull-Up Resistor Provided for P0B Pin	R_{P0B}	5	15	30	kΩ		
Power Supply Current **Note3**	I_{DD1}		65	150	μA	Operation mode	V_{DD} = 3 V ± 10 % f_{CC} = 200 kHz ± 20 %
	I_{DD2}		55	130	μA	HALT mode	V_{DD} = 3 V ± 10 % f_{CC} = 200 kHZ ± 20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 3 V ± 10 %

Note 1. When a built-in pull-up resistor is mask-selected

2. When a built-in pull-up resistor is not mask-selected

3. This current excludes the current which flows through the built-in pull-up resistors.

DATA MEMORY STOP MODE DATA RETENTION CHARACTERISTICS ON LOW SUPPLY VOLTAGE
(T_a = −40 to + 85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Retention Supply Voltage	V_{DDDR}	1.5		3.6	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 1.5 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 1.5 to 3.6 V)

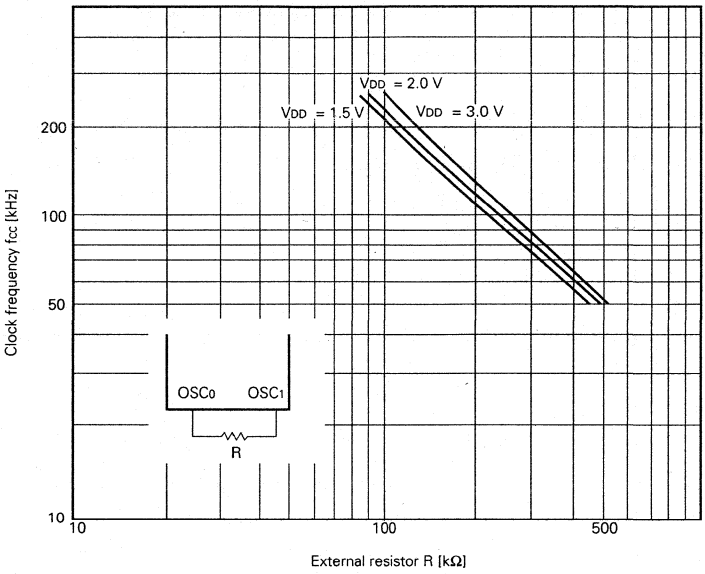
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	t_{CY}	32		160	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	t_{PBH} t_{PBL}	100			μs	
High/Low Level Width on $\overline{RESET}$	t_{RSH} t_{RSL}	100			μs	

Remark t_{CY} = 8/f_{CC} (f_{CC}: System clock oscillation frequency)

12. CHARACTERISTICS CURVE

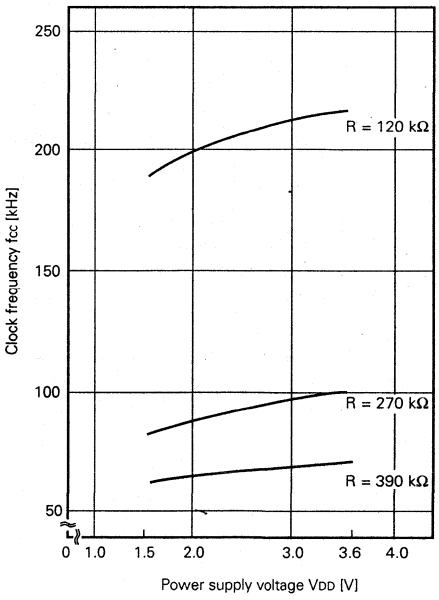
fcc vs R

(Ta = 25 °C)

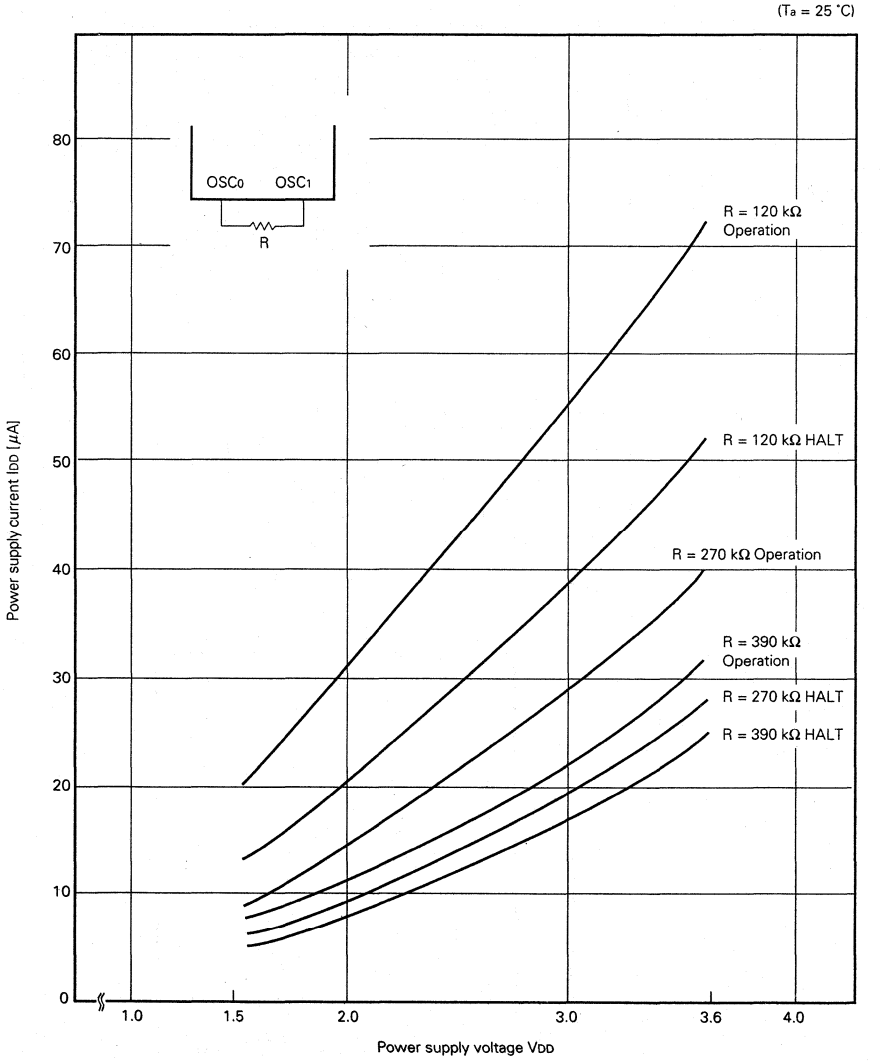


fcc vs VDD

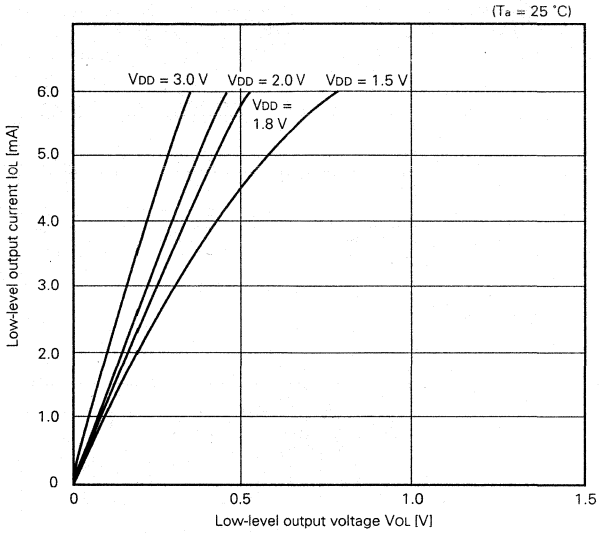
(Ta = 25 °C)



IDD vs VDD

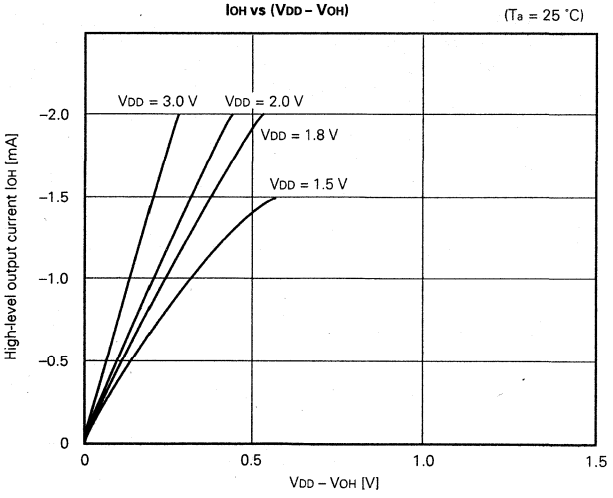

(Ta = 25 °C)
OSC0
OSC1
R
R = 120 kΩ Operation
R = 120 kΩ HALT
R = 270 kΩ Operation
R = 390 kΩ Operation
R = 270 kΩ HALT
R = 390 kΩ HALT
Power supply current IDD [μA]
80
70
60
50
40
30
20
10
0
1.0
1.5
2.0
3.0
3.6
4.0
Power supply voltage VDD

I_{OL} vs V_{OL}



Caution The absolute maximum rated current is 30 mA per pin.

I_{OH} vs (V_{DD} – V_{OH})

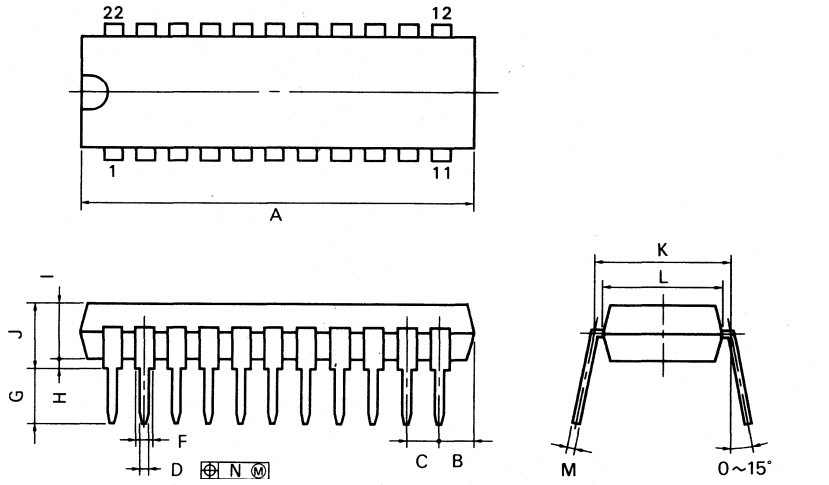


Caution The absolute maximum rated current is –5 mA per pin.

Remark The characteristics curves are reference values.

13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-300B

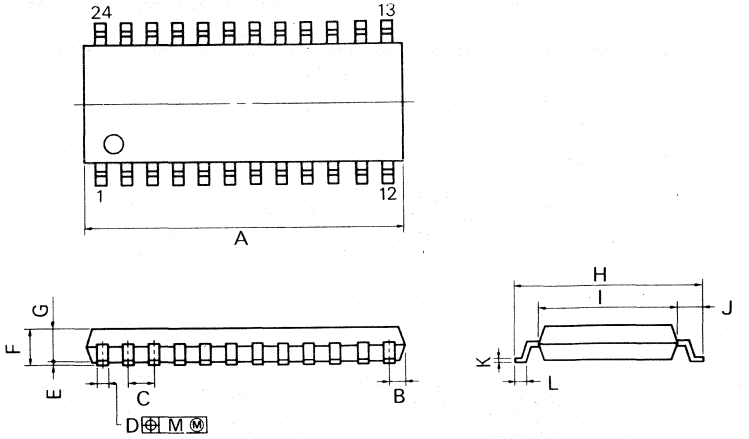
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



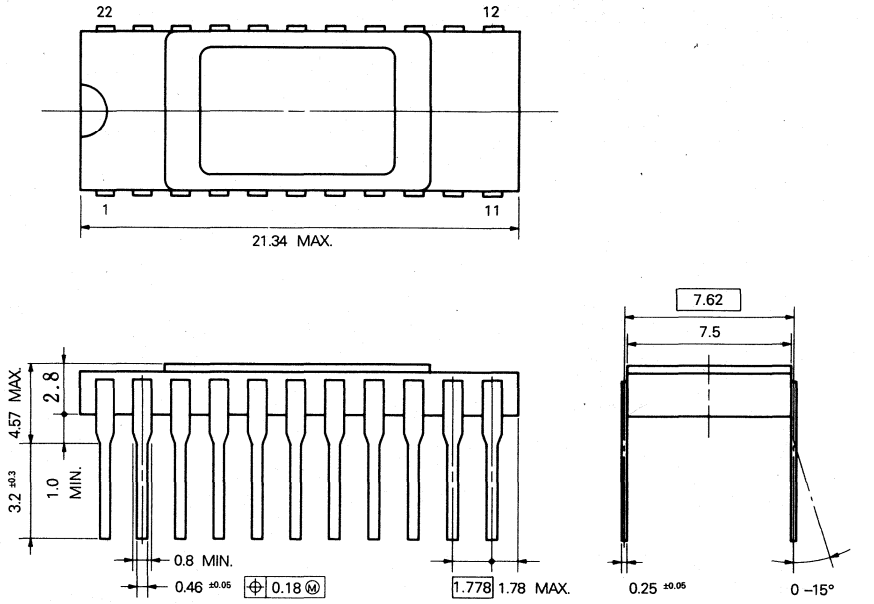
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

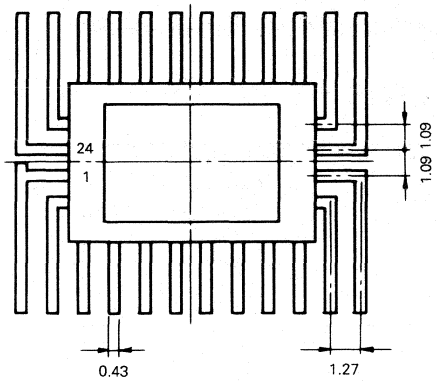
ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

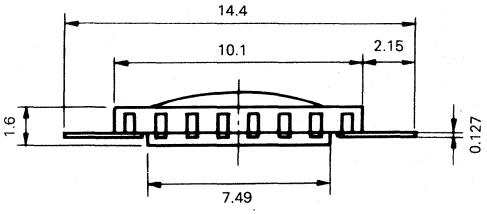
Package dimensions of the 22-pin ceramic shrink DIP (300 mil) (for ES) (Unit: mm)

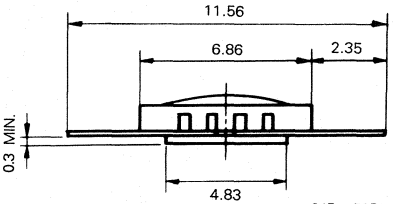


P22D – 70 – 300B

Package dimensions of the 24-pin ceramic SOP for ES (reference) (Unit: mm)







24B – 50B

14. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD17108L.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 14-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17108LCS-×××	22-pin plastic shrink DIP (300 mil)	• Wave soldering • Partial heating method
μPD17108LGS-×××	24-pin plastic SOP (300 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 14-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow process: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow process: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow process: 1
Partial heating method	Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply more than a single process at once, except for "Partial heating method."

Remark For details of the recommended soldering conditions for surface mount type products, refer to our document **"SMT MANUAL" (IEI-1207)**.

15. TINY MICROCONTROLLER FAMILY

Item	μPD17103	μPD17104	μPD17103L	μPD17140L	μPD17107	μPD17108	μPD17107L	μPD17108L
ROM size	512 x 16 bits							
RAM size	16 x 4 bits							
Number of input/ output port pins *	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)	11 (3)	16 (4)
System clock	Ceramic/crystal oscillation				RC oscillation			
Power supply voltage	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)		1.8 to 3.6 V (at 2 MHz)		2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)		1.5 to 3.6 V (at 200 kHz)	
Package	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP	• 16-pin DIP • 16-pin SOP	• 22-pin shrink DIP • 24-pin SOP
PROM version	μPD17P103	μPD17P104	μPD17P103	μPD17P104	μPD17P107	μPD17P108	μPD17P107	μPD17P108

* A number in parentheses indicates the number of input/ouput port pins selectable between N-ch open-drain and pull-up resistor connection, depending on the mask option.

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P107 is a tiny microcontroller composed of a ROM with 1K-byte capacity, a RAM with 16-word capacity and 11 I/O ports. It is a product developed by replacing the on-chip mask ROM of the μPD17107 with the one-time PROM.

The μPD17P107CX, which is writable only once, and the μPD17P107GS are available. They are convenient for evaluating or producing in small quantities the μPD17107.

Very efficient programming is possible due to the μPD17000 architecture incorporating the general-purpose register system, which allows the data memory to be manipulated directly, being adopted in the CPU. Every instruction is composed of 1 word of 16-bit length.

FEATURES

- μPD17107 compatible
- Program memory (one-time PROM): 1K byte (512 words × 16 bits)
- Data memory (RAM): 16 words × 4 bits
- I/O ports: 11 ports (N-ch open-drain output 3 ports)
- Instruction execution time: 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Instruction types: 24 types (all 1-word instructions)
- Stack levels: 1 level
- Standby function available (by STOP, HALT instruction)
- Data memory data retainable at low voltage (MIN. 2.0 V)
- With on-chip system clock oscillator (only resistor externally provided)
- Operating supply voltage: 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

APPLICATIONS

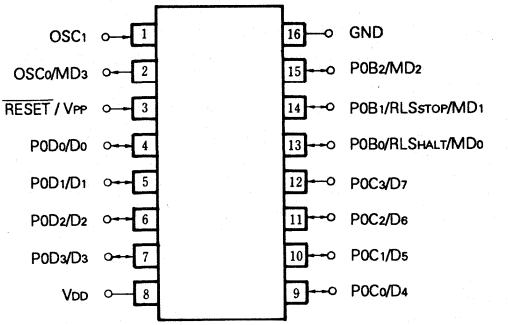
- Electronic control of home electric appliances, TOY, etc.

ORDERING INFORMATION

Order Code	Package
μPD17P107CX	16-pin plastic DIP (300 mil)
μPD17P107GS	16-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

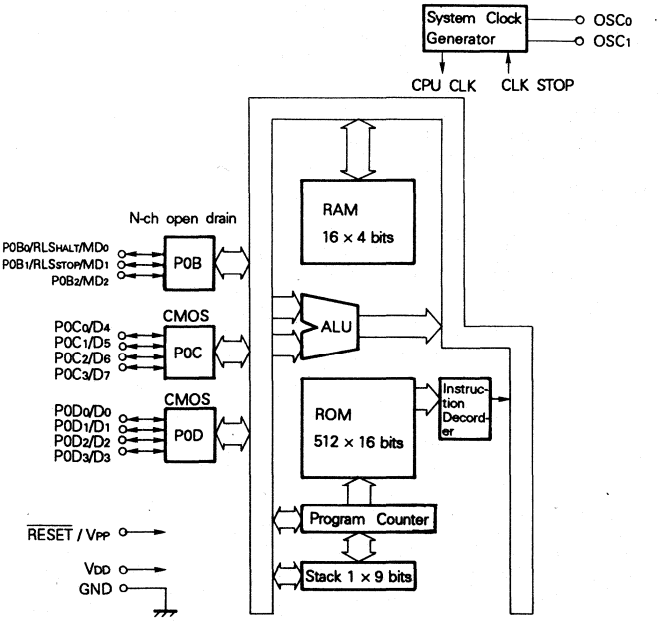
μPD17P107CX/μPD17P107GS



16 Pin Plastic DIP

16 Pin Plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

PIN FUNCTION LIST

- Port pins

Pin Name	Input/ Output	Dual-Function Pin		Function		Program Memory Write/Verify Mode	Reset
P0B0	Input/ Output	RLSHALT	MD0	• N-ch open-drain 4-bit input/ output port (Port 0B)	HALT mode releasing	Mode setting pin	High impedance (input mode)
P0B1		RLSSTOP	MD1		STOP mode releasing		
P0B2		MD2					
P0C0	Input/ Output	D4		• CMOS (push-pull) 4-bit input/output port (Port 0C)		8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
P0C1		D5					
P0C2		D6					
P0C3		D7					
P0D0	Input/ output	D0		• CMOS (push-pull) 4-bit input/output port (Port 0D)		8-bit data input/ output pin (low-order 4 bits)	High impedance (input mode)
P0D1		D1					
P0D2		D2					
P0D3		D3					

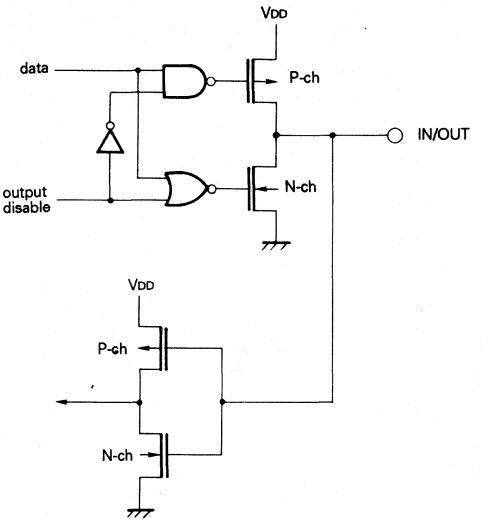
- Other than port pins

Pin Name	Input Output	Dual-Function Pin	Function	Program Memory Write/Verify Mode
$\overline{\text{RESET}}$	Input	VPP	System reset input pin	Voltage impression pin (+12.5 V)
VDD			Positive power pin	Positive power pin (+6.0 V)
GND			GND pin	GND pin
OSC1			System clock oscillation resonator connection pin	Program memory address update
OSC0		MD3	System clock oscillation resonator connection pin	Mode setting pin

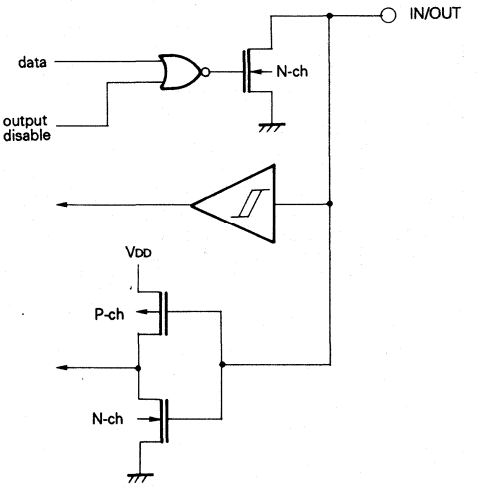
PIN INPUT/OUTPUT CIRCUITS

The μPD17P107 pin input/output circuit diagrams are shown below.

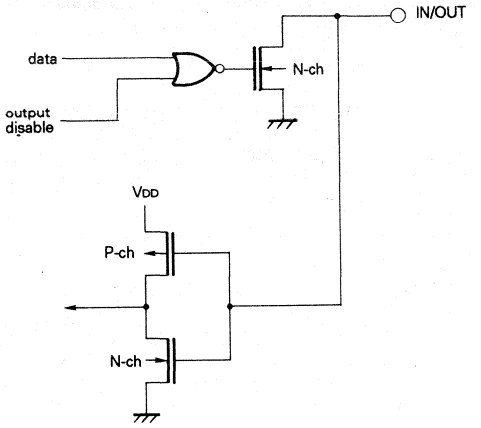
(1) P0C, P0D



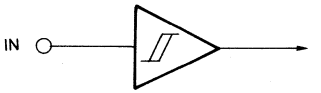
(2) P0B0, P0B1



(3) P0B2



(4) $\overline{\text{RESET}}$



9. DIFFERENCES BETWEEN μPD17P107 AND μPD17107

The μPD17P107 is a product developed by replacing the program memory of the μPD17107 with the on-chip mask ROM with the one-time PROM. These 2 models have the same CPU functions and on-chip hardware with the only difference being the program memory and the mask option. Table 9-1 shows the differences between the μPD17P107 and μPD17107.

Table 9-1 Differences between μPD17P107 and μPD17107

Item	μPD17P107	μPD17107
ROM	One-time PROM 512 × 16 bits	Mask ROM 512 × 16 bits
$P0B_0$ to $P0B_2$ pin pull-up resistor	Not available	Mask option
$\overline{RESET}$ pin pull-up resistor	Not available	Mask option
Connection pin	V_{PP} pin, run mode selection pin available	V_{PP} pin, run mode selection pin not available
Input power	2.5 to 6.0 V (at 250 kHz) 4.5 to 6.0 V (at 1 MHz)	
Package	16-pin DIP 16-pin SOP	

10. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The μPD17P107's on-chip program memory is a 512 × 16-bit one-time PROM.

To write/verify this one-time PROM, the pins shown in the table below are used. No address input is available. Instead, a system to update the address by the clock input via the OSC_1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage impression pin at program memory write/verify
OSC_1	Address updating clock input pin at program memory write/verify
MD_0 to MD_3	Input pin at program memory write/verify. Used as run mode selection pin.
D_0 to D_7	8-bit data input/output pin at program memory write/verify

10.1 RUN MODE AT PROGRAM MEMORY WRITE/VERIFY

The μPD17P107 assumes the program memory write/verify mode if +6 V is impressed to the V_{DD} pin and +12.5 V is impressed to the V_{PP} pin after the reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V) assumed for a certain period of time. In that mode, the following run mode is entered according to the MD_0 to MD_3 pin setting. All the remaining pins are at the GND potential by the pull-down resistor.

Run Mode Setting						Run Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

x: L or H

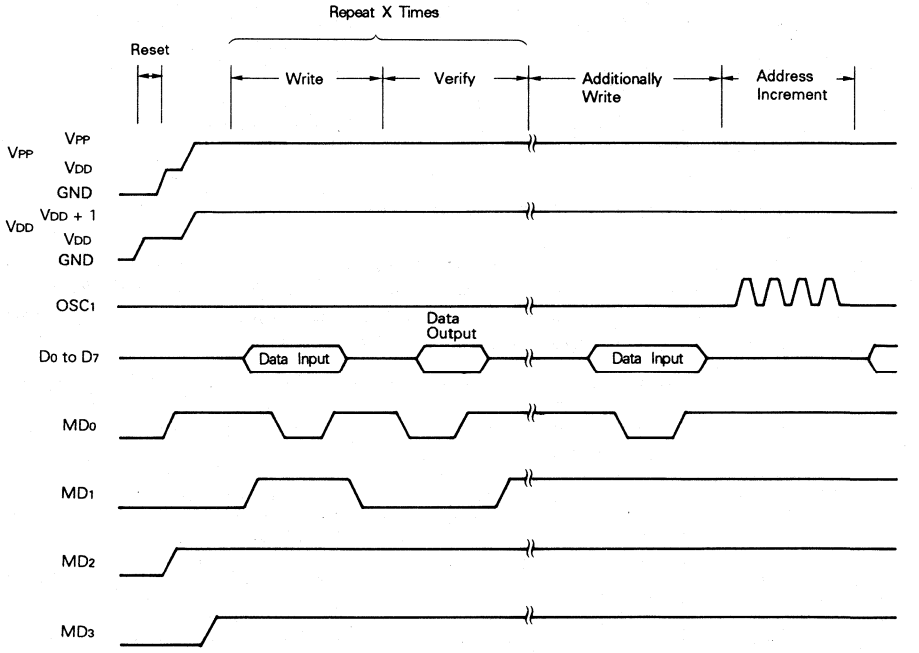
10.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down the pins not to be used to GND via the resistor. The OSC_1 pin at the low level.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
(3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to the program memory address 0 clear mode.
(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Assume the program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) Assume the program inhibit mode.
(9) Assume the verify mode. If written, go to (10). If not, repeat (7) to (9).

(10) Additionally write (number of times written in (7) to (9): X) × 1 ms.
(11) Assume the program inhibit mode.
(12) Update (+1) the program memory address by inputting a pulse to the OSC_1 pin 4 times.
(13) Repeat (7) to (12) up to the last address.
(14) Assume the program memory address 0 clear mode.
(15) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(16) Power off.

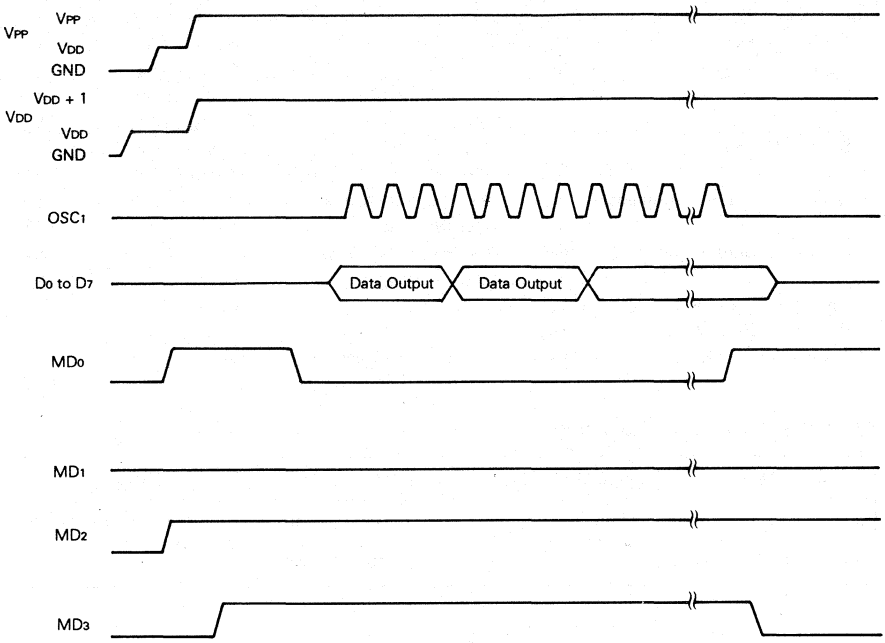
The above procedure of (2) to (12) is shown in the diagram below.



10.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the pins not to be used to GND via the resistor. The OSC_1 pin at the low level.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin at the low level.
(3) Wait 10 μs and then supply 5 V to the V_{PP} pin.
(4) Set the mode setting pin to the program memory address 0 clear mode.
(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Assume the program inhibit mode.
(7) Assume the verify mode. Output data sequentially 1 address at a time at intervals of 4 inputs when a clock pulse is input to the OSC_1 pin.
(8) Assume the program inhibit mode.
(9) Assume the program memory address 0 clear mode.
(10) Change the V_{DD}, V_{PP} pin voltage to 5 V.
(11) Power off.

The above procedure of (2) to (9) is shown in the diagram below.



13. ELECTRIC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Supply Voltage	V_{PP}			−0.3 to +13.5	V
Input Voltage	V_I	P0C, P0D, $\overline{\text{RESET}}$		0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
Output Voltage	V_O	P0C, P0D		0.3 to V_{DD} +0.3	V
		P0B		−0.3 to +11	V
High-level Output Amperage	I_{OH}	P0B, P0C, P0D per pin		−5	mA
		Total for all pins		−15	mA
Low-level Output Amperage	I_{OL}	P0B, P0C, P0D per pin		30	mA
		Total for all pins		100	mA
Operating Temperature	T_{opt}			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C	16 pin DIP	400	mW
			16 pin SOP	190	mW

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_{IN}			15	pF	f = 1 MHz, 0 V at other than measured pins
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than specified below.	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B*	
	V_{IH4}	V_{DD} - 0.5		V_{DD}	V	OSC_1	
Low-level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than specified below.	
	V_{IL2}	0		0.2 V_{DD}	V	P0B, $\overline{RESET}$	
	V_{IL3}	0		0.5	V	OSC_1	
P0C, D High-level Output Voltage	V_{OH}	V_{DD} - 2.0			V	V_{DD} = 4.5 to 6.0 V I_{OH} = −2 mA	
		V_{DD} - 1.0			V	I_{OH} = −200 μA	
P0B, C, D Low-level Input Voltage	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
P0B, C, D High-level Input Leak Current	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V*	
P0B, C, D Low-level Input Leak Current	I_{LIL}			−5	μA	V_{IN} = 0 V	
P0B, C, D High-level Output Leak Current	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V*	
P0B, C, D Low-level Output Leak Current	I_{LOL}			−5	μA	V_{OUT} = 0 V	
Supply Amperage	I_{DD1}		0.4	1.2	mA	Run mode	V_{DD} = 5 V ±10 % f_{CC} = 1.0 MHz ±20 %
			50	150	μA		V_{DD} = 3 V ±10 % f_{CC} = 250 kHz ±20 %
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ±10 % f_{CC} = 1.0 MHz ±20 %
			40	120	μA		V_{DD} = 3 V ±10 % f_{CC} = 250 kHz ±20 %
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10 %
			0.1	5	μA		V_{DD} = 3 V ±10 %

*: If N-ch open-drain input/output selected.

LOW-SUPPLY VOLTAGE DATA HOLDING CHARACTERISTICS IN DATA MEMORY STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Holding Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Holding Supply Amperage	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
$P0B_0$, $P0B_1$, High/Low Level Width	T_{PBH} T_{PBL}	10			μs	
$\overline{RESET}$, High/Low Level Width	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than OSC_1
	V_{IH2}	V_{DD} - 0.5		V_{DD}	V	OSC_1
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than OSC_1
	V_{IL2}	0		0.4	V	OSC_1
Input Leak Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

NOTE 1: V_{PP} must not be a minimum of +13.5 V including overshoot.
2: Impress V_{DD} before V_{PP} and break it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

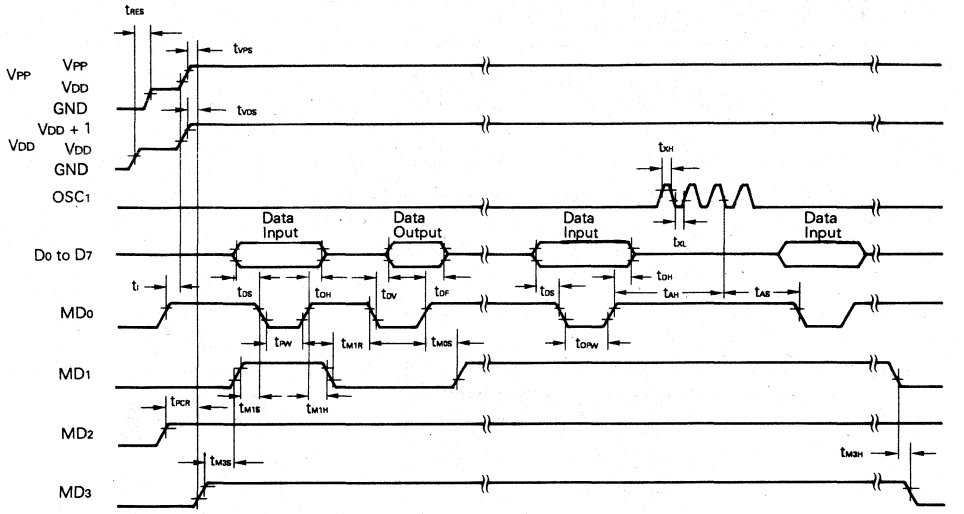
CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set-Up Time *2 (for MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Set-Up Time (for MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data Set-Up Time (for MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time *2 (for MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (for MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Set-Up Time (for MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Set-Up Time (for MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITION
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Set-Up Time (for MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (for MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recover Time (for MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	-	10			μs	
OSC_1 Input High/Low Level Width	t_{XH}, t_{XL}	-	0.42			μs	
OSC_1 Input Frequency	f_{OSC}	-			1.2	MHz	
Initial Mode Set Time	t_I	-	2			μs	
MD3 Set-Up Time (for MD1 ↑)	t_{M3S}	-	2			μs	
MD3 Hold Time (for MD1 ↓)	t_{M3H}	-	2			μs	
MD3 Set-Up Time (for MD0 ↓)	t_{M3SR}	-	2			μs	At program memory read
Address *2 → Data Output Delay Time	t_{DAD}	t_{ACC}	2			μs	At program memory read
Address *2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	At program memory read
MD3 Hold Time (for MD0 ↑)	t_{M3HR}	-	2			μs	At program memory read
MD3 ↓→ Data Output Float Delay Time	t_{DFR}	-	2			μs	At program memory read
Reset Set-Up Time	t_{RES}		10			μs	

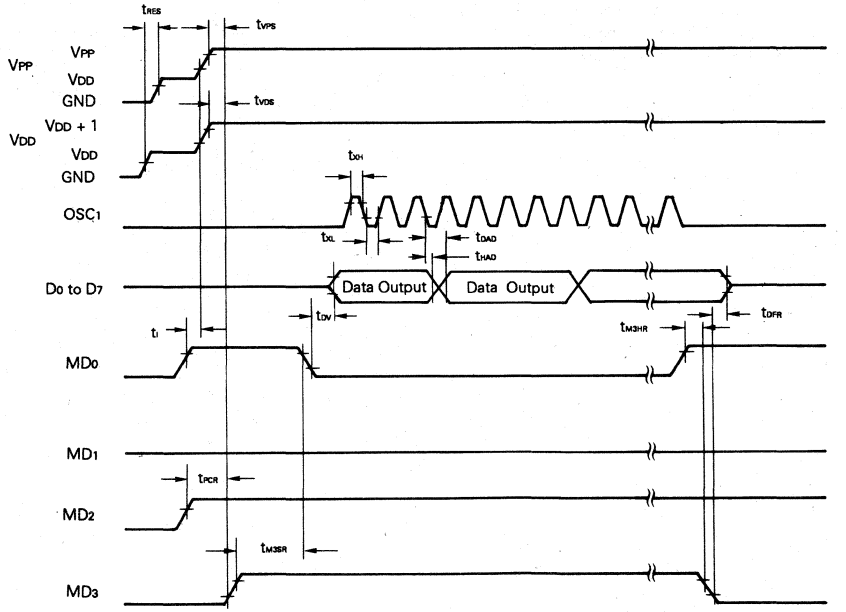
*1: A symbol of the corresponding μPD27C256.

*2: The internal address signal is incremented (+1) at the 3rd OSC_1 input falling and is not connected to a pin.

PROGRAM MEMORY WRITING TIMING

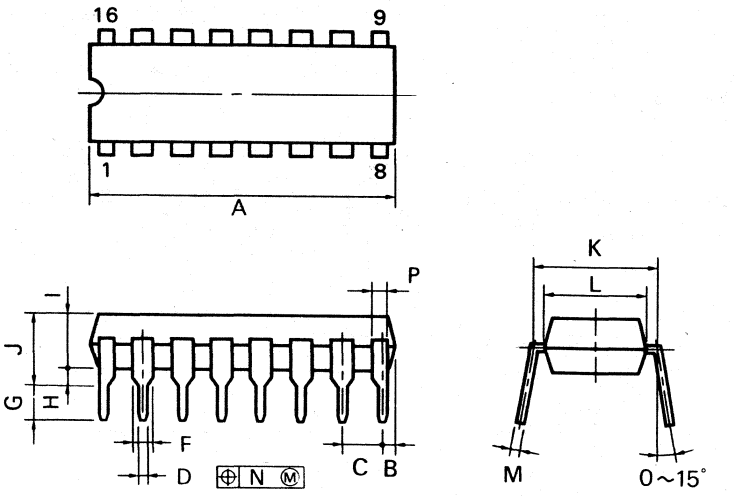


PROGRAM MEMORY READING TIMING



13. PACKAGE DIMENSIONS

16PIN PLASTIC DIP (300 mil)



P16C-100-300B

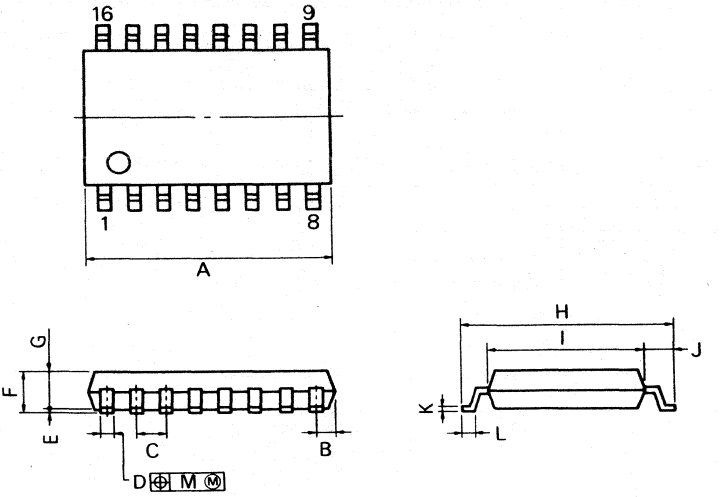
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{-0.10}$	$0.020^{-0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.5^{-0.3}$	$0.138^{-0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{-0.10}_{-0.05}$	$0.010^{-0.004}_{-0.003}$
N	0.25	0.01
P	1.1 MIN.	0.043 MIN.

16PIN PLASTIC SOP (300 mil)



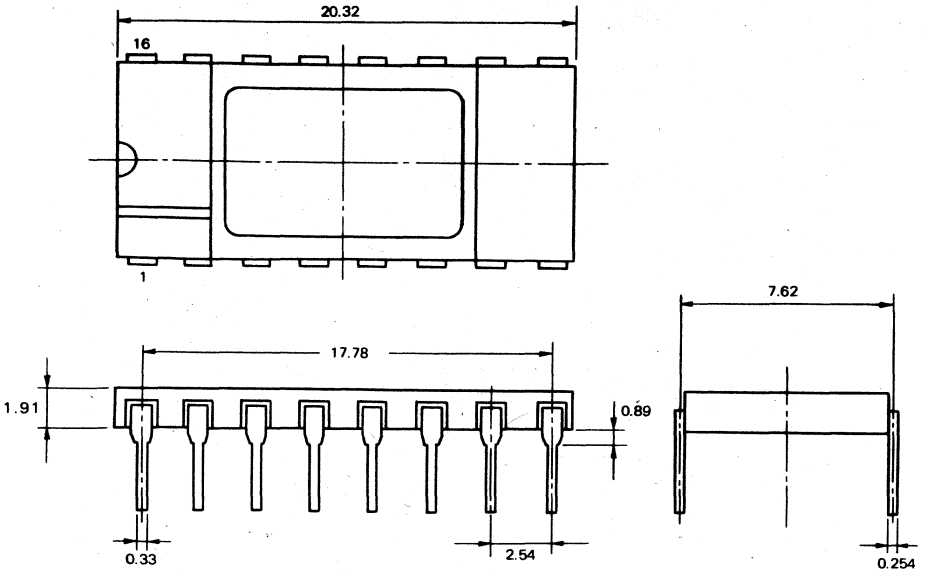
P16GM-50-300B-1

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

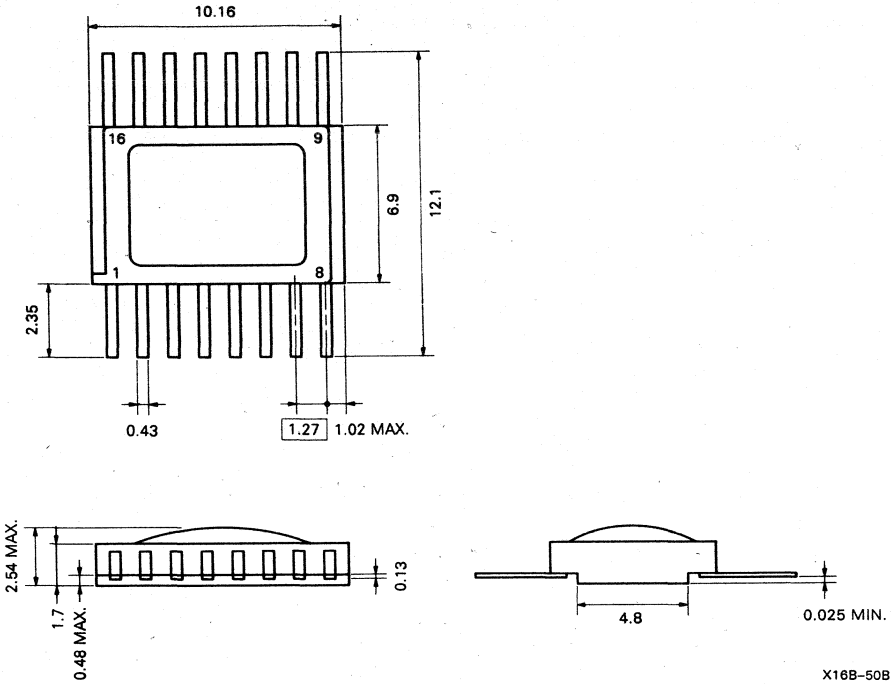
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

PACKAGE DIMENSION FOR ENGINEERING SAMPLE 16-PIN CERAMIC DIP (for reference) (Unit: mm)



PACKAGE DIMENSION FOR ENGINEERING SAMPLE 16-PIN CERAMIC SOP (for reference) (Unit: mm)



X16B-50B

4-BIT SINGLE CHIP MICROCONTROLLER

The μPD17P108 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17108, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P108 models are available: μPD17P108CS and μPD17P108GS, which allow a program to be written only once. They are suitable for evaluation of μPD17108 and for small-scale production.

The 17K architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

- Compatible with the μPD17108
- Program memory (one-time PROM) : 1K bytes (512 words x 16 bits)
- Data memory (RAM) : 16 words x 4 bits
- Input/output ports : 16 ports (including four N-ch open-drain outputs)
- Instruction execution time : 128 μs (62.5 kHz) to 8 μs (1 MHz)
- Number of instructions : 24 (Each instruction is 1 word long.)
- Stack level : 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock. (Only resistors are mounted externally.)
- Operating supply voltage : 2.5 to 6.0 V (at 250 kHz)
  4.5 to 6.0 V (at 1 MHz)

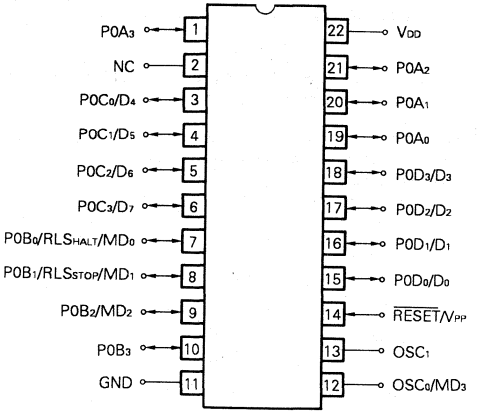
APPLICATIONS

- Controlling electric appliances or toys

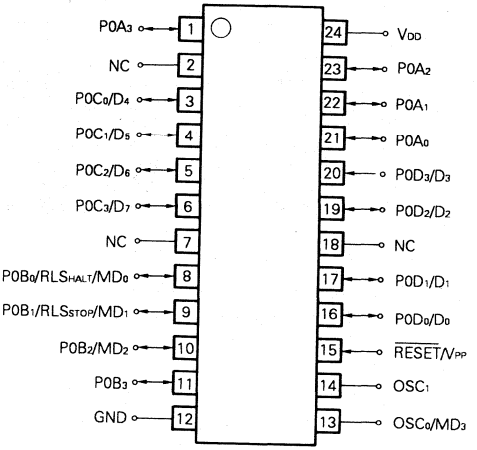
ORDERING INFORMATION

Order Code	Package
μPD17P108CS	22-pin plastic shrink DIP (300 mil)
μPD17P108GS	24-pin plastic SOP (300 mil)

PIN CONFIGURATION (Top View)

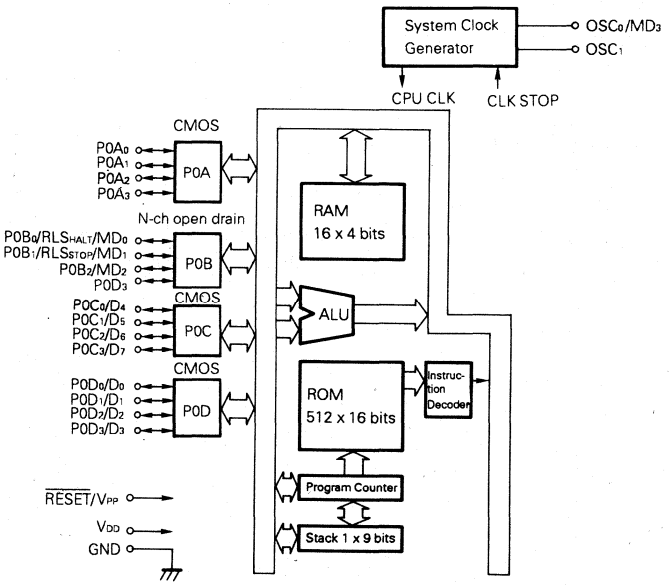


22-pin plastic shrink DIP



24-pin plastic SOP

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Functions

- Port pins

Pin name	Input/ output	Dual function pin	Function	When writing to program memory or verifying its contents	When reset
$P0A_0$	Input/ output		CMOS (push-pull) 4-bit input/output port (port 0A)	Pull down	High impedance (input mode)
$P0A_1$					
$P0A_2$					
$P0A_3$					
$P0B_0$	Input/ output	RLS_{HALT} MD_0	N-ch open-drain 4-bit input/output port (port 0B)	Mode selection pin	High impedance (input mode)
$P0B_1$		RLS_{STOP} MD_1	For the HALT mode releasing		
$P0B_2$		MD_2	For the STOP mode releasing		
$P0B_3$				Pull down	
$P0C_0$	Input/ output	D_4	CMOS (push-pull) 4-bit input/output port (port 0C)	8-bit data input/ output pin (high-order 4 bits)	High impedance (input mode)
$P0C_1$		D_5			
$P0C_2$		D_6			
$P0C_3$		D_7			
$P0D_0$	Input/ output	D_0	CMOS (push-pull) 4-bit input/output port (port 0D)	8-bit data input/ output pin (low-order 4 bits)	High impedance (input mode)
$P0D_1$		D_1			
$P0D_2$		D_2			
$P0D_3$		D_3			

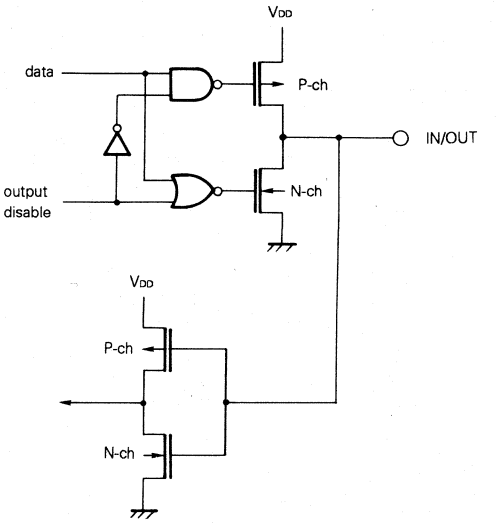
- Non-port pins

Pin name	Input/ output	Dual Function pin	Function	When writing to program memory or verifying its contents
$\overline{RESET}$	Input	V_{PP}	System reset input pin	Voltage is applied to this pin (+12.5 V)
V_{DD}			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
OSC_1			Pins to be connected to the system clock resonator	Program memory address update
OSC_0		MD_3	Pins to be connected to the system clock resonator	
NC			NC pin is not connected internally.	Mode selection pin

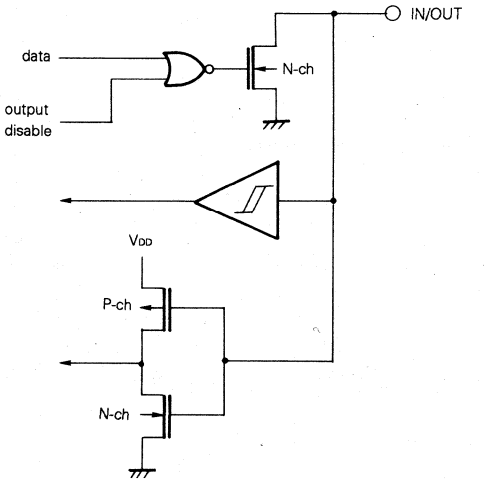
PIN INPUT/OUTPUT CIRCUITS

Following are schematics of the input/ouput circuits of the pins of the μPD17P108.

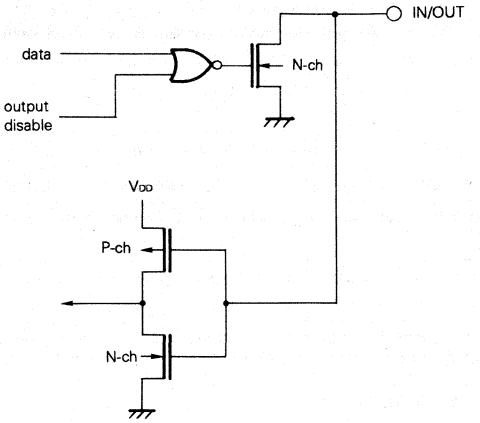
(1) P0A, P0C, and P0D



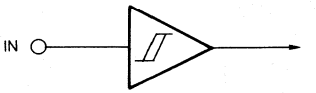
(2) P0B0 and P0B1



(3) $P0B_2$ and $P0B_3$



(4) $\overline{\text{RESET}}$



10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P108's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the OSC_1 pin.

Pin name	Function
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
OSC_1	Input pin for address update clock used when writing to program memory or verifying its contents
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P108 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

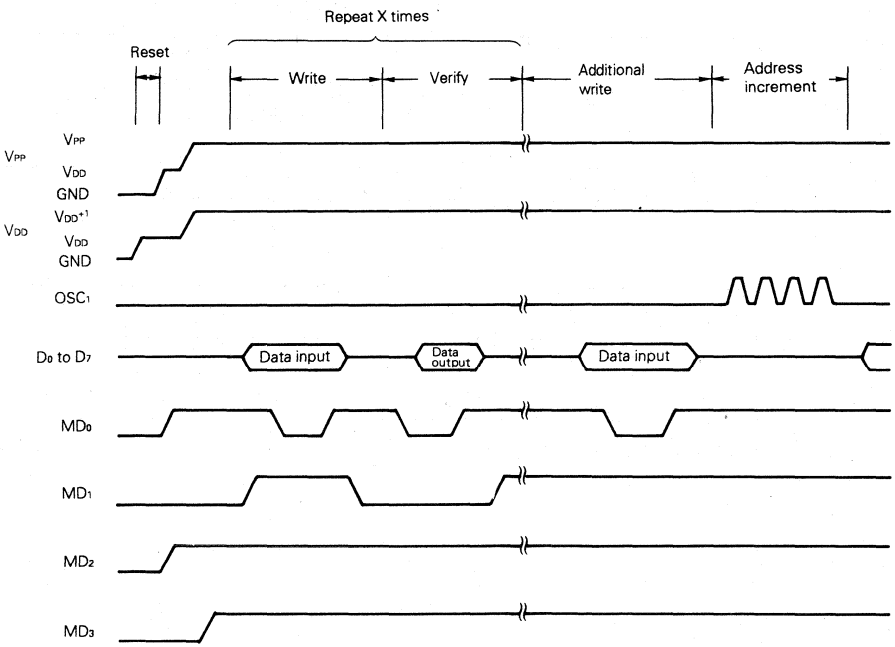
x : L (low) or H (high)

10.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring OSC_1 to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9) x 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the OSC_1 pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

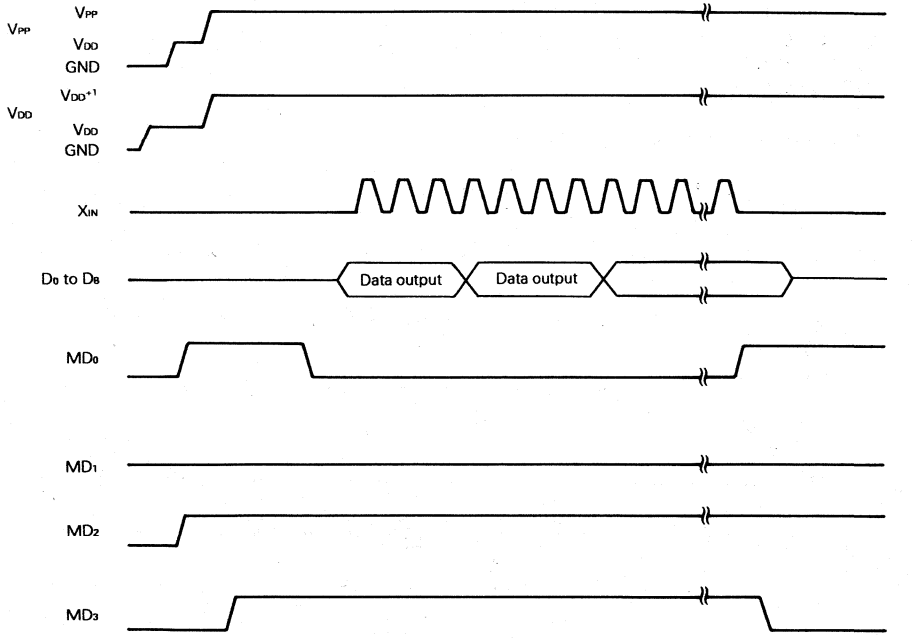
The timing for steps (2) to (12) is shown below.



10.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring OSC_1 to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the OSC_1 pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for steps (2) to (9) is shown below.



13. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		−0.3 to +7.0	V
Supply Voltage	V_{PP}		−0.3 to +13.5	V
Input Voltage	V_I	P0A, P0C, P0D	−0.3 to V_{DD}+0.3	V
		P0B	−0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D	−0.3 to V_{DD}+0.3	V
		P0B	−0.3 to +11	V
High-Level output Current	I_{OH}	Each of P0A, P0B, P0C, P0D	−5	mA
		Total of all pins	−15	mA
Low-Level output Current	I_{OL}	Each of P0A, P0B, P0C, P0D	30	mA
		Total of all pins	100	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Power Consumption	P_d	T_a = 85 °C 22-pin shrink DIP	400	mW
		24-pin SOP	250	

CAPACITY (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			15	pF	f = 1 MHz
Input/Output Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IH3}	0.8 V_{DD}		9	V	P0B	(*)
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	OSC_1	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than the following pins and port	
	V_{IL2}	0		0.2 V_{DD}	V	P0B and $\overline{RESET}$	
	V_{IL3}	0		0.5	V	OSC_1	
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	V_{DD} − 2.0			V	V_{DD} = 4.5 to 6.0 V, I_{OH} = −2 mA	
		V_{DD} − 1.0			V	I_{OH} = −200 μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA	
				0.5	V	I_{OL} = 600 μA	
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	V_{IN} = 9 V	(*)
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			−5	μA	V_{IN} = 0 V	
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	V_{OUT} = 9 V	(*)
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			−5	μA	V_{OUT} = 0 V	
Power Supply Current	I_{DD1}		0.4	1.2	mA	Operation mode	V_{DD} = 5 V ±10%, f_{CC} = 1.0 MHz ±20%
			50	150	μA		V_{DD} = 3 V ±10% f_{CC} = 250 kHz ±20%
	I_{DD2}		0.3	0.9	mA	HALT mode	V_{DD} = 5 V ±10%, f_{CC} = 1.0 MHz ±20%
			40	120	μA		V_{DD} = 3 V ±10% f_{CC} = 250 kHz ±20%
	I_{DD3}		0.1	10	μA	STOP mode	V_{DD} = 5 V ±10%
			0.1	5	μA		V_{DD} = 3 V ±10%

* When N-ch open-drain input/output is selected

CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE IN THE STOP MODE (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	V_{DDDR} = 2.0 V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.5 to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Internal Clock Cycle Time	T_{CY}	6.6		160	μs	V_{DD} = 4.5 to 6.0 V
		26.6		160	μs	
High/Low Level Width on $P0B_0$ and $P0B_1$	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except OSC_1
	V_{IH2}	V_{DD} −0.5		V_{DD}	V	OSC_1
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except OSC_1
	V_{IL2}	0		0.4	V	OSC_1
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD} −1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1. V_{PP} must be under +13.5 V including overshoot.
2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

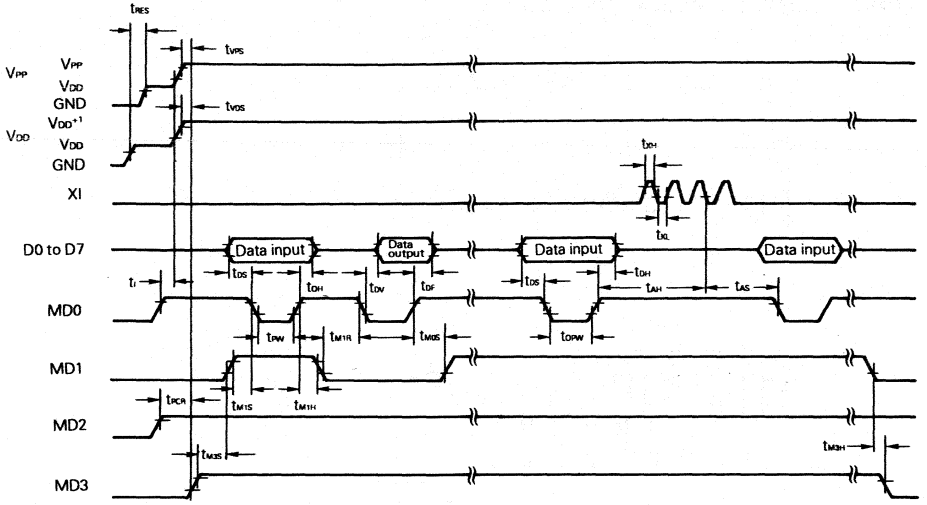
CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time to MD0↓ (*2)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time to MD0↑ (*2)	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	
MD1 Hold Time to MD0↑	t_{M1H}	t_{OEH}	2			μs	MD0 = MD1 = V_{IL}
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	$t_{M1H} = t_{M1R} \geq 50$ μs
OSC_1 Input High, Low Level Range	t_{XH}, t_{XL}	–	0.42			μs	
OSC_1 Input Frequency	f_{OSC}				1.2	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time From Address (*2)	t_{DAD}	–	2			μs	Read program memory
Data Output Hold Time From Address (*2)	t_{HAD}	t_{ACC}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	t_{OH}	2			μs	Read program memory
Data Output float Delay Time From MD3↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}	–	10			μs	

*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third OSC_1 input, and it is not connected to the pin.

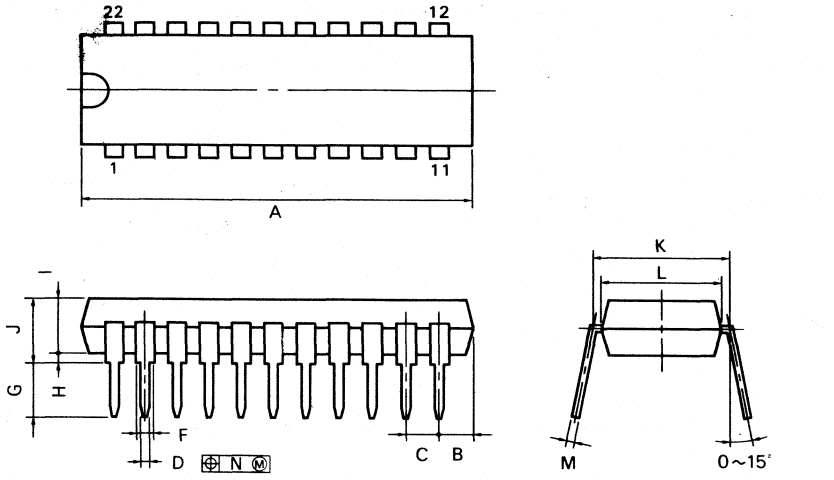
2

Write program memory timing



13. PACKAGE DIMENSIONS

22PIN PLASTIC SHRINK DIP (300 mil)



S22C-70-3008

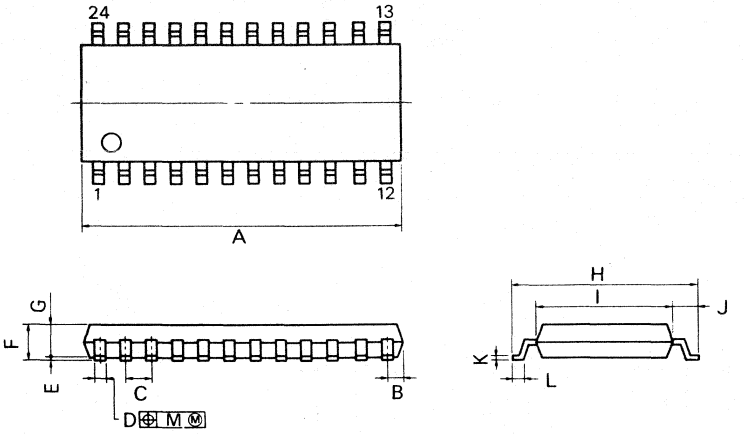
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



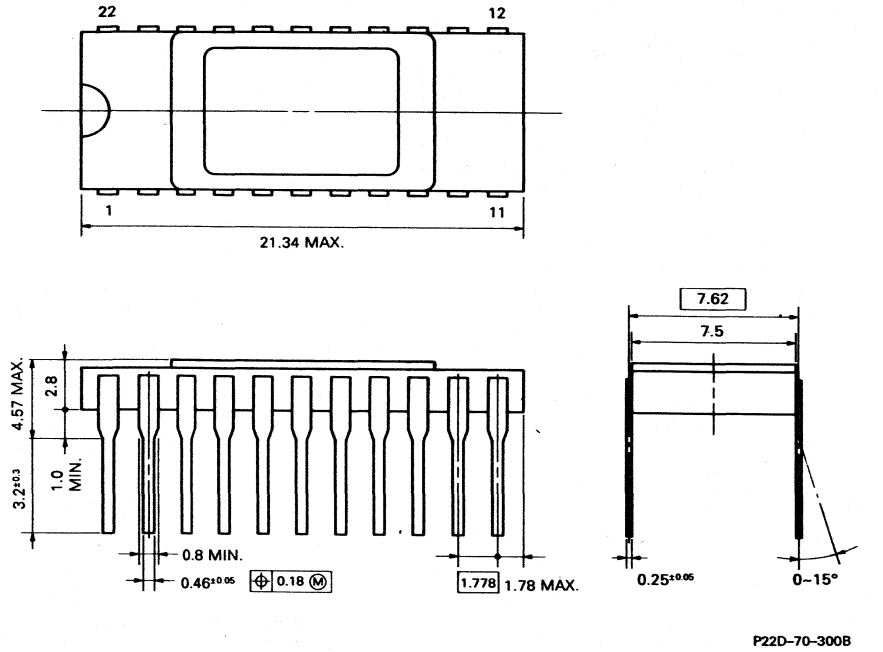
P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

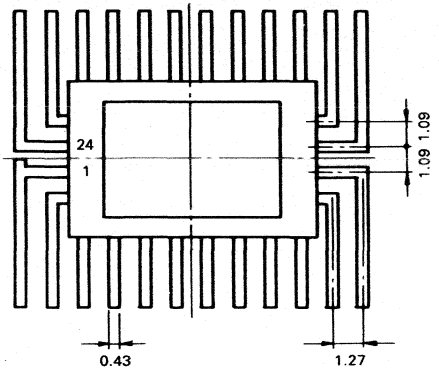
ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

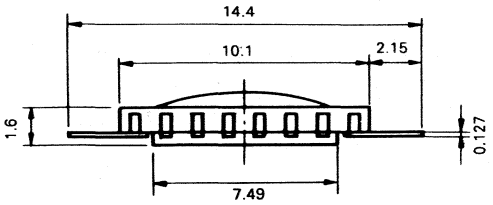
PACKAGE DIMENSIONS OF THE 22-PIN CERAMIC SHRINK DIP FOR ES (reference) (Unit: mm)

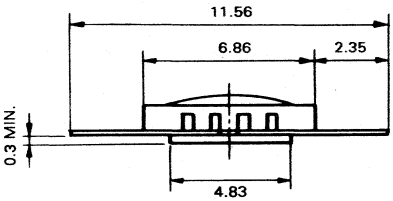


P22D-70-300B

PACKAGE DIMENSION FOR ENGINEERING SAMPLE 24 PIN CERAMIC SOP (for reference) (Unit: mm)







24B-50B

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17120 and μPD17121 are 4-bit single-chip microcontrollers containing a ROM (768 x 16 bits), RAM (64 x 4 bits), input/output ports (18 pins), a one-channel 8-bit timer, and a 3-wire serial interface.

The CPUs of the μPD17120 and μPD17121 employ the 17K architecture that has no accumulator and that enables manipulating data memory directly, thus allowing effective programming. Instructions for the μPD17120 and μPD17121 are all one word long, each consisting of 16 bits.

Since these microcontrollers have a one-channel timer, they facilitate implementation of electronic control of electric home appliances such as an electric fan.

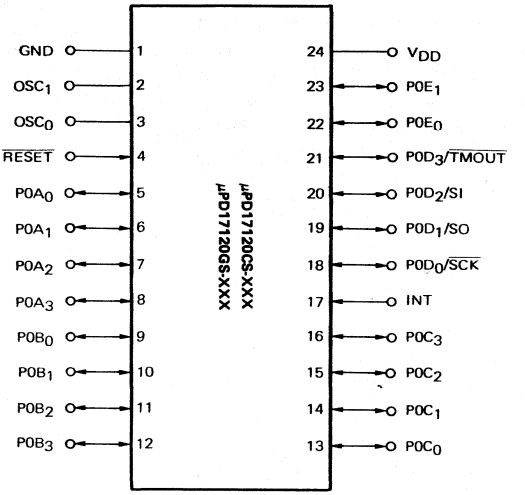
The μPD17P132 and μPD17P133, one-time PROMs (can be written to only once), are available for evaluation of the μPD17120 and μPD17121 and for small-scale production.

FEATURES

- 17K architecture is used.
- Program memory (ROM) : 768 x 16 bits
- Data memory (RAM) : 64 x 4 bits
- External interrupt : 1 line (INT pin, with sensor input)
- Stack level : 5 levels (for interrupt: 1 level)
- Instruction execution time:
  - μPD17120: 8 μs (at 2 MHz), RC oscillation (Note), V_{DD} = 5 V
  - μPD17121: 2 μs (at 8 MHz), ceramic oscillation V_{DD} = 5 V
- 8-bit timer : 1 channel
- 3-wire serial interface : 1 channel
- Input/output pins : 18 pins (including 6 N-ch open-drain input/output pins)
- Standby function (HALT,STOP) provided
- Operating voltage : 2.7 to 5.5 V
- Power-on/Powerdown reset circuit

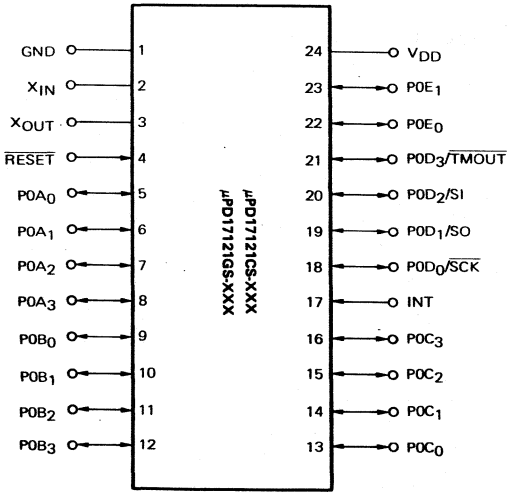
Note The capacitor for RC oscillation is contained in the μPD17120.

PIN CONFIGURATION FOR THE μPD17120 (Top View)



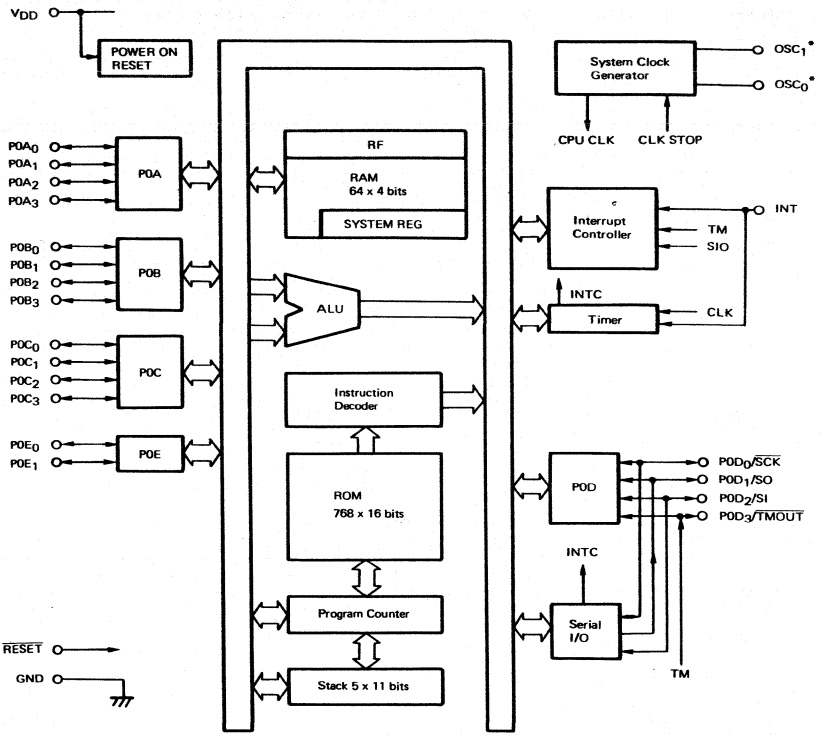
24-pin plastic shrink DIP
24-pin plastic SOP

PIN CONFIGURATION FOR THE μPD17121 (Top View)



24-pin plastic shrink DIP
24-pin plastic SOP

BLOCK DIAGRAM FOR THE μPD17120 AND μPD17121



*: The pins OSC_1 and OSC_0 in the μPD17120 correspond to pins X_{IN} and X_{OUT} in the μPD17121, respectively.

MICROCONTROLLER FAMILY FOR SMALL WHITE GOODS APPLIANCES

Item	μPD17120*	μPD17121*	μPD17132*	μPD17133*	Remarks
ROM size	768 x 16 bits		1024 x 16 bits		
RAM size	64 x 4 bits		111 x 4 bits		
Number of I/O port lines	18				Including 6 N-ch open drain lines
External interrupt	1				With sensor input
Analog input	None		Comparator (4 channels)		Also used as port pins
Timer	1 timer				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on/Powerdown reset	Provided				
System clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	
Instruction execution time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby	Provided				STOP,HALT
Power supply	2.7 to 5.5 V				
Package	28-pin shrink DIP 28-pin SOP				
One time PROM product	μPD17P132	μPD17P133	μPD17P132	μPD17P133	

Item	μPD17134A	μPD17135A	μPD17136A	μPD17137A	Remarks
ROM size	1024 x 16 bits		2048 x 16 bits		
RAM size	112 x 4 bits				
Number of I/O port lines	21 lines (including one input line)				Including 8 N-ch open drain lines
External interrupt	1				With sensor input
Analog input	8-bit A/D convertor (4 channels)				Also used as port pins
Timer	3 timers				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on/Powerdown reset	Provided				
System clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	
Instruction execution time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby function	Provided				STOP,HALT
Power supply	2.7 to 5.5 V				5 V ± 10 % for A/D converter
Package	28-pin shrink DIP 28-pin SOP				
One time PROM product	μPD17P136A	μAD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output

*: Under development

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17132 and μPD17133 are 4-bit single-chip microcontrollers containing a 4-channel comparator, ROM (1024 x 16 bits), RAM (111 x 4 bits), input/output ports (18 pins), and a one-channel 8-bit timer.

The CPUs of the μPD17132 and μPD17133 employ the 17K architecture that has no accumulator and that enables manipulating data memory directly, thus allowing effective programming. Instructions for the μPD17132 and μPD17133 are all one word long, each consisting of 16 bits.

Since these microcontrollers have a comparator, they facilitate implementation of electronic control of electric home appliances.

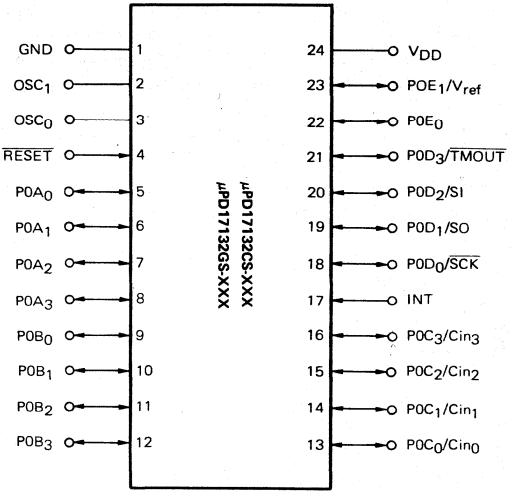
The μPD17P132 and μPD17P133, one-time PROMs (can be written to only once), are available for evaluation of the μPD17132 and μPD17133 and for small-scale production.

FEATURES

- 17K architecture is used.
- Program memory (ROM) : 1024 x 16 bits
- Data memory (RAM) : 111 x 4 bits
- External interrupt : 1 line (INT pin, with sensor input)
- Stack level : 5 levels (for interrupt: 1 level)
- Instruction execution time:
  - μPD17132: 8 μs (at 2 MHz), RC oscillation (Note), V_{DD} = 5 V
  - μPD17133: 2 μs (at 8 MHz), ceramic oscillation V_{DD} = 5 V
- 8-bit timer : 1 channel
- Comparator input : 4 channels (Built-in comparator compares signals with the external V_{ref} pin signal. Also usable as a 4-bit A/D converter using internal power supply (V_{DD}).)
- 3-wire serial interface : 1 channel
- Input/output pins : 18 pins (including 6 N-ch open-drain input/output pins)
- Standby function (HALT,STOP) provided
- Operating voltage : 2.7 to 5.5 V
- Power-on/Powerdown reset circuit

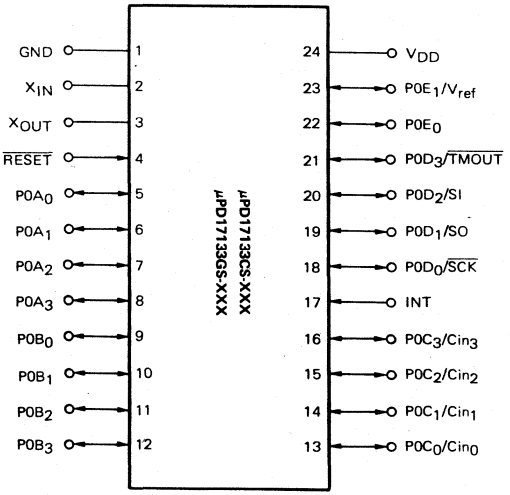
Note The capacitor for RC oscillation is contained in the μPD17132.

PIN CONFIGURATION FOR THE μPD17132 (Top View)



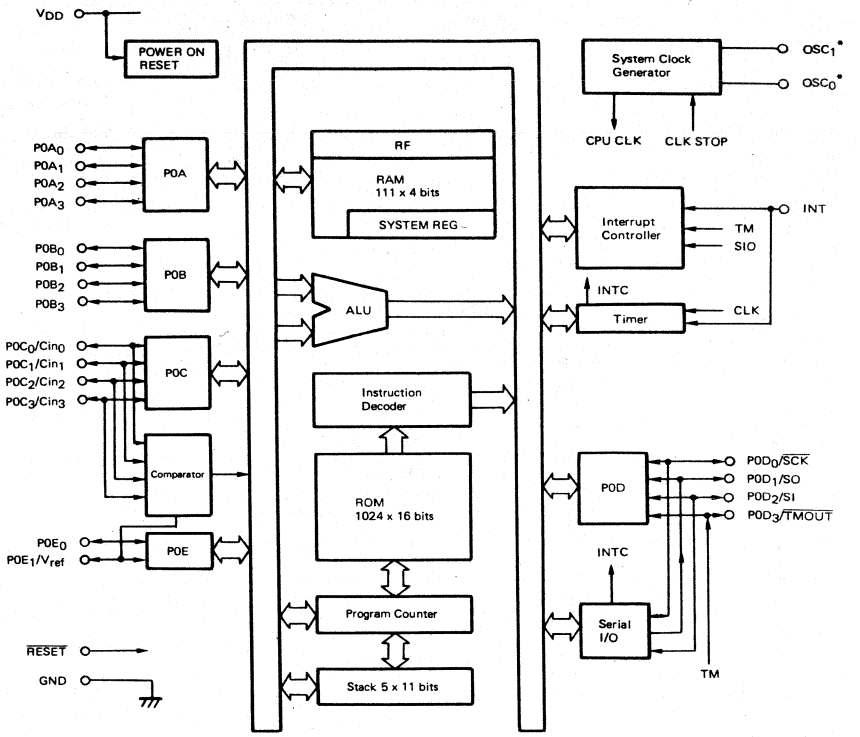
24-pin plastic shrink DIP
24-pin plastic SOP

PIN CONFIGURATION FOR THE μPD17133 (Top View)



24-pin plastic shrink DIP
24-pin plastic SOP

BLOCK DIAGRAM FOR THE μPD17132 AND μPD17133



*: The pins OSC_1 and OSC_0 in the μPD17132 correspond to pins X_{IN} and X_{OUT} in the μPD17133, respectively.

MICROCONTROLLER FAMILY FOR SMALL WHITE GOODS APPLIANCES

Item	μPD17120*	μPD17121*	μPD17132*	μPD17133*	Remarks
ROM size	768 x 16 bits		1024 x 16 bits		
RAM size	64 x 4 bits		111 x 4 bits		
Number of I/O port lines	18				Including 6 N-ch open drain lines
External interrupt	1				With sensor input
Analog input	None		Comparator (4 channels)		Also used as port pins
Timer	1 timer				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on/Powerdown reset	Provided				
System clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	
Instruction execution time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby	Provided				STOP,HALT
Power supply	2.7 to 5.5 V				
Package	28-pin shrink DIP 28-pin SOP				
One time PROM product	μPD17P132	μPD17P133	μPD17P132	μPD17P133	

Item	μPD17134A	μPD17135A	μPD17136A	μPD17137A	Remarks
ROM size	1024 x 16 bits		2048 x 16 bits		
RAM size	112 x 4 bits				
Number of I/O port lines	21 lines (including one input line)				Including 8 N-ch open drain lines
External interrupt	1				With sensor input
Analog input	8-bit A/D convertor (4 channels)				Also used as port pins
Timer	3 timers				
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on/Powerdown reset	Provided				
System clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	
Instruction execution time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby function	Provided				STOP,HALT
Power supply	2.7 to 5.5 V				5 V ± 10 % for A/D converter
Package	28-pin shrink DIP 28-pin SOP				
One time PROM product	μPD17P136A	μAD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output

*: Under development

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES
4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P132 is a one-time PROM version of the μPD17132, in which the internal mask ROM of the μPD17132 is replaced with a one-time PROM that can be written to just once.

Since a user program can be written on the PROM, this microcontroller is suited for trial manufacture during μPD17120, μPD17132 system development, or multiple device production.

The reader also should refer to the publications on the μPD17120 or μPD17132.

FEATURES

- Upward compatible with the μPD17120
- Pin compatible with the μPD17132 (except for PROM programming function)
- Internal one-time PROM: 1024 × 16 bits
- Supply voltage range: 2.7 to 5.5 V (When the power-on reset circuit is used)
  4.5 to 5.5 V (When the power-down reset function is used)

DIFFERENCES BETWEEN THE μPD17P132, μPD17120, AND μPD17132

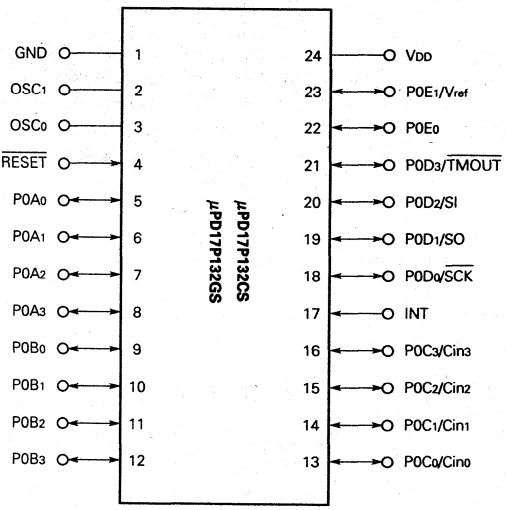
Item	μPD17P132	μPD17120	μPD17132
ROM	One-time PROM	Mask ROM	
	1024 × 16 bits (0000H-03FFH)	768 × 16 bits (0000H-02FFH)	1024 × 16 bits (0000H-03FFH)
RAM	111 × 4 bits	64 × 4 bits	111 × 4 bits
Pull-up resistors of P0D, P0E, and $\overline{\text{RESET}}$ pins	Not provided	Mask option	
V_{PP} pin and operation mode selection pins	Provided	Not provided	
Comparator	Provided	Not provided	Provided

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P132CS	24-pin plastic shrink DIP (300 mil)	Standard
μPD17P132GS	24-pin plastic SOP (300 mil)	Standard

PIN CONFIGURATION (Top View)

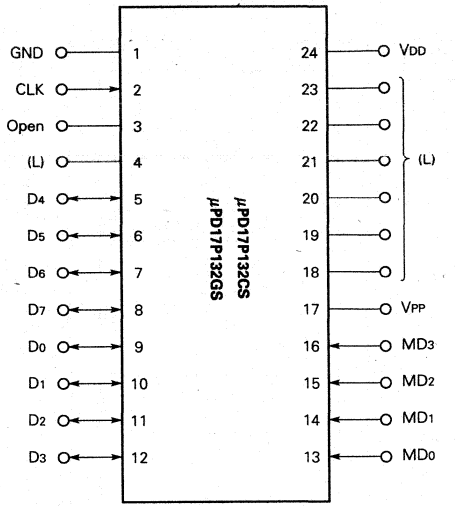
(1) Normal operating mode



24-pin plastic shrink DIP
24-pin plastic SOP

$\overline{\text{RESET}}$	:	Reset input
$\overline{\text{TMOUT}}$	:	Timer carry output
INT	:	External interrupt input
V_{ref}	:	External reference voltage input
Cin_0-Cin_3	:	Comparator input
SI	:	Serial data input
SO	:	Serial data output
$\overline{\text{SCK}}$	:	Serial clock input/output
OSC_0, OSC_1	:	System clock oscillation
$P0A_0$-$P0A_3$	:	Port 0A
$P0B_0$-$P0B_3$	:	Port 0B
$P0C_0$-$P0C_3$	:	Port 0C
$P0D_0$-$P0D_3$	:	Port 0D
$P0E_0$, $P0E_1$	:	Port 0E
CLK	:	Address update clock input
MD_0-MD_3	:	Operation mode selection input
D_0-D_7	:	Data input/output
V_{PP}	:	Programming power supply
V_{DD}	:	Positive power supply
GND	:	Ground

(2) Program memory write/verify



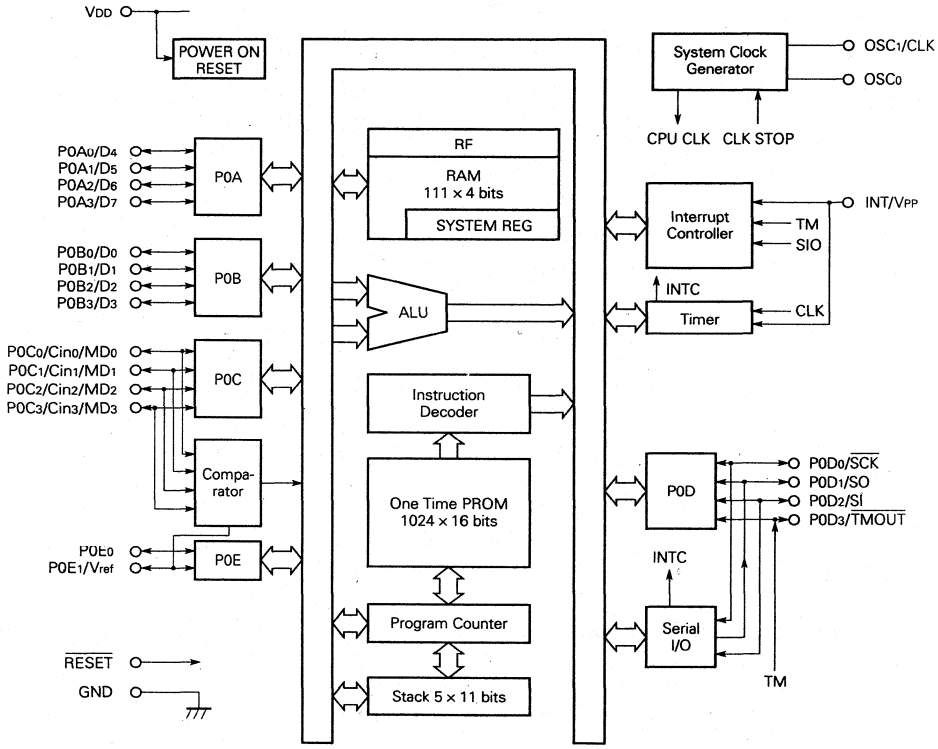
24-pin plastic shrink DIP
24-pin plastic SOP

Note Symbols in parentheses denote processing for pins not used in the program memory write/verify mode.

L : Connect these pins separately to the GND pin through pull-down resistors.

Open : Nothing should be connected on these pins.

BLOCK DIAGRAM



1. DIFFERENCES BETWEEN THE μPD17P132, μPD17120, AND μPD17132

The μPD17P132 is a one-time PROM version of the μPD17132, in which the internal mask ROM (program memory) is replaced with a one-time PROM.

Table 1-1 lists the differences between the μPD17P132, μPD17120, and μPD17132.

The μPD17P132 has the same CPU functions and internal peripheral hardware as the μPD17120 and μPD17132 except for the comparator function, ROM and RAM capacity, and whether a mask option can be specified. The μPD17P132 can be used for program evaluation in μPD17120, μPD17132 system development.

Table 1-1 Differences between the μPD17P132, μPD17120, and μPD17132

Item	μPD17P132	μPD17120	μPD17132
ROM	One-time PROM	Mask ROM	
	1024 × 16 bits (0000H-03FFH)	768 × 16 bits (0000H-02FFH)	1024 × 16 bits (0000H-03FFH)
RAM	111 × 4 bits	64 × 4 bits	111 × 4 bits
Pull-up resistors of P0D, P0E, and $\overline{\text{RESET}}$ pins	Not provided	Mask option	
V_{PP} pin and operation mode selection pins	Provided	Not provided	
Comparator	Provided	Not provided	Provided

2. PIN FUNCTIONS

2.1 NORMAL OPERATING MODE

PIN No.	PIN NAME	FUNCTION	OUTPUT	WHEN POWER-ON OR RESET
1	GND	Ground	–	–
2 3	OSC_1 OSC_0	For system clock oscillation. Resistor is connected from OSC_0 to OSC_1.	–	–
4	$\overline{RESET}$	System reset input pin	–	Input
5 to 8	$P0A_0$ to $P0A_3$	Port 0A · 4-bit input/output port · Input/output setting allowed in units of 1 bit	CMOS push-pull	Input (P0A)
9 to 12	$P0B_0$ to $P0B_3$	Port 0B · 4-bit input/output port · Input/output setting allowed in units of 4 bits	CMOS push-pull	Input (P0B)
13 to 16	$P0C_0/Cin_0$ to $P0C_3/Cin_3$	Port 0C. Analog voltage is supplied to the comparator through these pins. • $P0C_0$ - $P0C_3$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • Cin_0 - Cin_3 · Analog input for the comparator	COMS push-pull	Input (P0C)
17	INT	External interrupt request or sensor signal	–	–
18 19 20 21	$P0D_0/\overline{SCK}$ $P0D_1/SO$ $P0D_2/SI$ $P0D_3/\overline{TMOUT}$	Pin for port 0D, timer carry output, serial data input, serial data output, and serial clock input/output • $P0D_0$ - $P0D_3$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{SCK}$ · Serial clock input/output • SO · Serial data output • SI · Serial data input • $\overline{TMOUT}$ · Timer carry output	N-ch open drain	Input (P0D)
22 23	$P0E_0$ $P0E_1/V_{ref}$	Port 0E. Reference voltage is supplied to the comparator through these pins. • $P0E_0$ and $P0E_1$ · 2-bit input/output port · Input/output setting allowed in units of 1 bit • V_{ref} · Input of external reference voltage for the comparator	N-ch open drain	Input (P0E)
24	V_{DD}	Positive power supply	–	–

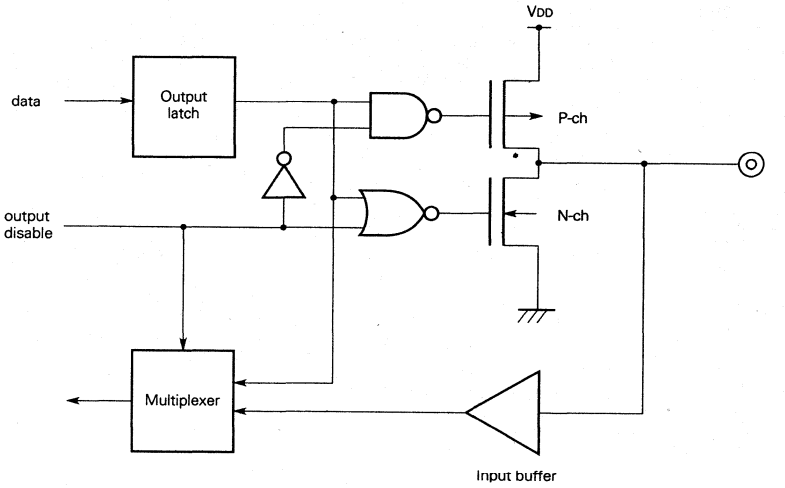
2.2 PROGRAM MEMORY WRITE/VERIFY MODE

PIN No.	PIN NAME	FUNCTION	INPUT/OUTPUT
1	GND	Ground	–
2	CLK	Input pin for address update clocks used when writing to program memory or verifying its contents	Input
5 to 8	D_4 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	I/O
9 to 12	D_0 to D_3		
13 to 16	MD_0 to MD_3	Input pins that select an operation mode when writing to program memory or verifying its contents	Input
17	V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.	–
24	V_{DD}	Positive power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.	–

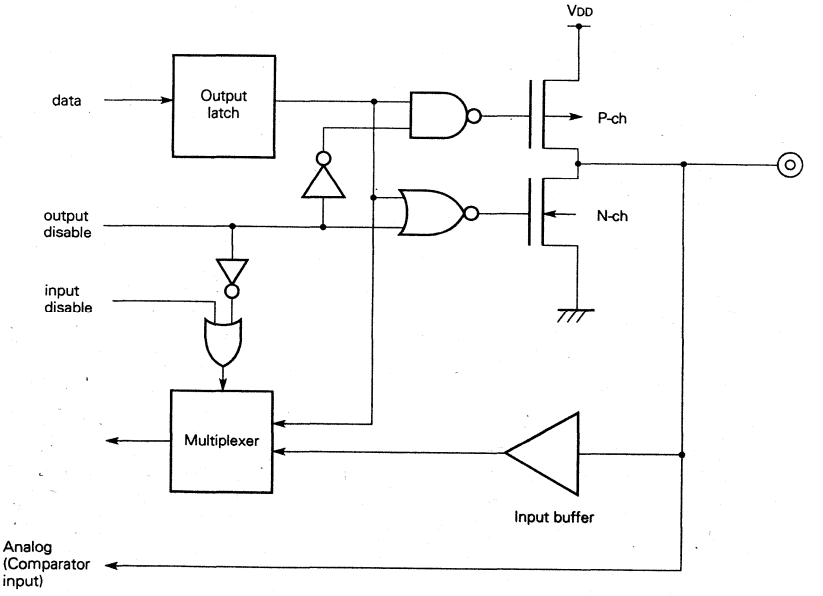
2.3 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

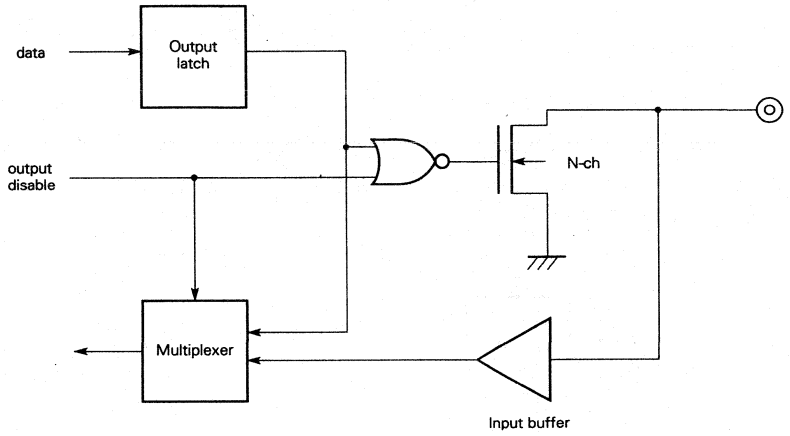
(1) P0A0 to P0A3, P0B0 to P0B3



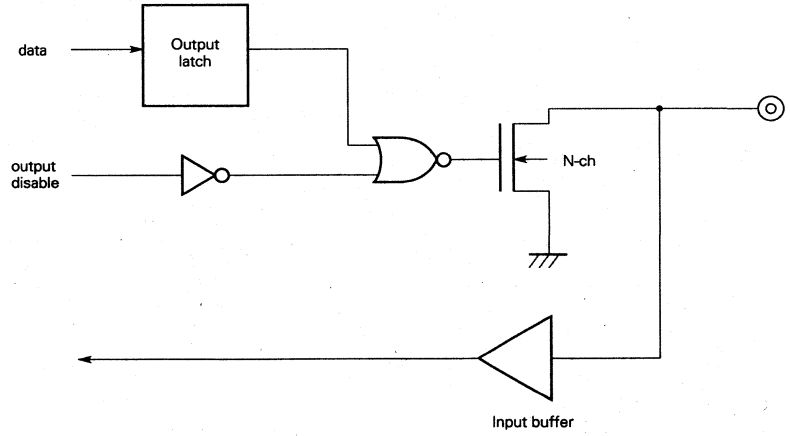
(2) P0C0/Cin0 to P0C3/Cin3



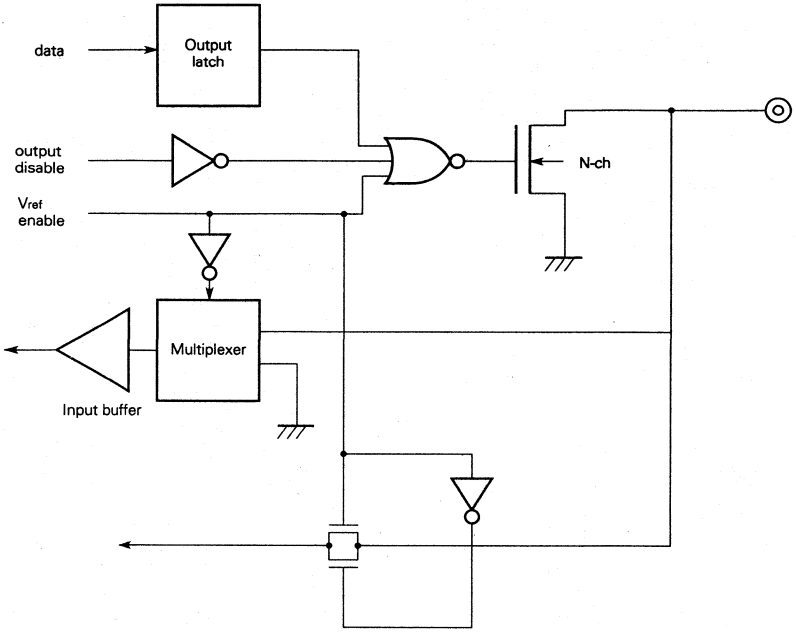
(3) $P0D_0$ to $P0D_3$



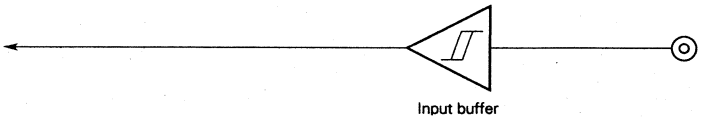
(4) $P0E_0$



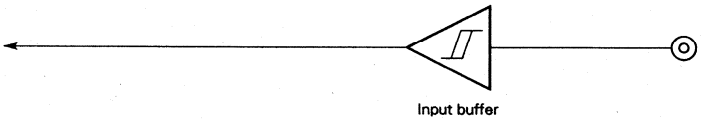
(5) POE1/Vref



(6) INT



(7) $\overline{\text{RESET}}$



3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P132's internal program memory consists of a 1024 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used when Writing to Program Memory or Verifying its Contents

Pin name	Function
V_{PP}	Voltage (+12.5 V) is applied to this pin when writing to program memory or verifying its contents.
V_{DD}	Positive power supply pin. +6 V is applied to this pin when writing to program memory or verifying its contents.
CLK	Input pin for address update clocks used when writing to program memory or verifying its contents. Input of four pulses to this pin updates the address of the program memory.
MD_0 - MD_3	Input pins that select an operation mode when writing to program memory or verifying its contents
D_0 - D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P132 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins (including the $\overline{RESET}$ pin) to GND level by means of pull-down resistors.

Table 3-2 Specification of Operating Modes

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory adress clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

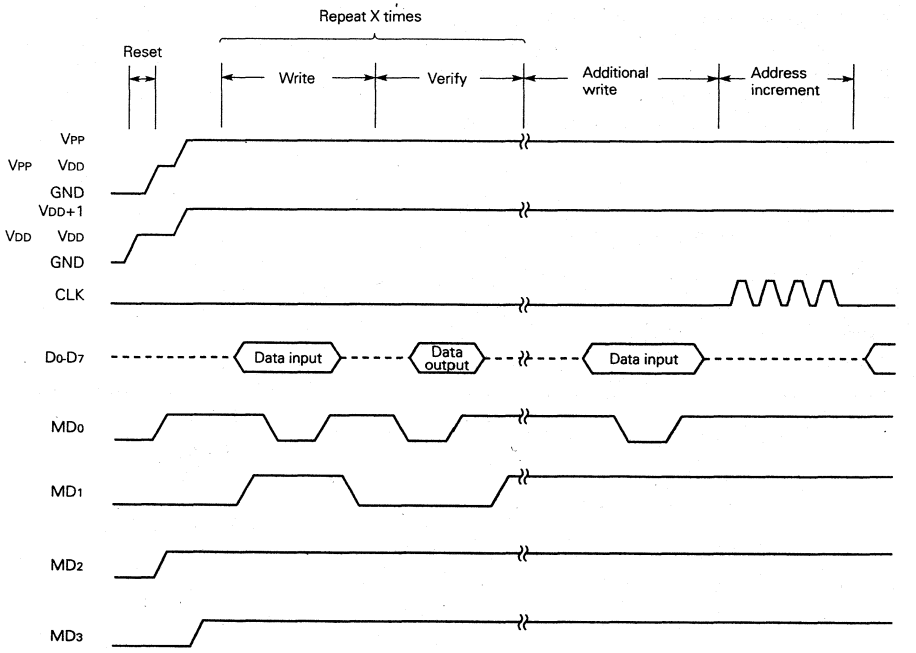
Remark ×: Don't care. L (low) or H (high)

3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for X (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the CLK pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

A timing chart for program memory writing steps (2) to (12) is shown below.

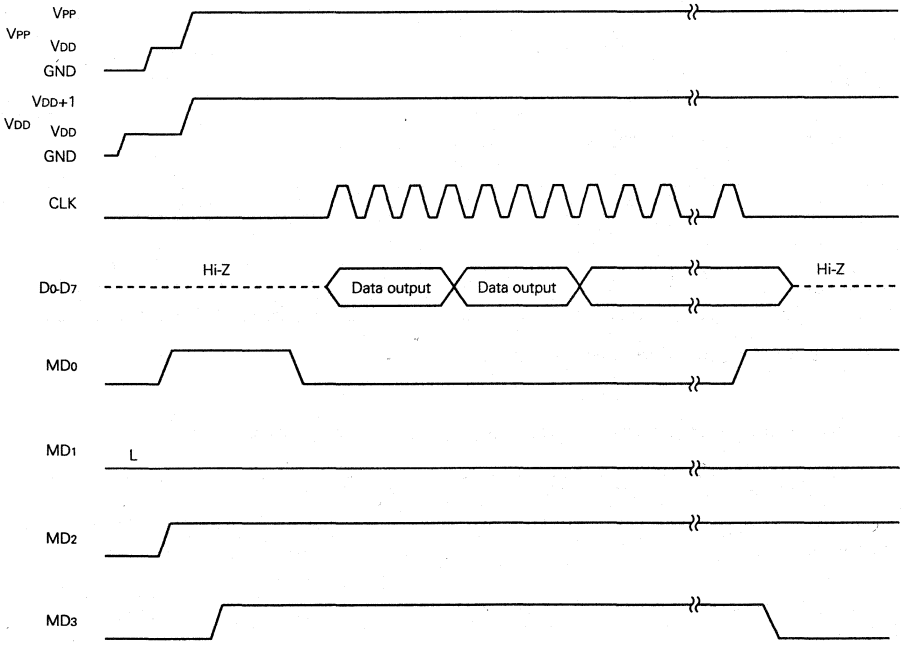


Remark The dashed line indicates high-impedance.

3.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for every 4 input clock pulses on the CLK.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

A timing chart for program memory reading steps (2) to (9) is shown below.



4. ELECTRICAL CHARACTERISTICS (TARGET)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, INT, $\overline{RESET}$	−0.3 to V_{DD} + 0.3	V
		P0D, P0E	−0.3 to +10.0	V
Output Voltage	V_O	P0A, P0B, P0C, INT, $\overline{RESET}$	−0.3 to V_{DD} + 0.3	V
		P0D, P0E	−0.3 to +10.0	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, and P0C	−5	mA
		Total of all output pins	−20	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, and P0C	5	mA
		Each of P0D and P0E	30	mA
		Total of P0A, P0B, and P0C output pins	20	mA
		Total of P0D and P0E output pins	60	mA
		Total of all output pins	80	mA
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C

RECOMMENDED POWER VOLTAGE RANGE (T_a = −40 to +85 °C)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITION
CPU*	2.7		5.5	V	
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (V_{DD} = 0 → 2.7 V): 4096 × 16/f_{CC} or less (f_{CC} = 400 kHz to 2.4 MHz)

* Excluding the power-on/power-down reset circuit

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
System Clock Oscillation Frequency	f_{CC}	1.6	2	2.4	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 9.1 kΩ
		0.8	1	1.2	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 22 kΩ
		0.6	1	1.2	MHz	V_{DD} = 2.7 to 5.5 V, R_{OSC} = 22 kΩ
		400	500	600	kHz	V_{DD} = 2.7 to 3.3 V, R_{OSC} = 47 kΩ

DC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P0D, P0E	
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $\overline{SCK}$, SI, INT	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C	
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P0E, $\overline{RESET}$, $\overline{SCK}$, SI, INT	
High-Level Output Current	I_{OH}	−1.0			mA	P0A, P0B, P0C $V_{DD} - V_{OH}$ = 0.3 V	V_{DD} = 4.5 to 5.5 V
		−0.5			mA		V_{DD} = 2.7 to 4.5 V
Low-Level Output Current	I_{OL}	1.0			mA	P0A, P0B, P0C V_{OL} = 0.3 V	V_{DD} = 4.5 to 5.5 V
		0.5			mA		V_{DD} = 2.7 to 4.5 V
Low-Level Output Voltage	V_{OL}			1.0	V	P0D, P0E I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V
				2.0	V		V_{DD} = 2.7 to 4.5 V
High-Level Input Leakage Current	I_{LIH}			3	μA	P0A, P0B, P0C, P0D, P0E V_{IN} = V_{DD}	
Low-Level Input Leakage Current	I_{LIL}			−3	μA	P0A, P0B, P0C, P0D, P0E V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH}			3	μA	P0A, P0B, P0C, P0D, P0E V_{OUT} = V_{DD}	
Low-Level Output Leakage Current	I_{LOL}			−3	μA	P0A, P0B, P0C, P0D, P0E V_{OUT} = 0 V	
Power Supply Current *Note*	I_{DD1}	Undefined				Operation mode, f_{CC} = 2.0 MHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
						f_{CC} = 1.0 MHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
						f_{CC} = 455 kHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
	I_{DD2}					HALT mode, f_{CC} = 2.0 MHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
						f_{CC} = 1.0 MHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
						f_{CC} = 455 kHz	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %
	I_{DD3}					STOP mode	V_{DD} = 5 V ± 10 %
							V_{DD} = 3 V ± 10 %

Note This current excludes the current which flows through the comparator.

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

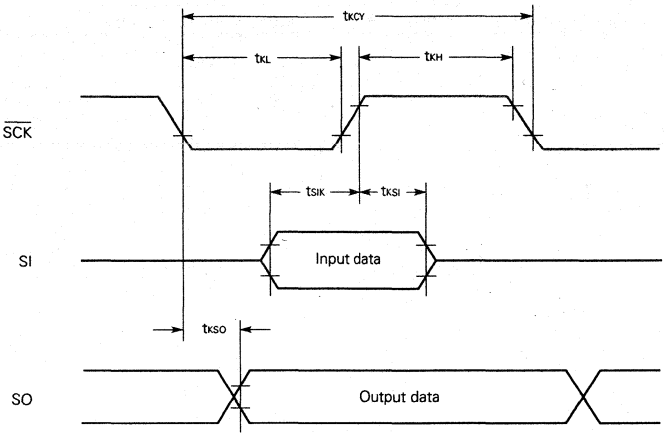
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Internal Clock Cycle Time	t_{CY}	6.6		41	μs		
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		16			μs		Output
		10			μs		Input
		32			μs		Output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		$t_{KCY}/2-6$			μs		Output
		5.0			μs		Input
		$t_{KCY}/2-12$			μs		Output
SI Setup Time (With Respect to $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI Hold Time (With Respect to $\overline{SCK}$↑)	t_{KSI}	100			ns		
SO Output Delay Time (With Respect to $\overline{SCK}$↓)	t_{KSO}			4.5	μs		
INT Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		

Remark t_{CY} = 16/f_{CC} (f_{CC}: frequency of system clock oscillator)

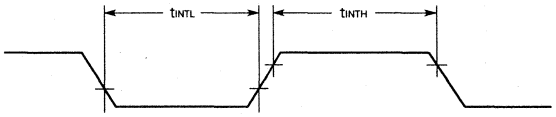
POWER-ON/POWER-DOWN RESET CIRCUIT CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Voltage Rise Time When Power-On Reset is Valid	t_{POR}			4096 × 16/fcc	s	V_{DD} = 0 → 2.7 V Rising must start at 0 V.
Voltage for Power-Down Reset Circuit	V_{PDR}		3.5	4.5	V	When PDRESEN = 1

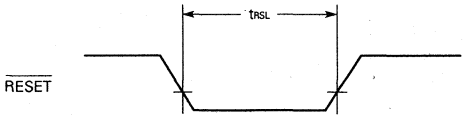
Serial transfer timing



Interrupt input timing



$\overline{\text{RESET}}$ input timing



COMPARATOR CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Comparator Input Voltage Range	V_{AIN}	0		V_{DD}	V	Cin_0 - Cin_3, V_{ref}
Resolution			10	50	mV	V_{DD} = 4.5 to 5.5 V
				100		
Response Time				32/f_{CC}	s	Time required for storing the comparison result in CMPFLG after execution of the comparator start instruction (execution time not included). (16 μs, when f_{CC} = 2 MHz)

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CLK
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	CLK
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

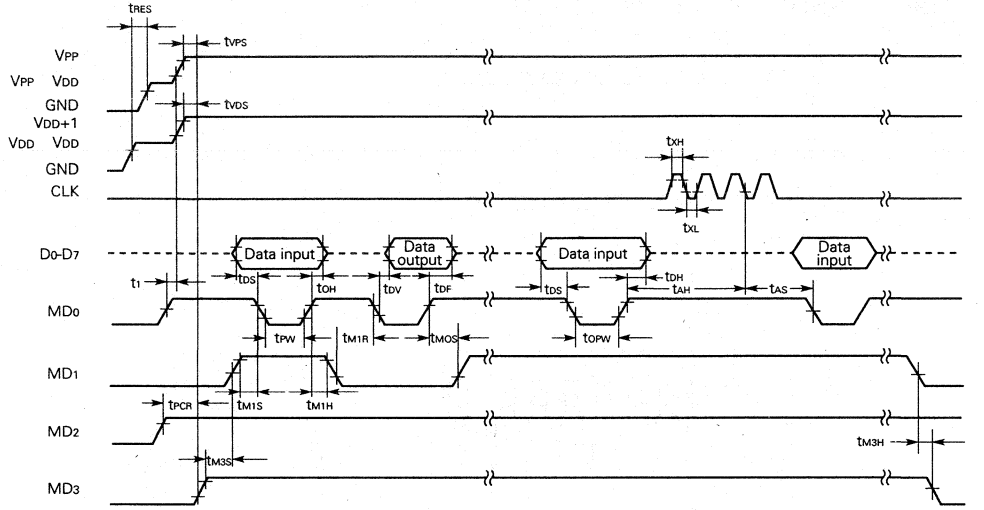
2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

AC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	Note 1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Setup Time Note 2 to MD0↓	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time Note 2 to MD0↑	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold time to MD0↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High, Low Level Range	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			2	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time from Address Note 2	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time from Address Note 2	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time from MD3↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

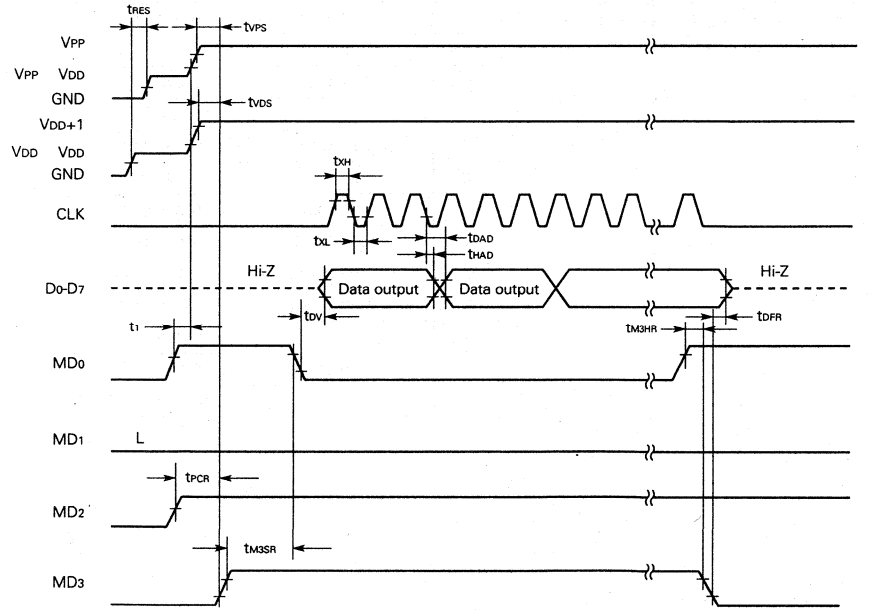
Note 1. Symbols for corresponding μPD27C256A.
2. Internal address signal is incremented by one at the falling edge of the third CLK input.

Write program memory timing



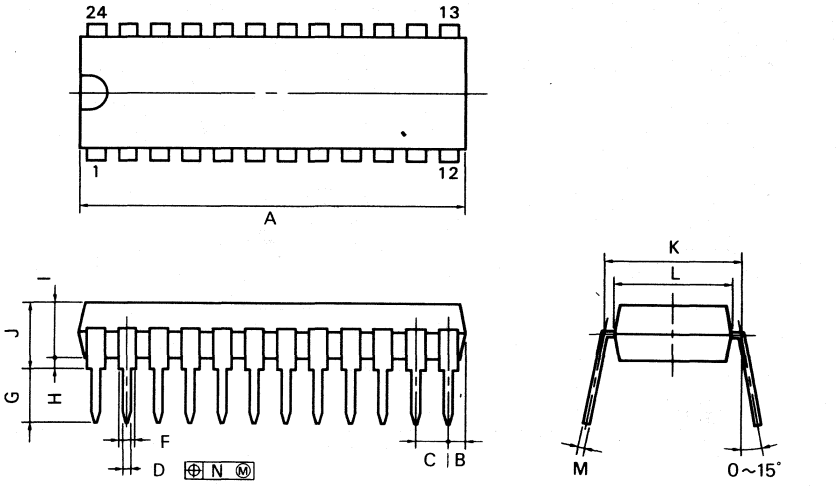
Remark The dashed line indicates high-impedance.

Read program memory timing



5. PACKAGE DIMENSIONS

24PIN PLASTIC SHRINK DIP (300 mil)



S24C-70-300B

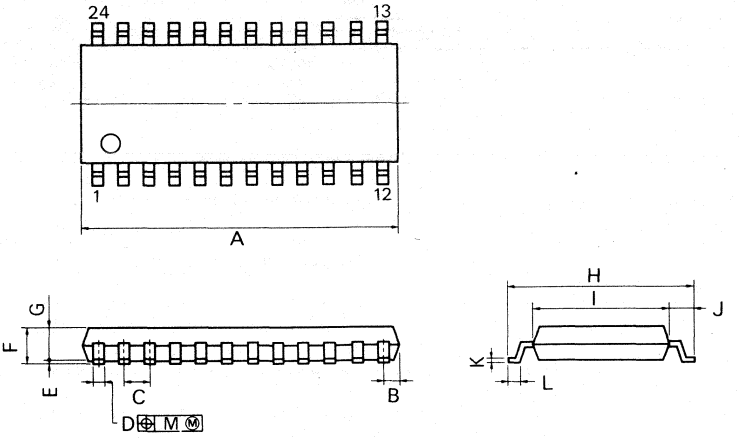
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (300 mil)



P24GM-50-300B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

APPENDIX A MICROCONTROLLER FUNCTIONS FOR SMALL HOME ELECTRIC APPLIANCES

ITEM	μPD17120[Note]	μPD17121[Note]	μPD17132[Note]	μPD17133[Note]	μPD17P132[Note]	μPD17P133[Note]
ROM Size	768 × 16 bits (Mask ROM)		1024 × 16 bits (Mask ROM)		1024 × 16 bits (One-time PROM)	
RAM Size	64 × 4 bits		111 × 4 bits			
Number of I/O Port Lines	18 lines (including 6 N-ch open drain lines)					
External Input	1 (with sensor input)					
Analog Input	None		Comparator (4 channels)			
Timer	1 (with 8-bit modulo register)					
Serial Interface	1 channel					
Stack	5 levels (including a level for an interrupt)					
System Clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation
Instruction Execution Time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz
Standby Function	Provided (HALT/STOP)					
Power-On/Power-Down Reset	Provided					
Supply Voltage Range	When the power-on reset circuit is used: 2.7 to 5.5 V When the power-down reset function is used: 4.5 to 5.5 V					
Package	24-pin plastic shrink DIP (300 mil) 24-pin plastic SOP (300 mil)					
One Time PROM Product	μPD17P132	μPD17P133	μPD17P132	μPD17P133	–	–

I/O: Input/output

Note Under development

Remark The comparator can be used as a 4-bit A/D converter by software.

ITEM	μPD17134A	μPD17135A	μPD17136A	μPD17137A	μPD17P136A[Note]	μPD17P137A[Note]
ROM Size	1024 × 16 bits (Mask ROM)		2048 × 16 bits (Mask ROM)		2048 × 16 bits (One-time PROM)	
RAM Size	112 × 4 bits					
Number of I/O Port Lines	21 lines (including 1 input line and 8 N-ch open drain lines)					
External Input	1 (with sensor input)					
Analog Input	8-bit A/D converter (4 channels)					
Timer	3 (2 timers with 8-bit modulo register and 1 basic interval timer)					
Serial Interface	1 channel					
Stack	5 levels (including three levels for an interrupt)					
System Clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation
Instruction Execution Time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz
Standby Function	Provided (HALT/STOP)					
Power-On/Power-Down Reset	Provided					
Supply Voltage Range	When the power-on reset circuit is used: 2.7 to 5.5 V When the power-down reset function is used: 4.5 to 5.5 V					
Package	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)					
One Time PROM Product	μPD17P136	μPD17P137	μPD17P136	μPD17P137	–	–

I/O: Input/output

Note Under development

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES 4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17134A is a 4-bit single-chip microcontroller containing an 8-bit A/D converter (4 channels), 3 times, an AC zerocross detector, a power-on reset circuit, and a serial interface.

For the CPU, the μPD17134A employs a 17K architecture using general registers. The new architecture allows operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (1 word) long, allowing programming to be done efficiently.

Since the μPD17134A has on-chip A/D converters and an AC zerocross detector, it is suitable for electronic control of electric home appliances. The μPD17P136A, a one-time PROM product (can be written to only once) is available for evaluation of the μPD17134A and μPD17136A and for small-scale production.

FEATURES

- 17 K architecture : General registers
- Program memory (ROM) : 1024 × 16 bits
- Data memory (RAM) : 112 × 4 bits
- Instruction execution time : 8 μs
  (at 2 MHz: RC oscillation(Note))
- 8-bit A/D convertor : 4 channels
  Absolute accuracy: ±1.5 LSB or lower (V_{DD} = 5 V ±10 %)
- Timer function : 3 channels
- 3-wire serial interface : 1 channel
- Input/output pins : 22 pins (including 1 general input pin and 1 sensor input pin)
- Power-on/power-down reset circuit
- Operates on low voltage : V_{DD} = 2.7 to 5.5 V

Note The capacitor for RC oscillation is contained in the μPD17134A.

ORDERING INFORMATION

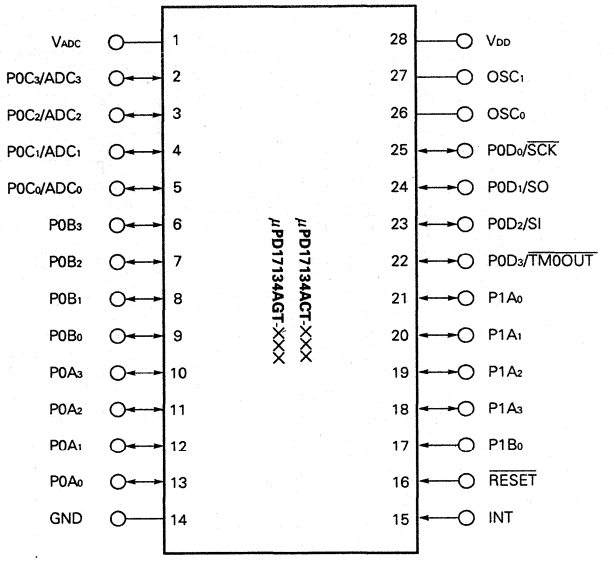
Order Code	Package	Quality Grade
μPD17134ACT-×××	28-pin plastic shrink DIP (400 mil)	Standard
μPD17134AGT-×××	28-pin plastic SOP (375 mil)	Standard

FUNCTION OF μPD17134A

Item	Description
ROM	1024 × 16 bits
RAM	112 × 4 bits (The stack is separated from data memory.)
Stack	5 address stacks, 3 interrupt stacks
Number of I/O ports	22 { • 20 I/O ports • 1 general input port • 1 input port for sensing an interrupt or AC zero cross
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ±1.5 LSB or less at a power voltage of 5 V ±10 %
Timer	3 channels { • 2 channels for 8-bit timers (They can be used together as one 16-bit timer) • 1 channel for a 7-bit basic interval timer (can be used as a watchdog timer)
Serial interface	1 channel (3-wire type)
Interrupt	• Up to 3 levels of multiple hardware interrupts • 1 external interrupt { • Shared with the input from the AC zero-cross detection circuit • Rising-edge detection, falling-edge detection • Detection of the rising edge, falling edge, or both edes can be selected. • With the sense input • 4 internal interrupts { • Timer 0 • Timer 1 • Basic interval timer • Serial interface
Execution time of an instruction	8 μs at 2 MHz clock, RC oscillation
Standby function	STOP/HALT
Operating power voltage	• 2.7 to 5.5 V • 4.5 to 5.5 V (when the power-on/power-down reset functions are used)
Package	• 28-pin plastic shrink DIP • 28-pin plastic SOP
One-time PROM	μPD17P136A

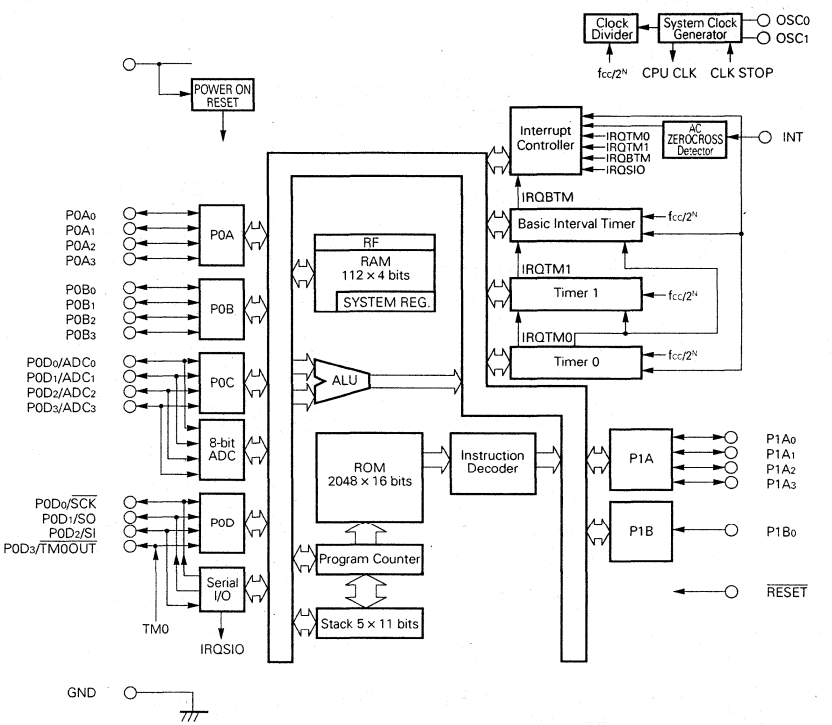
PIN CONFIGURATION (Top View)

28-pin plastic shrink DIP
28-pin plastic SOP



ADC0 - ADC3	:	Analog input for the A/D converter
RESET	:	Reset input
TM0OUT	:	Timer 0 carry output
INT	:	External interrupt input
SI	:	Serial data input
SO	:	Serial data output
SCK	:	Serial clock input/output
OSC0 - OSC1	:	System clock oscillation
P0A0 - P0A3	:	Port 0A
P0B0 - P0B3	:	Port 0B
P0C0 - P0C3	:	Port 0C
P0D0 - P0D3	:	Port 0D
P1A0 - P1A3	:	Port 1A
P1B0	:	Port 1B
VADC	:	Analog power supply
VDD	:	Power supply
GND	:	Ground

BLOCK DIAGRAM



1. PINS

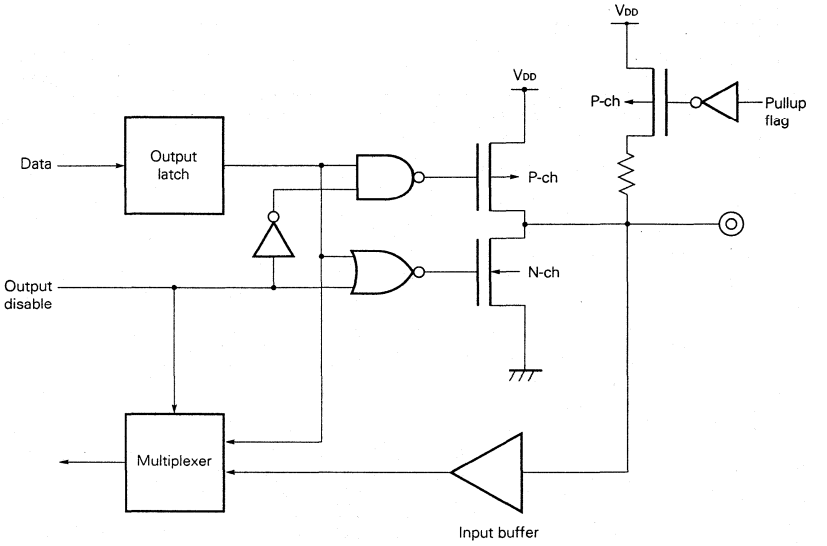
1.1 PIN FUNCTIONS

PIN No.	PIN NAME	FUNCTION	OUTPUT	AFTER POWER-ON OR RESET
1	V_{ADC}	Power voltage for the A/D converter and for the circuit generating reference voltage	–	Input
2 to 5	$P0C_3/ADC_3$ to $P0C_0/ADC_0$	Pin for port 0C and A/D converter • $P0C_3$ to $P0C_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • ADC_3 to ADC_0 · Analog input for the A/D converter	CMOS push-pull	Input (P0C)
6 to 9	$P0B_3$ to $P0B_0$	Port 0B · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
10 to 13	$P0A_3$ to $P0A_0$	Port 0A · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
14	GND	Ground	–	–
15	INT	Input of external interrupt requests and release of standby mode	–	Input
16	$\overline{RESET}$	System reset input pin	–	Input
17	$P1B_0$	Port 1B · 1-bit input/output port · Pull-up resistor incorporation specifiable by mask option	–	Input
18 to 21	$P1A_3$ to $P1A_0$	Port 1A · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input
22	$P0D_3/\overline{TM0OUT}$	Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input/output. • $P0D_3$ to $P0D_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{TM0OUT}$ · Timer 0 carry output	N-ch open-drain	Input
23	$P0D_2/SI$	• SI · Serial data input		
24	$P0D_1/SO$	• SO · Serial data output		
25	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ · Serial clock input/output		
26 27	OSC_0 OSC_1	For system clock oscillation. Resistor is connected from OSC_0 to OSC_1.	–	–
28	V_{DD}	Power supply	–	–

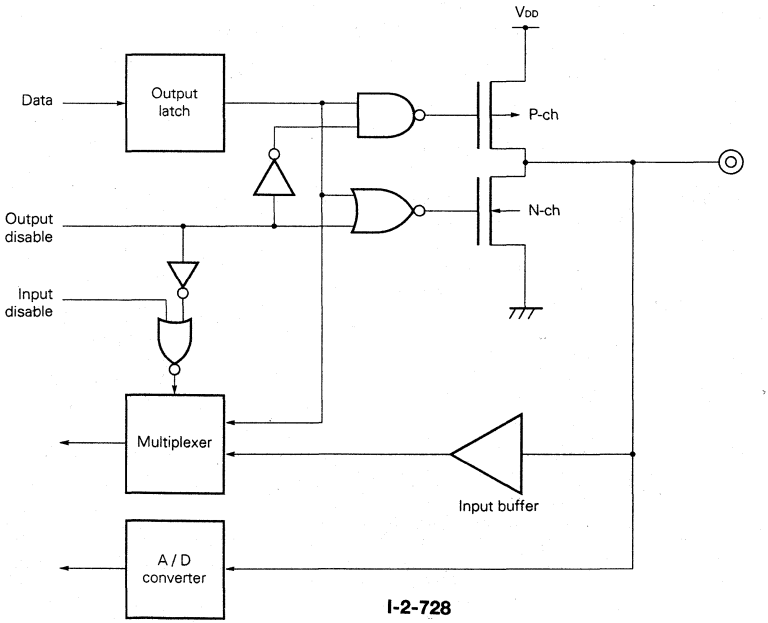
1.2 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

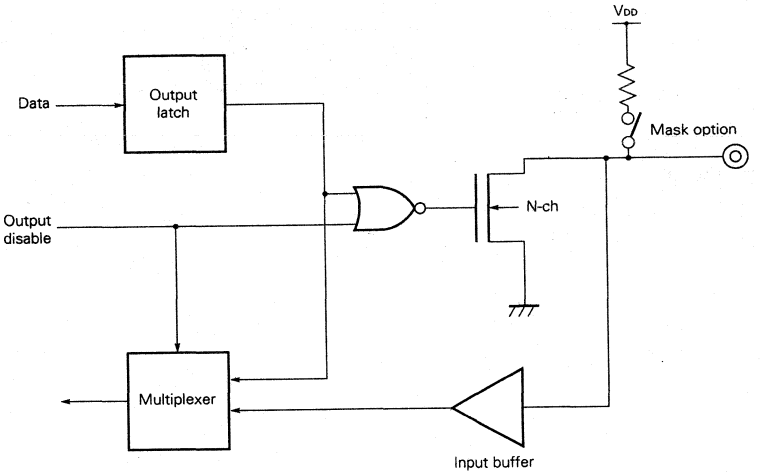
(1) P0A0 to P0A3, P0B0 to P0B3



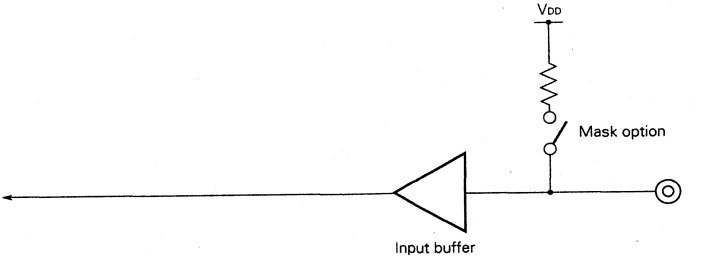
(2) P0C0/ADC0 to P0C3/ADC3



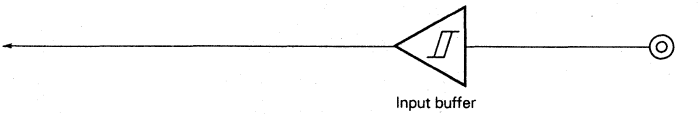
(3) $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$



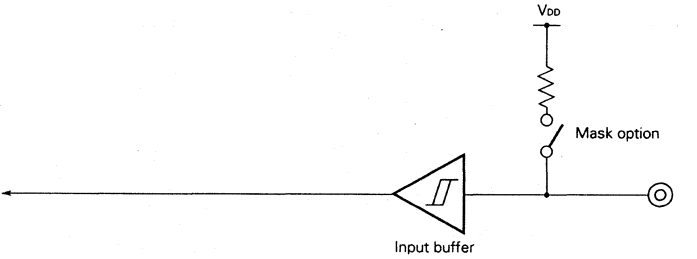
(4) $P1B_0$



(5) INT



(6) $\overline{\text{RESET}}$



26. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) shall be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 26-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17134ACT-xxx	28-pin plastic shrink DIP (400 mil)	• Wave soldering • Partial heating method
μPD17134AGT-xxx	28-pin plastic SOP (375 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 26-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow processes: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow processes: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow processes: 1
Partial heating method	Terminal to be heated	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

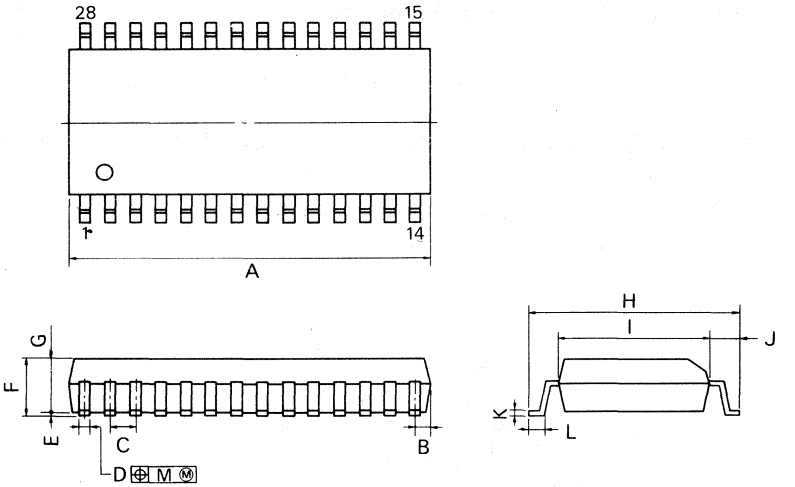
Remark For details of the recommended soldering conditions, refer to our document **"SMT MANUAL" (IEI-1207).**

25. MICROCONTROLLER FUNCTIONS FOR SMALL HOME ELECTRIC APPLIANCES

Item	μPD17134A	μPD17135A	μPD17136A	μPD17137A	Remarks
ROM Size	1024 × 16 bits		2048 × 16 bits		
RAM Size	112 × 4 bits				
Number of I/O Port Lines	22 lines (including one input line and one sense input line)				Including 8 N-ch open drain lines
A/D Converter Input	4 channels				Also used as port pins
Timer	3 timers				8 bits: 2 channels, 7 bits: 1 channel (Basic interval timers)
Serial Interface	1 channel				Also used as port pin
Stack	5 levels				
Power-On/Power-Down Reset	Provided (valid only when V_{DD} = 5 V ±10 %)				
System Clock	RC oscillation	Ceramic/crystal oscillation	RC oscillation	Ceramic/crystal oscillation	
Instruction Execution Time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby Function	Provided				STOP/HALT
Power Supply	2.7 to 5.5 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
One Time PROM Product	μPD17P136A	μPD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

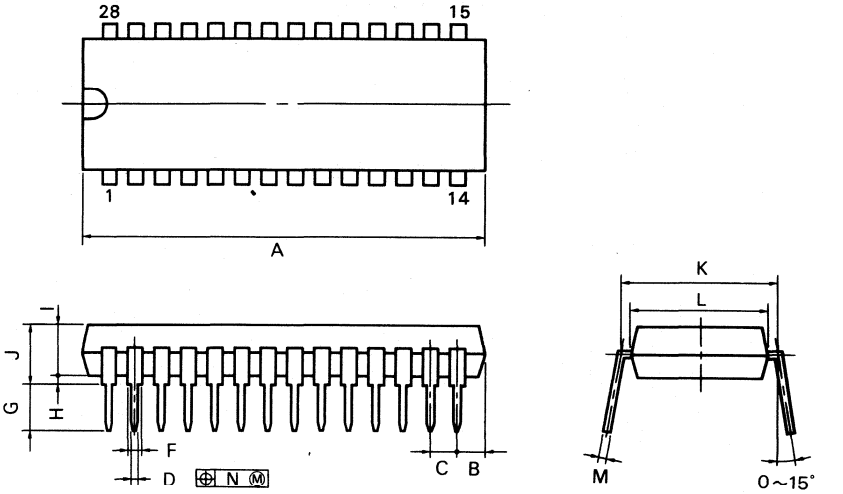
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

24. PACKAGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

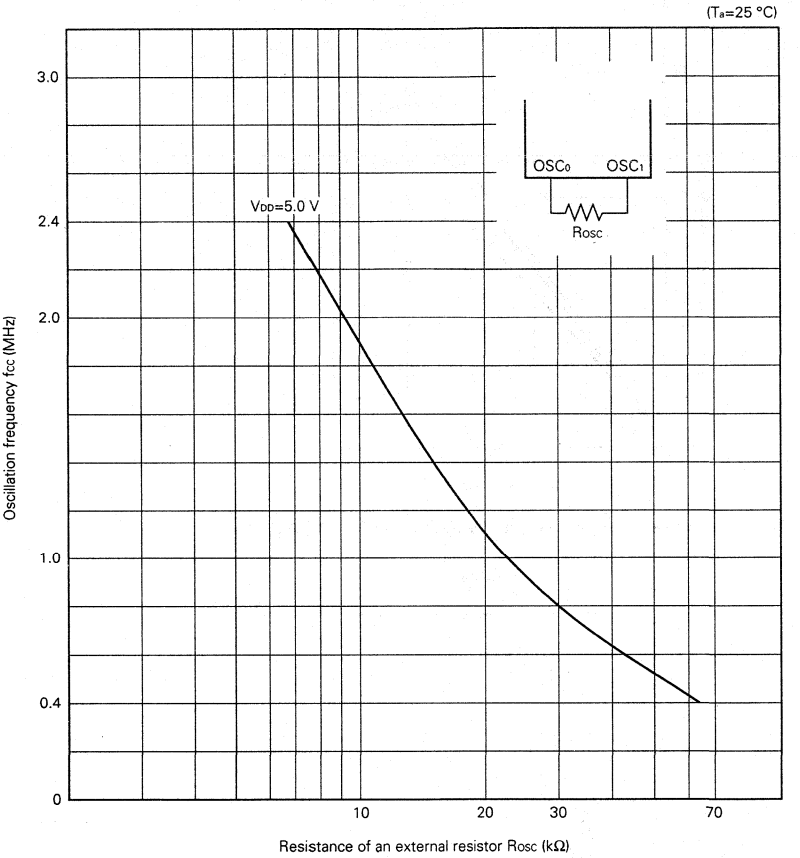
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

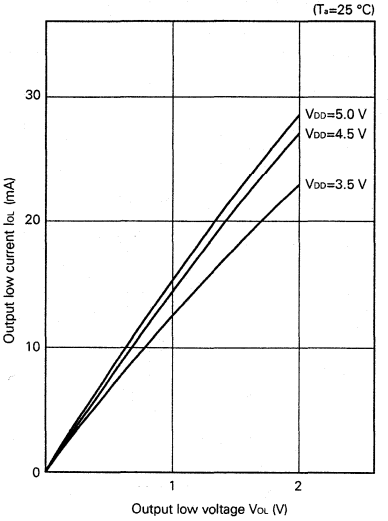
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

fcc vs Rosc

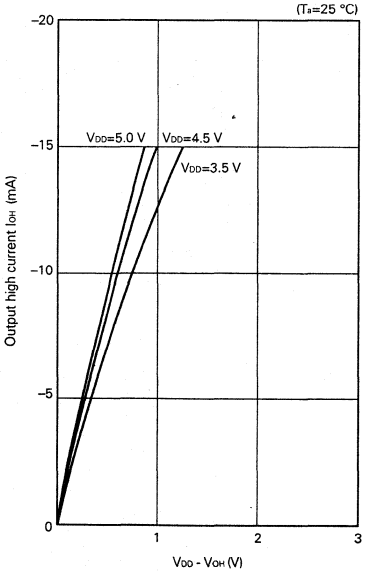

(Ta=25 °C)
3.0
2.4
2.0
1.0
0.4
0
Oscillation frequency fcc (MHz)
VDD=5.0 V
OSC0
OSC1
Rosc
10
20
30
70
Resistance of an external resistor Rosc (kΩ)

I_{OL} vs V_{OL} (P0D, P1A)



Note Absolute maximum rating of output current is 30 mA per pin.

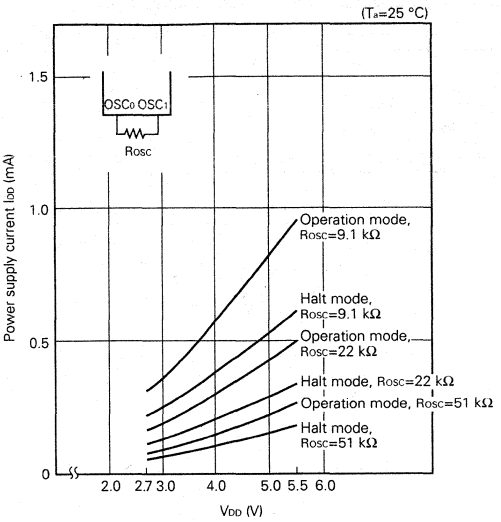
I_{OH} vs (V_{DD} - V_{OH})



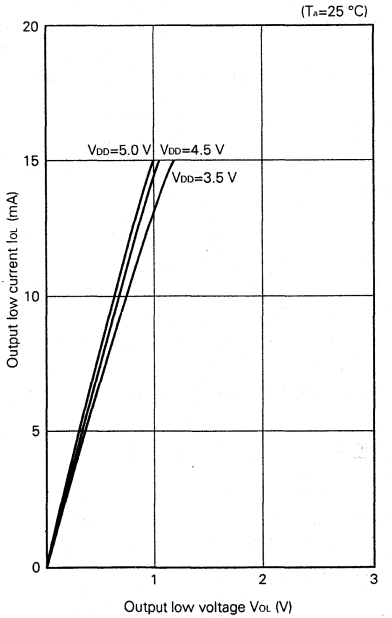
Note Absolute maximum rating of output current is –15 mA per pin.

23. CHARACTERISTIC CURVES (FOR REFERENCE)

I_{DD} vs V_{DD}



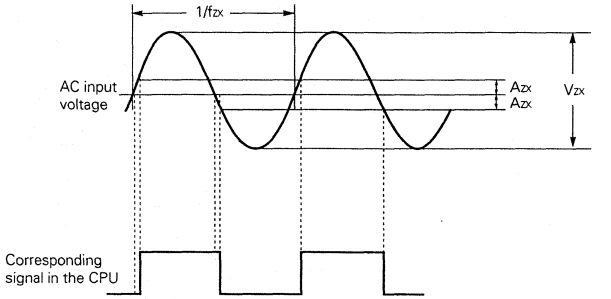
I_{OL} vs V_{OL} (P0A, P0B, P0C, P1B)



Note Absolute maximum rating of output current is 15 mA per pin.

ZEROCROSS DETECTION INPUT CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V_{P-P}	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	f_{ZX}	40	50 or 60	1000	Hz	
Zerocross Accuracy	A_{ZX}		40	±120	mV	50 Hz/60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by A_{ZX} in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C, V_{ADC} = V_{DD} ±0.5 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		8	8	8	bit	
Absolute Accuracy Note 1				±1.5	LSB	V_{ADC} = V_{DD}
ADC Circuit Current	I_{ADC}		1.5	2.0	mA	
Conversion Time Note 2	t_{CONV}			400/fx	s	

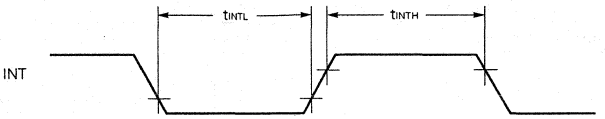
Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at f_{CC} = 2 MHz, 200 μs)

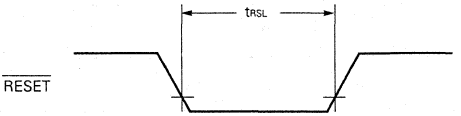
CHARACTERISTICS OF THE POWER-ON AND POWER-DOWN RESET CIRCUITS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Time it Take for the Power to Rise to the Voltage Level that Enables Power-On Reset	t_{POR}			8192 × 16/f_{CC}	s	The power voltage (V_{DD}) must change from ground level to 2.7 V.
Low Voltage to be Detected by the Power-Down Reset Circuit	V_{PDR}		3.5	4.5	V	When PDRESEN = 1

Interrupt input timing



$\overline{\text{RESET}}$ input timing

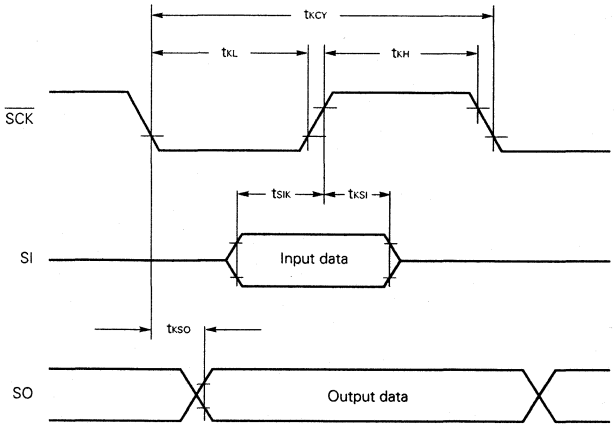


AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Internal Clock Cycle Time	t_{CY}	6.6		41	μs	V_{DD} = 4.5 to 5.5 V	
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		16			μs		Output
		10			μs		Input
		32			μs		Output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		t_{KCY}/2−6			μs		Output
		5.0			μs		Input
		t_{KCY}/2−12			μs		Output
SI Setup Time (Referred to $\overline{SCK}$ ↑)	t_{SIK}	100			ns		
SI Hold Time (Referred to $\overline{SCK}$ ↑)	t_{KSI}	100			ns		
SO Output Delay Time (Referred to $\overline{SCK}$ ↓)	t_{KSO}			4.5	μs		
Interrupt Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		

Remark t_{CY} = 16/f_{CC} (f_{CC}: frequency of system clock oscillator)

Serial transfer timing



CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION		
Power Supply Current [Note]	I_{DD1}		0.8	2.0	mA	Operation mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			0.5	1.5	mA			V_{DD} = 3 V ±10 %
			0.4	1.0	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.25	0.75	mA			V_{DD} = 3 V ±10 %
			250	500	μA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			125	375	μA			V_{DD} = 3 V ±10 %
	I_{DD2}		0.6	1.5	mA	HALT mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			0.3	1.0	mA			V_{DD} = 3 V ±10 %
			0.3	0.8	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.15	0.5	mA			V_{DD} = 3 V ±10 %
			150	300	μA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			100	200	μA			V_{DD} = 3 V ±10 %
	I_{DD3}		3.0	10	μA	STOP mode	V_{DD} = 5 V ±10 %	
			2.0	10	μA		V_{DD} = 3 V ±10 %	

Note When neither the A/D converter nor zerocross detection circuit is used, and excluding the current which flows through the built-in pull-up resistor

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0D, 01A	**Note 1**
				9			**Note 2**
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $\overline{SCK}$, SI, INT	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P1A, $\overline{RESET}$, $\overline{SCK}$, SI, INT	
High-Level Output Voltage	V_{OH}			V_{DD} −0.3	V	P0A, P0B, P0C **Note 3**	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1.0 mA
				V_{DD} −0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OH} = −0.5 mA
Low-Level Output Voltage	V_{OL1}			0.3	V	P0A, P0B, P0C, P0D, P1A **Note 3**	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA
				0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA
	V_{OL2}			1.0	V	P0D, P1A, I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V
				2.0	V		V_{DD} = 2.7 to 4.5 V
High-Level Input Leakage Current	I_{LIH1}			3	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	P0D, P1A, V_{IN} = 9 V **Note 2**	
Low-Level Input Leakage Current	I_{LIL}			−5	μA	P0A, P0B, P0C, P0D, 01A, P1B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			3	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	P0D, P1A, V_{OUT} = 9 V **Note 2**	
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = 0 V	
Built-In Pull-Up Resistor	R_{PULL}	50	100	200	kΩ	P0A, P0B, P1B, $\overline{RESET}$	

Note 1. When a built-in pull-up resistor is selected as mask option
2. When N-ch open-drain input/output is selected
3. When a built-in pull-up resistor is not selected by the software

22. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V		−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$, OSC_0, OSC_1		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} +0.3	
			Note 2	−0.3 to +11.0	
Output Voltage	V_O	P0A, P0B, P0C		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} +0.3	
			Note 2	−0.3 to +11.0	
High-Level Output Current	I_{OH}	Each of P0A, P0B, and P0C		−15	mA
		Total of all pins		−30	
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C and P1B		15	mA
		Each of P0D and P1A		30	
		Total of all pins		100	
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C		180	mW

RECOMMENDED POWER VOLTAGE RANGE (T_a = −40 to +85 °C)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITION
CPU **Note 3**	2.7		5.5	V	
A/D Converter		4.5		5.5	VAbsolute accuracy: ±1.5 LSB or less
Zerocross Detection Circuit	4.5		5.5	V	Zerocross accuracy: Azx = ±120 mV or less
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (V_{DD} = 0 → 2.7 V): 8192 × 16/f_{CC} or less

Note 1. When a built-in pull-up resistor is selected as mask option
2. When N-ch open-drain input/output is selected
3. Excluding the A/D converter, zerocross detection circuit, and power-on/power-down rest circuits

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
System Clock Oscillation Frequency	f_{CC}	1.6	2	2.4	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 9.1 kΩ
		0.8	1	1.2	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 22 kΩ
		0.6	1	1.2	MHz	V_{DD} = 2.7 to 5.5 V, R_{OSC} = 22 kΩ
		400	500	600	kHz	V_{DD} = 2.7 to 3.3 V R_{OSC} = 47 kΩ

1.3 HANDLING UNUSED PINS

To prevent malfunctions, connect the unused pins as follows:

Table 1-1 Handling Unused Pins

Pin			Handling
Port Note	Input mode	P0A, P0B, P0C, P0D, P1A, P1B0	To be connected to the V_{DD} or GND pin
	Output mode	P0A, P0B, P0C (CMOS port)	Open
		P0D, P1A (N-ch open-drain port)	Open (0s are output on the pins.)
INT			To be connected to the V_{DD} or GND pin
V_{ADC}			To be connected to the V_{DD} pin Note

Note 1. When a pull-up resister is not incorporated.

2. Connect the V_{ADC} pin to the V_{DD} pin even when the A/D converter is not used.

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES 4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17136A is a 4-bit single-chip microcontroller containing an 8-bit A/D converters (4 channels), 3 timers, an AC zerocross detector, a power-on reset circuit, and a serial interface.

For the CPU, the μPD17136A employs a 17K architecture using general registers. The new architecture allows operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (1 word) long, allowing programming to be done efficiently.

Since the μPD17136A has on-chip A/D converters and an AC zerocross detector, it is suitable for electronic control of electric home appliances. The μPD17P136A, a one-time PROM (can be written to only once) is available for evaluation of the μPD17134A and μPD17136A and for small-scale production.

FEATURES

- 17K architecture : General registers
- Program memory (ROM) : 2048 × 16 bits
- Data memory (RAM) : 112 × 4 bits
- Instruction execution time : 8 μs (at 2 MHz: RC oscillation)(Note)
- 8-bit A/D convertor : 4 channels
  Absolute accuracy: ±1.5 LSB or lower (V_{DD} = 5 V ±10 %)
- Timer function : 3 channels
- 3-wire serial interface : 1 channel
- Input/output pins : 22 pins (including 1 input pin and 1 sensor input pin)
- Power-on/power-down reset circuit
- Operates on low voltage : V_{DD} = 2.7 to 5.5 V

Note The capacitor for RC oscillation is contained in the μPD17136A.

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17136ACT-×××	28-pin plastic shrink DIP (400 mil)	Standard
μPD17136AGT-×××	28-pin plastic SOP (375 mil)	Standard

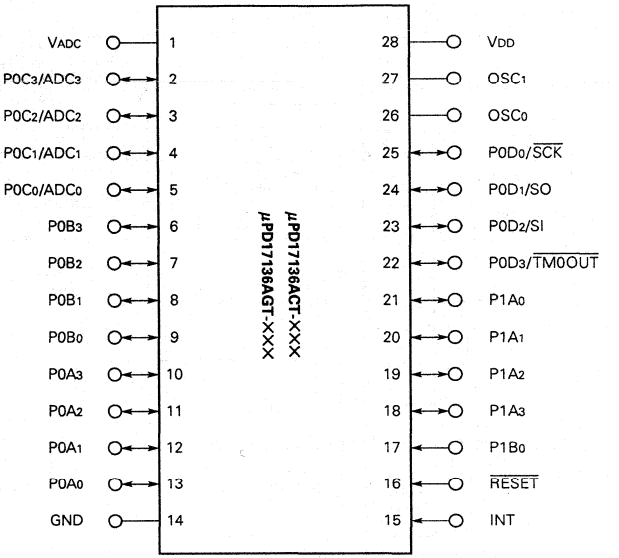
CHARACTERISTICS OF μPD17136A

Item	Description
ROM	2048 × 16 bits
RAM	112 × 4 bits (The stack is separate from data memory.)
Stack	5 address stacks, 3 interrupt stacks
Number of I/O ports	22 { • 20 I/O ports • 1 general input port • 1 input port for sensing an interrupt or AC zero-cross
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ±1.5 LSB or less at a power voltage of 5 V ±10 %
Timer	3 channels { 2 channels for 8-bit timers (They can be used together as one 16-bit timer.) 1 channel for a 7-bit basic interval timer (can be used as a watchdog timer.)
Serial interface	1 channel (3-wire type)
Interrupt	• Up to 3 levels of multiple hardware interrupts • 1 external interrupt { • Shared with the input from the AC zerocross detection circuit • Rising-edge detection, falling-edge detection • Detection of the rising edge, falling edge, or both edges can be selected. • With the sense input • 4 internal interrupts { • Timer 0 • Timer 1 • Basic interval timer • Serial interface
Execution time of an instruction	8 μs at 2 MHz clock, RC oscillation
Standby function	STOP/HALT
Operating power voltage	• 2.7 to 5.5 V • 4.5 to 5.5 V (when the power-on/power-down reset functions are used)
Package	• 28-pin plastic shrink DIP • 28-pin plastic SOP
One-time PROM	μPD17P136A

I/O: input/output

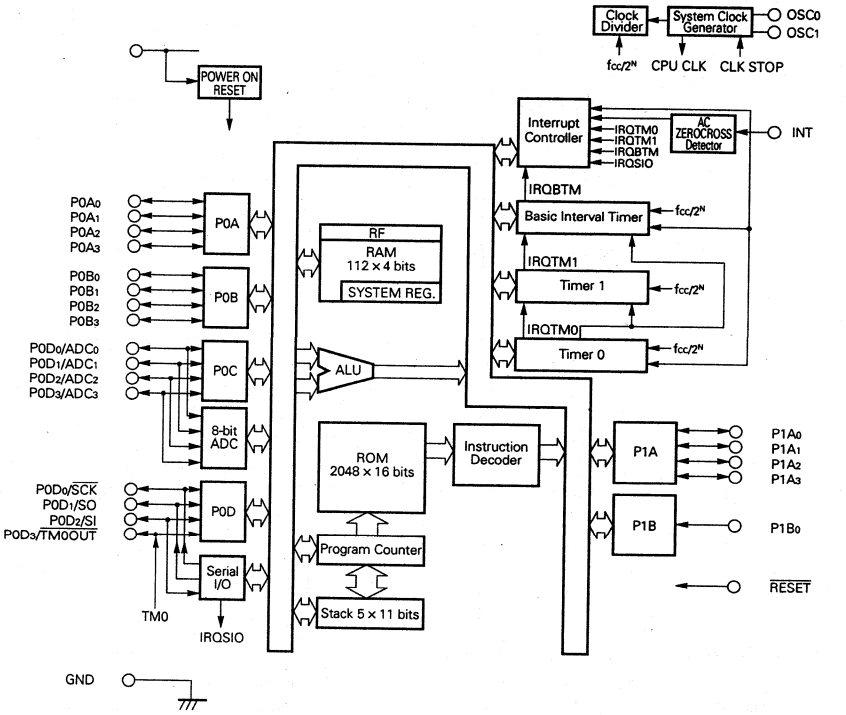
PIN CONFIGURATION (Top View)

28-pin plastic shrink DIP
28-pin plastic SOP



ADC0 - ADC3	:	Analog input for the A/D converter
RESET	:	Reset input
TM0OUT	:	Timer 0 carry output
INT	:	External interrupt input
SI	:	Serial data input
SO	:	Serial data output
SCK	:	Serial clock input/output
OSC0, OSC1	:	System clock oscillation
P0A0 - P0A3	:	Port 0A
P0B0 - P0B3	:	Port 0B
P0C0 - P0C3	:	Port 0C
P0D0 - P0D3	:	Port 0D
P1A0 - P1A3	:	Port 1A
P1B0	:	Port 1B
VADC	:	Analog power supply
VDD	:	Power supply
GND	:	Ground

BLOCK DIAGRAM



1. PINS

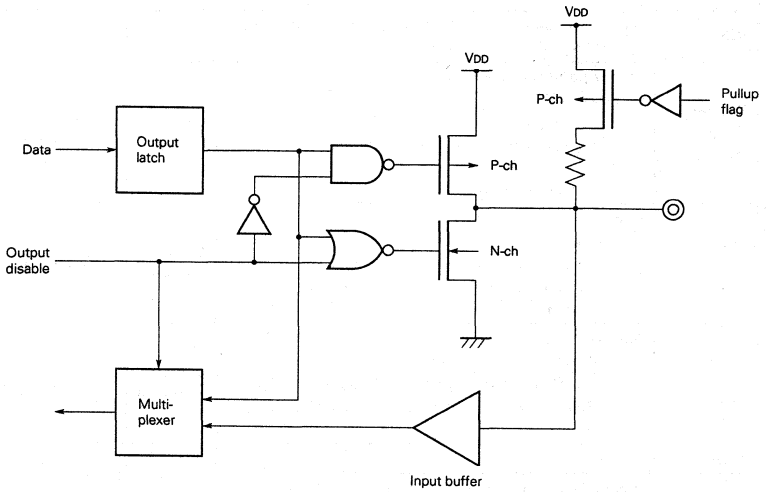
1.1 PIN FUNCTIONS

Pin No.	Pin name	Function	Output	After power-on or reset
1	V_{ADC}	Power voltage for the A/D converter and for the circuit generating reference voltage	–	–
2 to 5	$P0C_3/ADC_3$ to $P0C_0/ADC_0$	Pin for port 0C and A/D converter • $P0C_3$ to $P0C_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • ADC_3 to ADC_0 · Analog input for the A/D converter	CMOS push-pull	Input (P0C)
6 to 9	$P0B_3$ to $P0B_0$	Port 0B · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
10 to 13	$P0A_3$ to $P0A_0$	Port 0A · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
14	GND	Ground	–	–
15	INT	Input of external interrupt requests and release of standby mode	Input	Input
16	$\overline{RESET}$	System reset input pin	Input	Input
17	$P1B_0$	Port 1B · 1-bit input port · Pull-up resistor incorporation specifiable by mask option	Input	Input
18 to 21	$P1A_3$ to $P1A_0$	Port 1A · 4-bit input/output port · Input/output setting allowed in units of 4 bits · Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input
22	$P0D_3/\overline{TM0OUT}$	Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input/output. • $P0D_3$ - $P0D_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{TM0OUT}$ · Timer 0 carry output	N-ch open-drain	Input
23	$P0D_2/SI$	• SI · Serial data input		
24	$P0D_1/SO$	• SO · Serial data output		
25	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ · Serial clock input/output		
26 27	OSC_0 OSC_1	For system clock oscillation. Resistor is connected from $0SC_0$ to $0SC_1$.	–	–
28	V_{DD}	Power supply	–	–

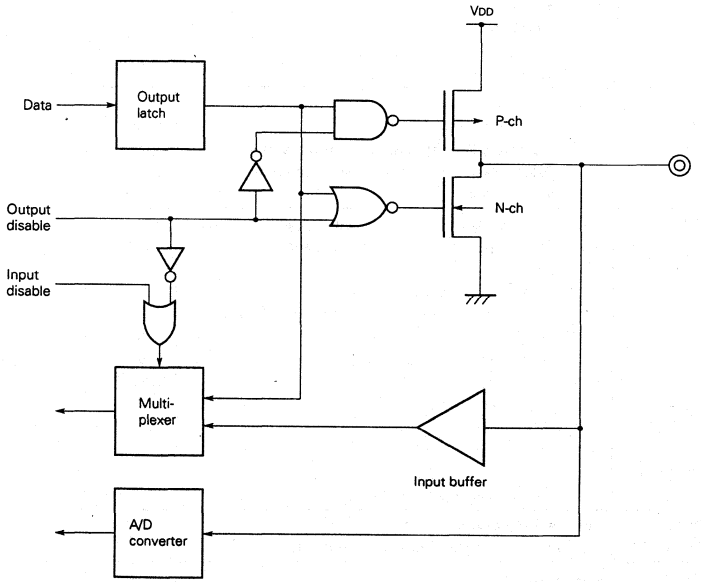
1.2 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

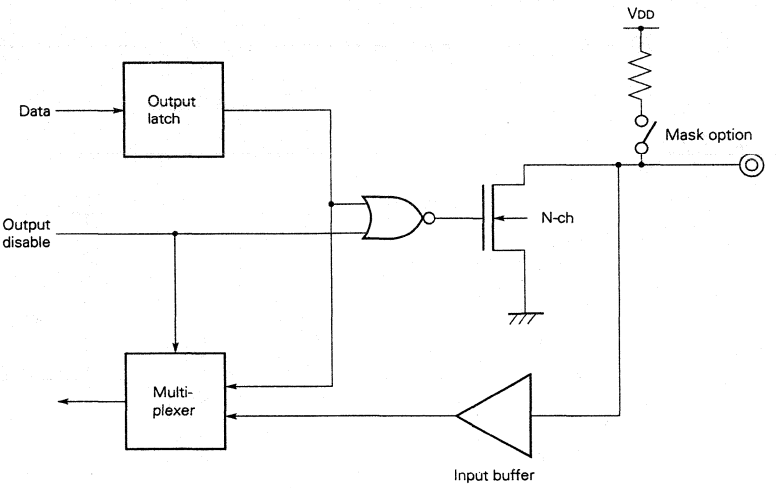
(1) $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$



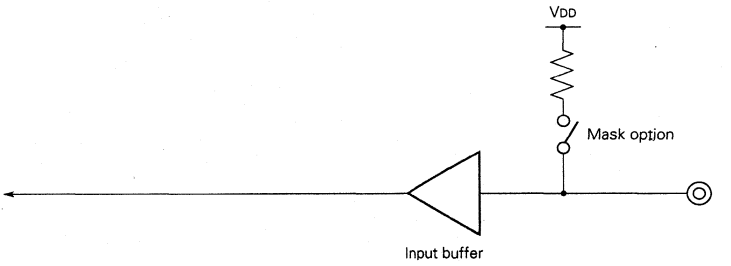
(2) $P0C_0$/ADC_0 to $P0C_3$/ADC_3



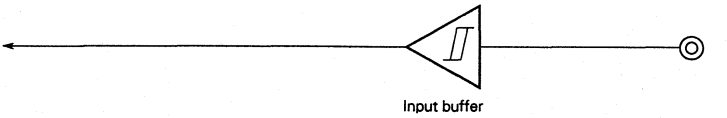
(3) P0D0 to P0D3, P1A0 to P1A3



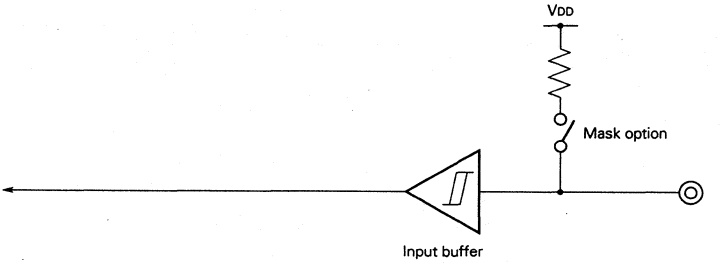
(4) P1B0



(5) INT



(6) $\overline{\text{RESET}}$



1.3 HANDLING UNUSED PINS

To prevent malfunctions, connect the unused pins as follows:

Fig. 1-1 Handling Unused Pins

Pin			Handling
Port Note1	Input mode	P0A, P0B, P0C, P0D, P1A, P1B0	To be connected to the V_{DD} or GND pin
	Output mode	P0A, P0B, POC (CMOS port)	Open
		P0D, P1A (N-ch open-drain port)	Open (0s are output on the pins.)
INT			To be connected to the V_{DD} or GND pin
V_{ADC}			To be connected to the V_{DD} pin Note2

Note 1. When a pull-up resistor is not incorporated.

2. Connect the V_{ADC} pin to the V_{DD} pin even when the A/D converter is not used.

22. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V		−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$ OSC_0, OSC_1		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} + 0.3	
			Note 2	−0.3 to +11.0	
Output Voltage	V_O	P0A, P0B, P0C		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} + 0.3	
			Note 2	−0.3 to +11.0	
High Level Output Current	I_{OH}	Each of P0A, P0B, and P0C		−15	mA
		Total of all pins		−30	
Low Level Output Current	I_{OL}	Each of P0A, P0B, P0C and P1B		15	mA
		Each of P0D and P1A		30	
		Total of all pins		100	
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C		180	mW

RECOMMENDED POWER VOLTAGE RANGE (T_a = −40 to +85 °C)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CPU **Note 3**	2.7		5.5	V	
A/D Converter	4.5		5.5	V	Absolute accuracy: ±1.5 LSB or less
Zerocross Detection Circuit	4.5		5.5	V	Zerocross accuracy: Azx = ±120 mV or less
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (from 0 to 2.7 V): 8192 × 16/f_{CC} or less

Note 1. When a built-in pull-up resistor is selected as mask option

2. When N-ch open-drain input/output is selected.

3. Excluding the A/D converter, zerocross detection circuit, and power-on/power-down rest circuits.

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
System Clock Oscillation Frequency	f_{CC}	1.6	2	2.4	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 9.1 kΩ
		0.8	1	1.2	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 22 kΩ
		0.6	1	1.2	MHz	V_{DD} = 2.7 to 5.5 V, R_{OSC} = 22 kΩ
		400	500	600	kHz	V_{DD} = 2.7 to 3.3 V R_{OSC} = 47 kΩ

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0D, P1A	Note 1
				9			Note 2
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $\overline{SCK}$, SI, INT	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P1A, $\overline{RESET}$, $\overline{SCK}$, SI, INT	
High-Level Output Voltage	V_{OH}			V_{DD} −0.3	V	P0A, P0B, P0C Note 3	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1.0 mA
				V_{DD} −0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OH} = −0.5 mA
Low-Level Output Voltage	V_{OL1}			0.3	V	P0A, P0B, P0C, P0D, P1A Note 3	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA
				0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA
	V_{OL2}			1.0	V	P0D, P1A I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V
				2.0	V		V_{DD} = 2.7 to 4.5 V
High-Level Input Leakage Current	I_{LIH1}			3	μA	P0A, P0B, P0C, P0D, P1A, P1B V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	P0D, P1A, V_{IN} = 9 V Note 2	
Low-Level Input Leakage Current	I_{LIL}			−5	μA	P0A, P0B, P0C, P0D, P1A, P1B V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			3	μA	P0A, P0B, P0C, P0D, P1A V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	P0D, P1A, V_{OUT} = 9 V Note 2	
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, P1A V_{OUT} = 0 V	
Built-In Pull-Up Resistor	R_{PULL}	50	100	200	kΩ	P0A, P0B, P1B, $\overline{RESET}$	

Note 1. When a built-in pull-up resistor is selected as mask option
2. When N-ch open-drain input/output is selected
3. When a built-in pull-up resistor is not selected by the software

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS		
Power Supply Current [Note]	I_{DD1}		0.8	2.0	mA	Operation mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			0.5	1.5	mA			V_{DD} = 3 V ±10 %
			0.4	1.0	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.25	0.75	mA			V_{DD} = 3 V ±10 %
			250	500	μA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			125	375	μA			V_{DD} = 3 V ±10 %
	I_{DD2}		0.6	1.5	mA	HALT mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			0.3	1.0	mA			V_{DD} = 3 V ±10 %
			0.3	0.8	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.15	0.5	mA			V_{DD} = 3 V ±10 %
			150	300	μA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			100	200	μA			V_{DD} = 3 V ±10 %
	I_{DD3}		3.0	10	μA	STOP mode	V_{DD} = 5 V ±10 %	
			2.0	10	μA		V_{DD} = 3 V ±10 %	

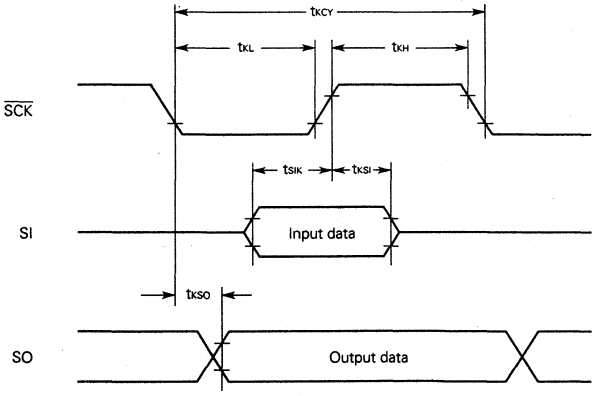
Note When neither the A/D converter nor zerocross detection circuit is used, and excluding the current which flows through the built-in pull-up resistor.

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

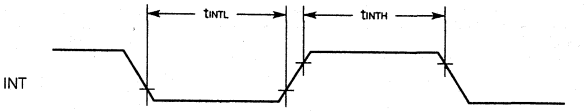
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Internal Clock Cycle Time	t_{CY}	6.6		41	μs	V_{DD} = 4.5 to 5.5 V	
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		16			μs		Output
		10			μs		Input
		32			μs		Output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		t_{KCY}/2−6			μs		Output
		5.0			μs		Input
		t_{KCY}/2−12			μs		Output
SI Setup Time (Referred to $\overline{SCK}$ ↑)	t_{SIK}	100			ns		
SI Hold Time (Referred to $\overline{SCK}$ ↑)	t_{KSI}	100			ns		
SO Output Delay Time (Referred to $\overline{SCK}$ ↓)	t_{KSO}			4.5	μs		
Interrupt Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		

Remark t_{CY} = 16/fcc (fcc: frequency of system clock oscillator)

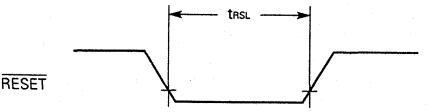
Serial transfer timing



Interrupt input timing

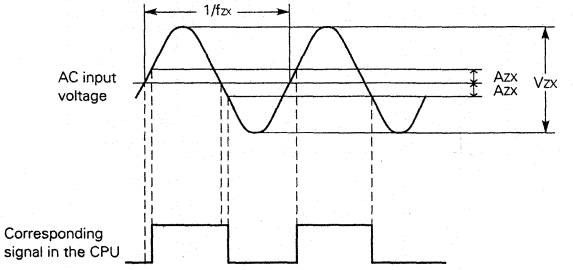


$\overline{\text{RESET}}$ input timing



ZEROCROSS DETECTION INPUT CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V_{P-P}	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	f_{ZX}	40	50 or 60	1000	Hz	
Zerocross Accuracy	A_{ZX}		40	±120	mV	50 Hz or 60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by A_{ZX} in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C, V_{ADC} = V_{DD} ±0.5 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Resolution		8	8	8	bit	
Absolute Accuracy Note 1				±1.5	LSB	V_{ADC} = V_{DD}
ADC Circuit Current	I_{ADC}		1.5	2.0	mA	
Conversion Time Note 2	t_{CONV}			400/fcc	s	

Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)

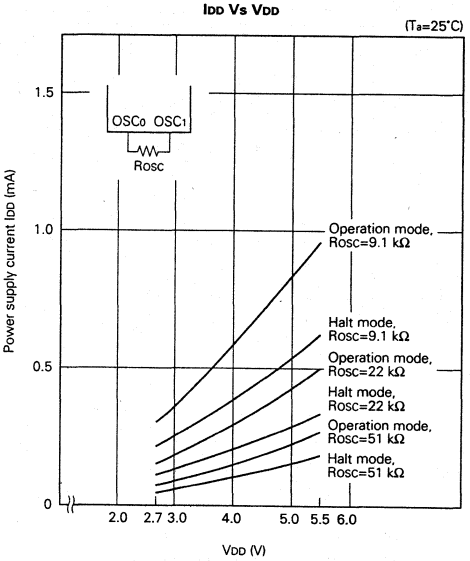
2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at fcc = 2 MHz, 200 μs)

CHARACTERISTICS OF THE POWER-ON AND POWER-DOWN RESET CIRCUITS (T_a = −40 to +85 °C)

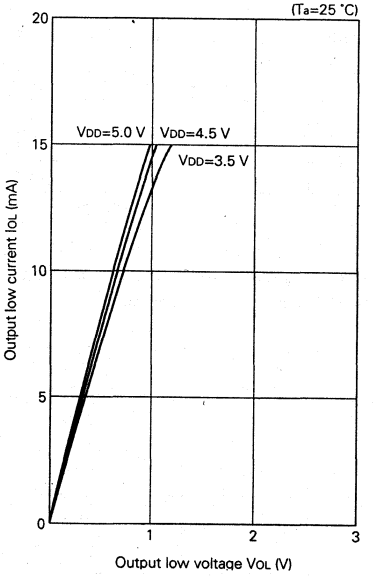
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Time it Takes for the Power to Rise to the Voltage Level that Enables Power-On Reset	t_{POR}			8192 × 16/fcc	s	The power voltage (V_{DD}) must change from ground level to 2.7 V.
Low Voltage to be Detected by the Power-Down Reset Circuit	V_{PDR}		3.5	4.5	V	When PDRESEN = 1

23. CHARACTERISTIC CURVES (FOR REFERENCE)

IDD Vs VDD

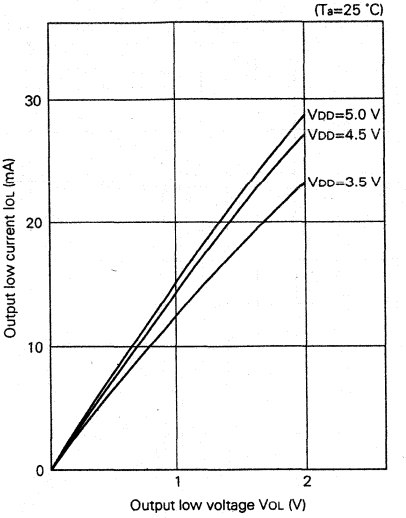


IOL Vs VOL (P0A, P0B, P0C, P1B)



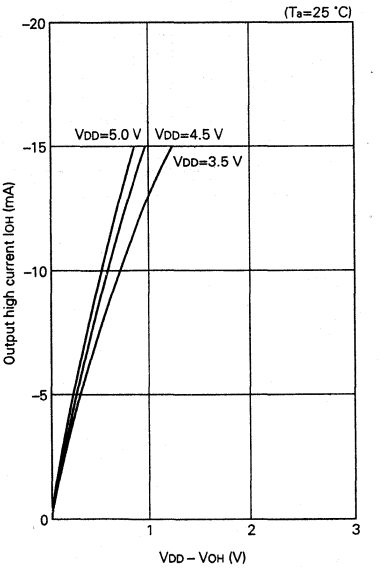
Note Absolute maximum rating of output current is 15 mA per pin.

I_{OL} Vs V_{OL} (P0D, P1A)



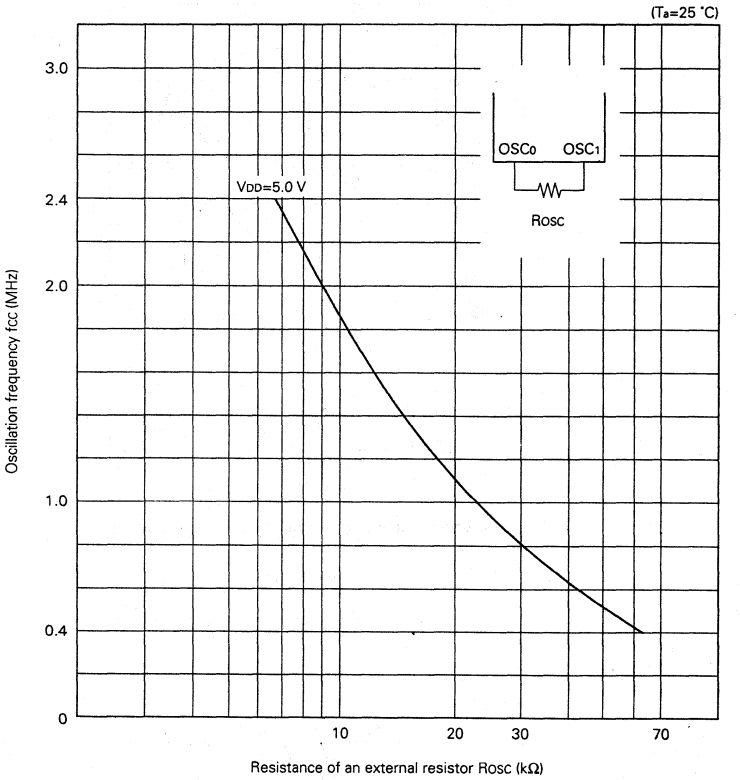
Note Absolute maximum rating of output current is 30 mA per pin.

I_{OH} Vs (V_{DD} – V_{OH})



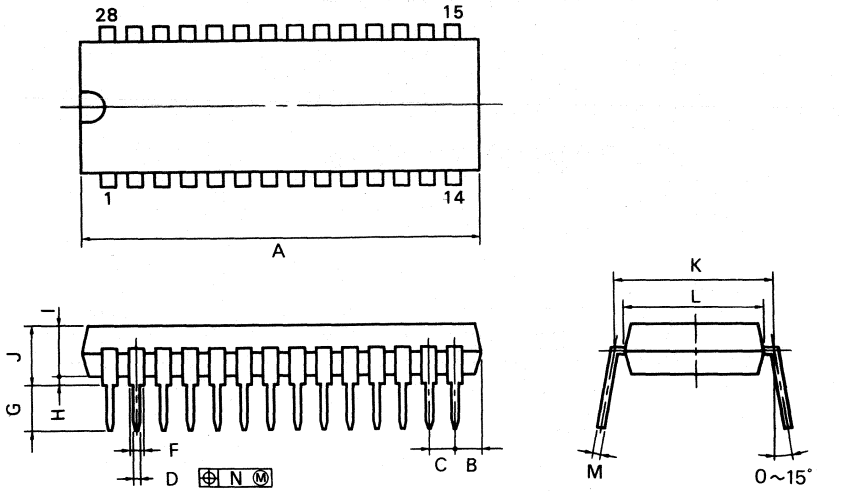
Note Absolute maximum rating of output current is –15 mA per pin.

fcc Vs Rosc


(Ta=25 °C)
3.0
2.4
2.0
1.0
0.4
0
VDD=5.0 V
OSCo
OSC1
Rosc
10
20
30
70
Oscillation frequency fcc (MHz)
Resistance of an external resistor Rosc (kΩ)

24. PACKAGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

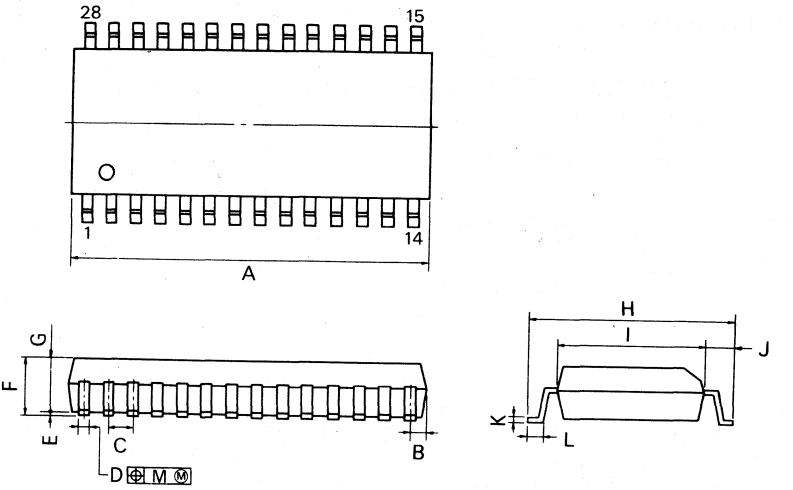
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

25. MICROCONTROLLER FUNCTIONS FOR SMALL HOME ELECTRIC APPLIANCES

Item	μPD17134A	μPD17135A	[redacted]	μPD17137A	Remarks
ROM size	1024 × 16 bits		2048 × 16 bits		
RAM size	112 × 4 bits				
Number of I/O port lines	22 lines (including one input line and one sense input line)				Including 8 N-ch open drain lines
A/D converter input	4 channels				Also used as port pins
Timer	3 timers				8 bits: 2 channels, 7 bits: 1 channel (Basic interval timers)
Serial interface	1 channel				Also used as port pin
Stack	5 levels				
Power-on/power-down reset	Provided (valid only when V_{DD} = 5 V ±10 %)				
System clock	RC oscillation	Ceramic/crystal oscillation	RC oscillation	Ceramic/crystal oscillation	
Instruction execution time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby function	Provided				STOP/HALT
Power supply	2.7 to 5.5 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
One time PROM product	μPD17P136A	μPD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output

26. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) shall be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 26-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17136ACT-xxx	28-pin plastic sharink DIP (400 mil)	• Wave soldering • Partial heating method
μPD17136AGT-xxx	28-pin plastic SOP (375 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 26-2 Soldering Conditions

Symbol	Soldering process	Soldring conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow processes: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow processes: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow processes: 1
Partial heating method	Terminal to be heated	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution **Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).**

Remark For details of the recommended soldering conditions, refer to our document **"SMT MANUAL" (IEI-1207).**

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES
4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P136A is a one-time PROM version of the μPD17136A, in which the internal mask ROM of the μPD17136A is replaced with a one-time PROM that can be written to just once.

Since a user program can be written on the PROM, this microcontroller is suited for trial manufacture during μPD17134A, μPD17136A system development, or multiple device production.

The reader also should refer to the publications on the μPD17136A.

FEATURES

- 17K architecture: General registers
- Pin compatible with the μPD17136A (except for PROM programming function)
- Internal one-time PROM: 2048 × 16 bits
- Operating supply voltage: 2.7 to 5.5 V
- System clock: RC oscillation

ORDERING INFORMATION

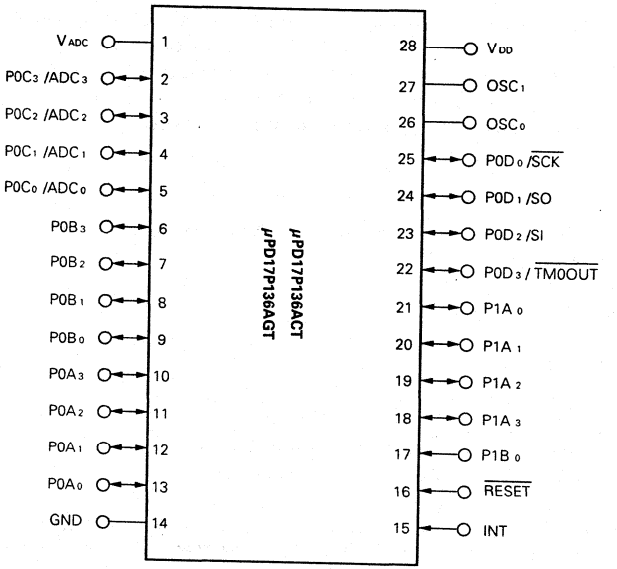
Order Code	Package	Quality Grade
μPD17P136ACT	28-pin plastic shrink DIP (400 mil)	Standard
μPD17P136AGT	28-pin plastic SOP (375 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In the program write/verify mode, the voltage used for programming is applied to pin No. 17, P1B0/VPP. If a voltage of VDD plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

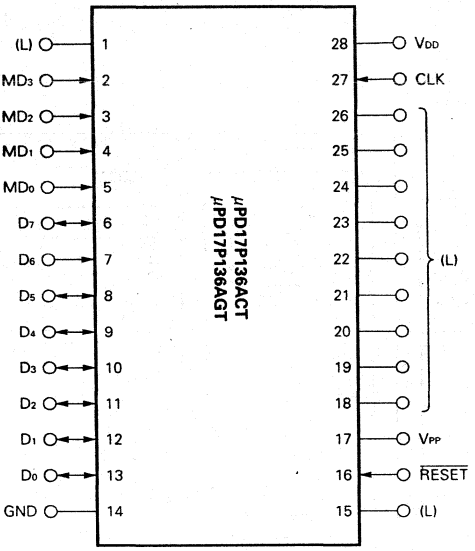
PIN CONFIGURATION (Top View)

(1) Normal operating mode



ADC0 to ADC3	:	Analog input for A/D converters
$\overline{\text{RESET}}$	:	Reset input
$\overline{\text{TM0OUT}}$	:	Timer 0 carry output
INT	:	External interrupt input
SI	:	Serial data input
SO	:	Serial data output
$\overline{\text{SCK}}$	:	Serial clock input /output
OSC0 to OSC1	:	System clock oscillation
P0A0 to P0A3	:	Port 0A
P0B0 to P0B3	:	Port 0B
P0C0 to P0C3	:	Port 0C
P0D0 to P0D3	:	Port 0D
P1A0 to P1A3	:	Port 1A
P1B0	:	Port 1B
CLK	:	Clock input for address update
MD0 to MD3	:	Operating mode selection
D0 to D7	:	Data input /output
VADC	:	Analog power supply
VPP	:	Program voltage
VDD	:	Positive power supply
GND	:	Ground

(2) Program memory write /verify mode

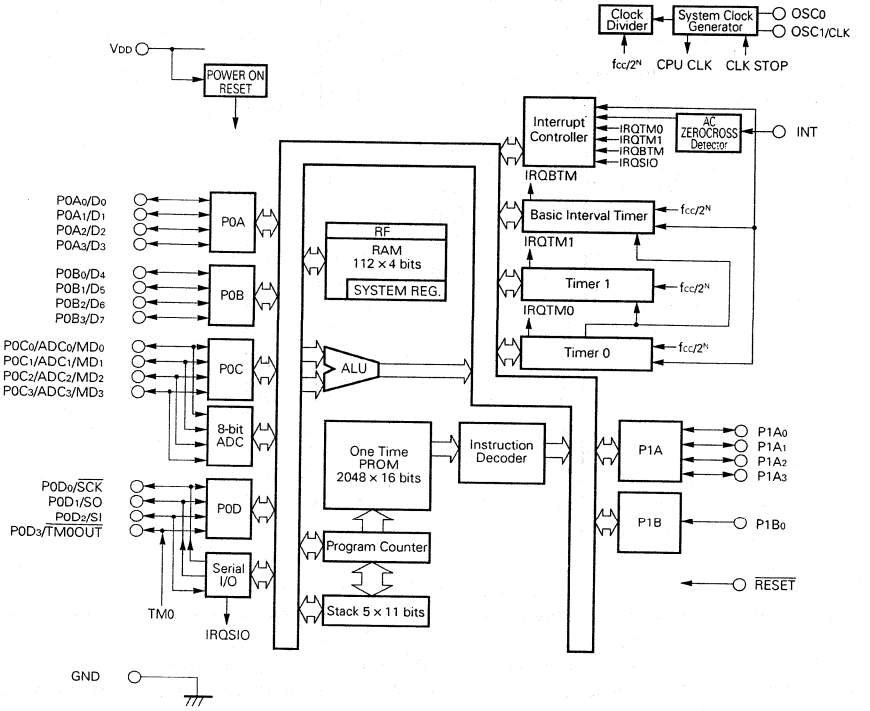


Cautions **Symbols in parentheses denote the processing for the pins not to be used in the program memory write/verify mode.**

L: Connect these pins separately to the GND pin through pull-down resistors.

$\overline{\text{RESET}}$: Apply a voltage equal to V_{DD} to this pin in the program write/verify mode. When this pin is used as the system reset input pin before the microcontroller enters the program write/verify mode, apply a voltage equal to V_{DD} to the pin 10 μs after the voltage is applied to the V_{DD} pin. For details, see 3.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT	AFTER POWER-ON OR RESET
1	V_{ADC}	Power for the A /D converter	—	—

2 to 5	$P0C_3$/ADC_3 to $P0C_0$/ADC_0	Pin for port 0C and A /D converter
		• $P0C_3$ to $P0C_0$
		  • 4-bit input /output port
		  • Input /output setting allowed in units of 1 bit
		• ADC_3 to ADC_0
		  • Analog input for the A /D converter
			CMOS push-pull	Input (P0C)

6 to 9	$P0B_3$ to $P0B_0$	Port 0B • 4-bit input /output port • Input /output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
10 to 13	$P0A_3$ to $P0A_0$	Port 0A • 4-bit input /output port • Input /output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
14	GND	Ground	—	—
15	INT	Input of external interrupt requests and release of standby mode	—	—
16	$\overline{RESET}$	System reset input pin	—	—
17	$P1B_0$	Port 1B • 1-bit input /output port • Pull-up resistor incorporation specifiable by mask option	—	Input
18 to 21	$P1A_3$ to $P1A_0$	Port 1A • 4-bit input /output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input

22
23
24
25
	$P0D_3$/ $\overline{TM0OUT}$
	$P0D_2$/SI
	$P0D_1$/SO
	$P0D_0$/$\overline{SCK}$
		Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input /output.
		• $P0D_3$ to $P0D_0$
		  • 4-bit input /output port
		  • Input /output setting allowed in units of 1 bit
		• $\overline{TM0OUT}$
		  • Timer 0 carry output
		• SI
		  • Serial data input
		• SO
		  • Serial data output
		• $\overline{SCK}$
		  • Serial clock input /output
			N-ch open-drain	Input

26 27	OSC_0 OSC_1	For system clock oscillation. Resistor is connected from OSC_0, OSC_1.	—	—
28	V_{DD}	Positive power supply	—	—

1.2 PROGRAM MEMORY WRITE /VERIFY MODE

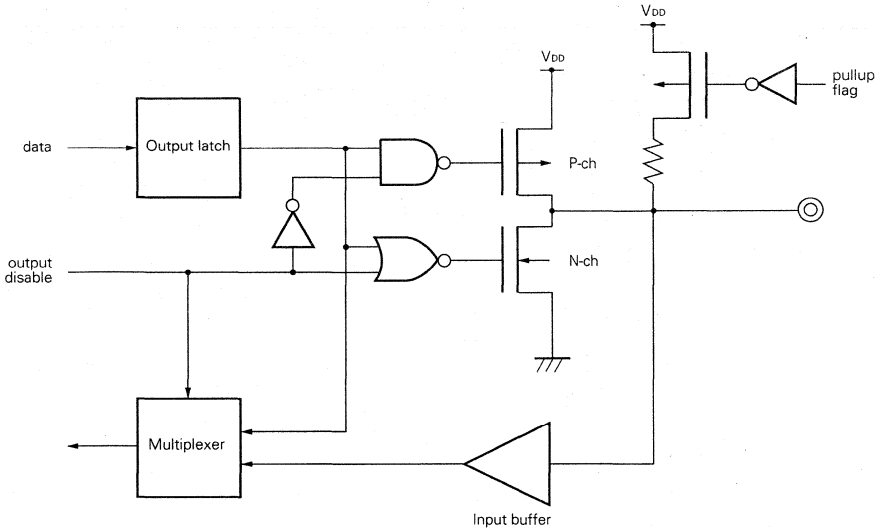
PIN No.	PIN NAME	FUNCTION	I/O
2 to 5	MD_3 to MD_0	Input pins used as operation mode selection pins when writing to program memory or verifying its contents	Input
6 to 13	D_7 to D_0	Input /output pins for 8-bit data used when writing to program memory or verifying its contents	I/O
14	GND	Ground	—
17	V_{PP}	+12.5 V is applied to this program voltage pin when writing to program memory or verifying its contents.	—
27	CLK	Input pin for address update clock used when writing to program memory or verifying its contents	Input
28	V_{DD}	+6 V is applied to this positive power supply pin when writing to program memory or verifying its contents.	—

I/O: Input /output

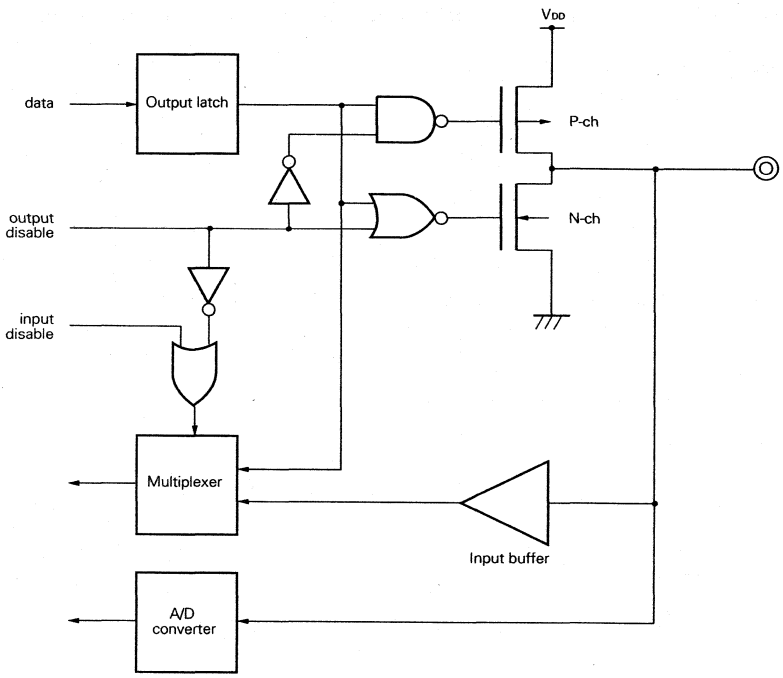
1.3 PIN EQUIVALENT CIRCUIT

The equivalent circuit of each μPD17P136A pin is shown below; some part of the circuit is simplified.

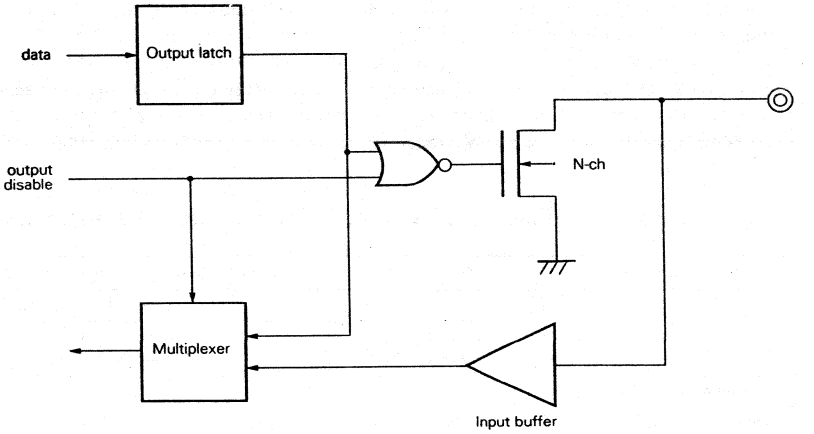
(1) $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$



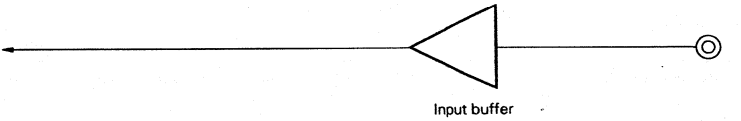
(2) $P0C_0$ /ADC_0, to $P0C_3$ /ADC_3



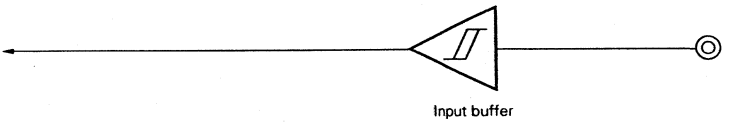
(3) $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$



(4) $P1B_0$



(5) INT, $\overline{\text{RESET}}$



2. DIFFERENCES AMONG THE μPD17134A, μPD17136A, AND μPD17P136A

The μPD17P136A is a one-time PROM version of the μPD17136A, in which the internal mask ROM is replaced with a one-time PROM.

Table 2-1 lists the differences among the μPD17134A, μPD17136A, and μPD17P136A.

The μPD17P136A has the same CPU functions and internal peripheral hardwares as those of μPD17134A and μPD17136A except for its program memory, program size, address register size, and mask option. The μPD17P136A can be used for evaluation of programs during μPD17134A, μPD17136A system development.

Table 2-1 Differences among the μPD17134A, μPD17136A, and μPD17P136A

Item	μPD17134A	μPD17136A	μPD17P136A
ROM	Mask ROM		One-time PROM
	1024 × 16 bits (0000H–03FFH)	2048 × 16 bits (0000H–07FFH)	
Program counter (PC)	10 bits	11 bits	
Address register (AR)			
Address stack register			
Pull-up resistors of pins P0D, P1A, P1B, and $\overline{\text{RESET}}$	Mask option		None
Connection pin	V_{PP} pin and operation mode selection pins are not provided.		V_{PP} pin and operation mode selection pins are provided.
Supply voltage	2.7 to 5.5 V (when A /D converter is used: 5 V ± 10 %)		
Package	28-pin shrink DIP 28-pin SOP		

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P136A internal program memory consists of a 2048 × 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used when Writing to Program Memory or Verifying its Contents

Pin name	Function
V_{PP}	+12.5 V is applied to this program voltage pin when writing to program memory or verifying its contents.
V_{DD}	+6 V is applied to this positive power supply pin when writing to program memory or verifying its contents.
$\overline{RESET}$	System reset input pin. The specific signal applied to this pin initializes the conditions of the microcontroller before it enters the program write/verify mode.
CLK	Input pin for address update clock used when writing to program memory or verifying its contents. Increment the program memory address by one on reception of 4 pulses on this CLK pin.
MD_0 to MD_3	Input pins used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

3.1 PROGRAM MEMORY WRITE /VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P136A enters program memory write /verify mode. A specific operating mode is then selected by setting the MD_0 to MD_3 pins as follows. Set the $\overline{RESET}$ pin and the other unused pins to GND level by means of pull-down resistors.

Table 3-2 Operating Mode Specification

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

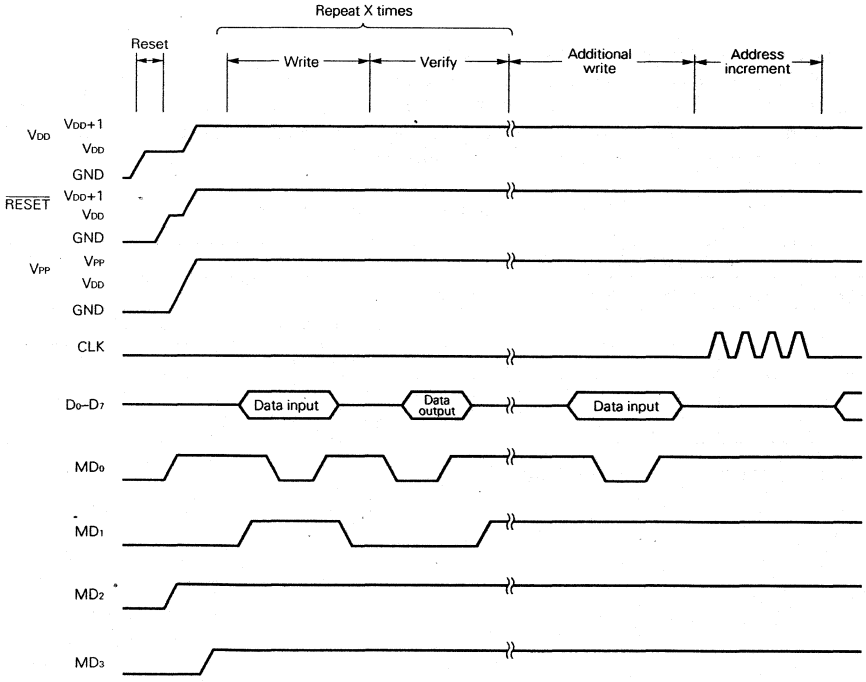
Remark ×: Don't care. L (low) or H (high)

3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} and $\overline{RESET}$ to low level.
(3) Wait 10 μs. Then apply 5 V to $\overline{RESET}$.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and $\overline{RESET}$ and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1-ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of 4 pulses on CLK.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to V_{DD} and V_{PP}.
(16) Turn power off.

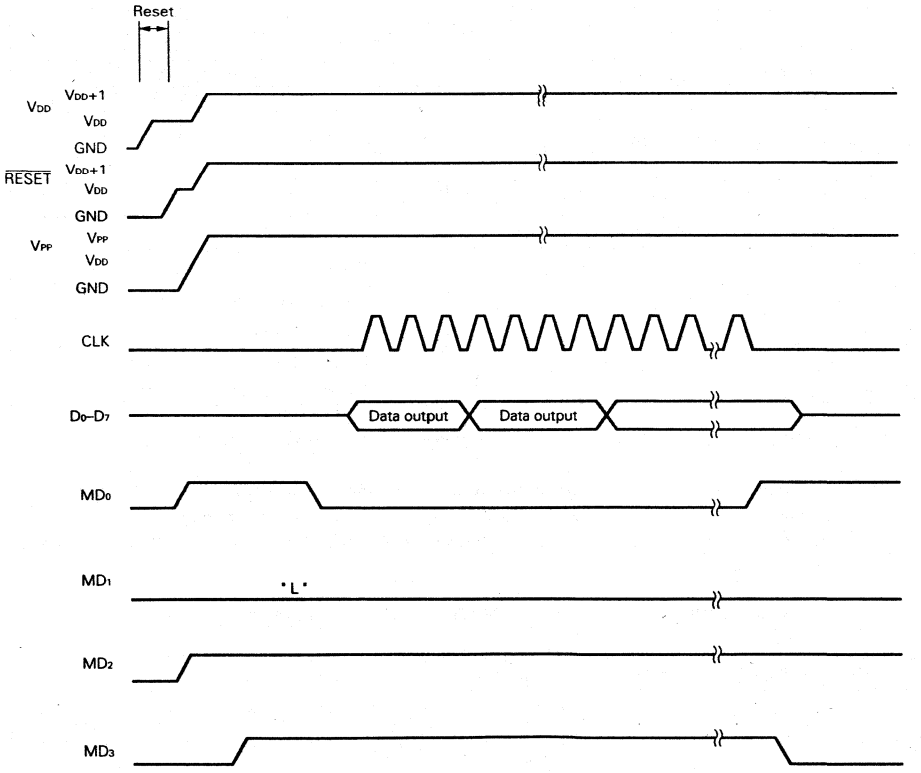
The timing for PROM writing steps (2) to (12) is shown below.



3.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} and $\overline{RESET}$ to low level.
(3) Wait 10 μs. Then apply 5 V to $\overline{RESET}$.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and $\overline{RESET}$ 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of 4 clock pulses on CLK.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to V_{DD} and V_{PP}.
(11) Turn power off.

The timing for PROM reading steps (2) to (9) is shown below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply Voltage	V_{DD}		−0.3 to +7.0	V
PROM Supply Voltage	V_{PP}		−0.3 to +13.5	V
Analog Supply Voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V	−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$, OSC_0, OSC_1	−0.3 to V_{DD} + 0.3	V
		P0D, P1A	−0.3 to +11.0	
Output Voltage	V_O	P0A, P0B, P0C	−0.3 to V_{DD} + 0.3	V
		P0D, P1A	−0.3 to +11.0	
High-Level Output Current	I_{OH}	Each of P0A, P0B, and P0C	−15	mA
		Total of all pins	−30	
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C and P1B	15	mA
		Each of P0D and P1A	30	
		Total of all pins	100	
Operating Temperature	T_{opt}		−40 to +85	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C	180	mW

RECOMMENDED POWER VOLTAGE (T_a = −40 to +85 °C)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CPU **Note**	2.7		5.5	V	
A/D Converter	4.5		5.5	V	Absolute accuracy: ±1.5 LSB or less
Zerocross detection Circuit	4.5		5.5	V	Zerocross accuracy: A_{ZX} = ±120 mV or less
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (V_{DD} = 0 → 2.7 V): 8192 × 16/fcc or less

Note Excluding the A/D converter, zerocross detection circuit, and power-on/power-down reset circuits.

Caution In the program write/verify mode, the voltage used for programming is applied to pin No. 17, $P1B_0/V_{PP}$. If a voltage of V_{DD} plus 0.3 V or more is applied to this pin in the normal operation mode, the microcontroller may crash. Design the circuit so that a voltage of this magnitude is never applied to the pin.

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
System Clock Oscillation Frequency	fcc	1.6	2	2.4	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 9.1 kΩ
		0.8	1	1.2	MHz	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 22 kΩ
		0.6	1	1.2	MHz	V_{DD} = 2.7 to 5.5 V, R_{OSC} = 22 kΩ
		400	500	600	kHz	V_{DD} = 2.7 to 3.3 V, R_{OSC} = 47 kΩ

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to + 85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS		
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B		
	V_{IH2}	0.7 V_{DD}		9	V	P0D, P1A		
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, SCK, SI, INT		
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B		
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P1A, $\overline{RESET}$, SCK, SI, INT		
High-Level Output Voltage	V_{OH}			V_{DD} −0.3	V	P0A, P0B, P0C Note 1		V_{DD} = 4.5 to 5.5 V, I_{OH} = −1.0 mA
				V_{DD} −0.3	V			V_{DD} = 2.7 to 4.5 V, I_{OH} = −0.5 mA
Low-Level Output Voltage	V_{OL1}			0.3	V	P0A, P0B, P0C, P0D, P1A		V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA
				0.3	V			V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA
	V_{OL2}			1.0	V	P0D, P1A		V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA
				2.0	V			V_{DD} = 2.7 to 4.5 V, I_{OL} = 15 mA
High-Level Input Leakage Current	I_{LIH1}			3	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = V_{DD}		
	I_{LIH2}			10	μA	P0D, P1A, V_{IN} = 9 V		
Low-Level Input Leakage Current	I_{LIL}			−5	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = 0 V		
High-Level Output Leakage Current	I_{LOH1}			3	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = V_{DD}		
	I_{LOH2}			10	μA	P0D, P1A, V_{OUT} = 9 V		
Low-Level Output Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = 0 V		
Built-In Pull-Up Resister	R_{PULL}	50	100	200	kΩ	P0A, P0B		
Power Supply Current Note 2	I_{DD1}		2.0	4.0	mA	Operation mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			1.0	2.5	mA			V_{DD} = 3 V ±10 %
			1.2	2.4	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.7	2.2	mA			V_{DD} = 3 V ±10 %
			1.0	2.0	mA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			0.5	2.0	mA			V_{DD} = 3 V ±10 %
	I_{DD2}		1.7	3.5	mA	HALT mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %
			0.9	2.4	mA			V_{DD} = 3 V ±10 %
			1.0	2.0	mA		f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %
			0.6	2.1	mA			V_{DD} = 3 V ±10 %
			0.8	1.6	mA		f_{CC} = 455 kHz	V_{DD} = 5 V ±10 %
			0.5	2.0	mA			V_{DD} = 3 V ±10 %
	I_{DD3}		12	50	μA	STOP mode	V_{DD} = 5 V ±10 %	
			10	45	μA		V_{DD} = 3 V ±10 %	

Note 1. When a built-in pull-up resistor is not selected by the software

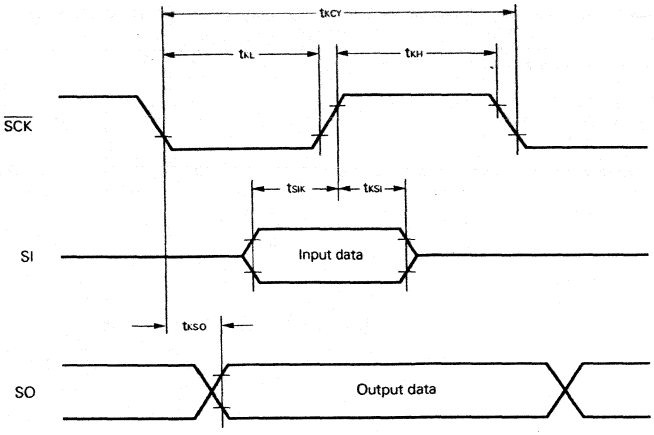
2. When neither the A/D converter nor zerocross detection circuit is used, and excluding the current which flows through the built-in pull-up resistor

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

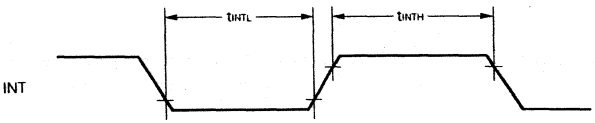
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Internal Clock Cycle Time	t_{CY}	6.6		41	μS	V_{DD} = 4.5 to 5.5 V	
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μS	V_{DD} = 4.5 to 5.5 V	Input
		16			μS		Output
		10			μS		Input
		32			μS		Output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μS	V_{DD} = 4.5 to 5.5 V	Input
		t_{KCY}/2-6			μS		Output
		5.0			μS		Input
		t_{KCY}/2-12			μS		Output
SI Setup Time (Referred to $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI Hold Time (Referred to $\overline{SCK}$↑)	t_{KSI}	100			ns		
SO Output Delay Time (Referred to $\overline{SCK}$↓)	t_{KSO}			4.5	μs		
Interrupt Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μS	V_{DD} = 4.5 to 5.5 V	
		50			μS		
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μS	V_{DD} = 4.5 to 5.5 V	
		50			μS		

Remark t_{CY} = 16/fcc (fcc: frequency of system clock oscillator)

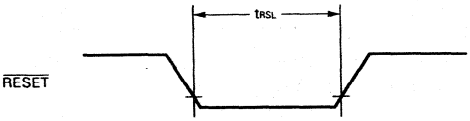
Serial transfer timing



Interrupt input timing

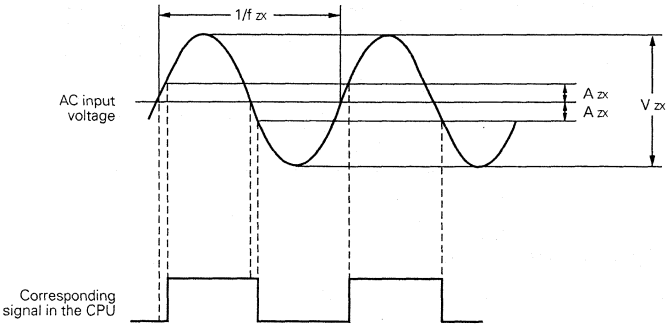


$\overline{\text{RESET}}$ input timing



ZEROCROSS CHARACTERISTICS (T_a = −25 to +75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	f_{ZX}	40	50 or 60	1000	Hz	
Zerocross Accuracy	A_{ZX}		40	±120	mV	50 or 60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by Azx in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (T_a = −25 to + 75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Resolution		8	8	8	bit	
Absolute Accuracy[Note1]				±1.5	LSB	$V_{ADC} = V_{DD}$
ADC Circuit Current	I_{AREF}		1.5	2.0	mA	
Conversion Time	t_{CONV}			400 /fx	s	**Note 2**

Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)

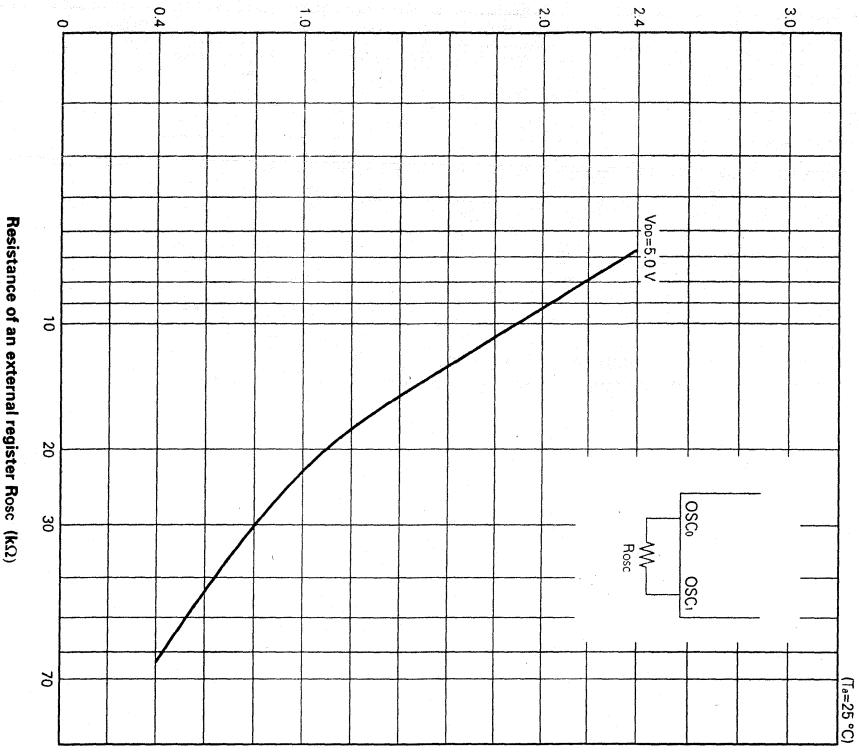
2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at fx = 2 MHz, 200 μs)

CHARACTERISTICS OF THE POWER-ON/POWER-DOWN RESET CIRCUITS (T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Time it Takes for the Power to Rise to the Voltage Level that Enables Power-On Reset	t_{POR}			8192 × 16/fcc	s	The power voltage (V_{DD}) must change from ground level to 2.7 V
Low Voltage to be Detected by the Power-Down Reset Circuit	V_{PDR}		3.5	4.5	V	When PDRESEN = 1

2

fcc vs Rosc


Oscillation frequency fcc (MHz)
0
0.4
1.0
2.0
2.4
3.0
Vcc=5.0 V
OSCo
OSCi
Rosc
(Ta=25 °C)
Resistance of an external register Rosc (kΩ)
10
20
30
70

DC PROGRAMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CLK
	V_{IH2}	V_{DD}–0.5		V_{DD}	V	CLK
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}–1.0			V	I_{OH} = –1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

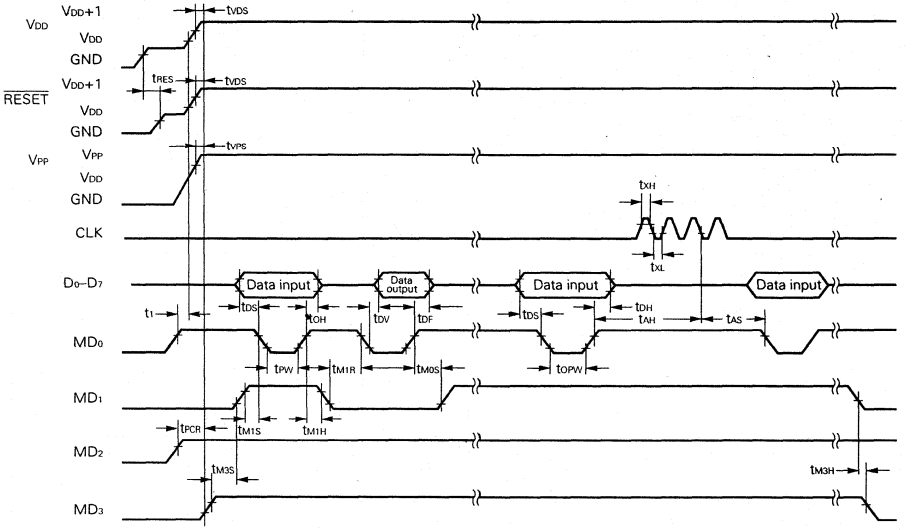
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

CHARACTERISTICS	SYMBOL	NOTE 1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time to MD0↓ Note 2	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time to MD0↑ Note 2	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0↓→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recovery Time to MD0↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	—	10			μs	
CLK Input High, Low Level Range	t_{XH}, t_{XL}	—	0.125			μs	
CLK Input Frequency	f_X	—			2	MHz	
Initial Mode Set Time	t_I	—	2			μs	
MD3 Setup Time to MD1↑	t_{M3S}	—	2			μs	
MD3 Hold Time to MD1↓	t_{M3H}	—	2			μs	
MD3 Setup Time to MD0↓	t_{M3SR}	—	2			μs	Read program memory
Data Output Delay Time from Address Note 2	t_{DAD}	t_{ACC}			2	μs	Read program memory
Data Output Hold Time from Address Note 2	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t_{M3HR}	—	2			μs	Read program memory
Data Output Float Delay Time from MD3↓→	t_{DFR}	—	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

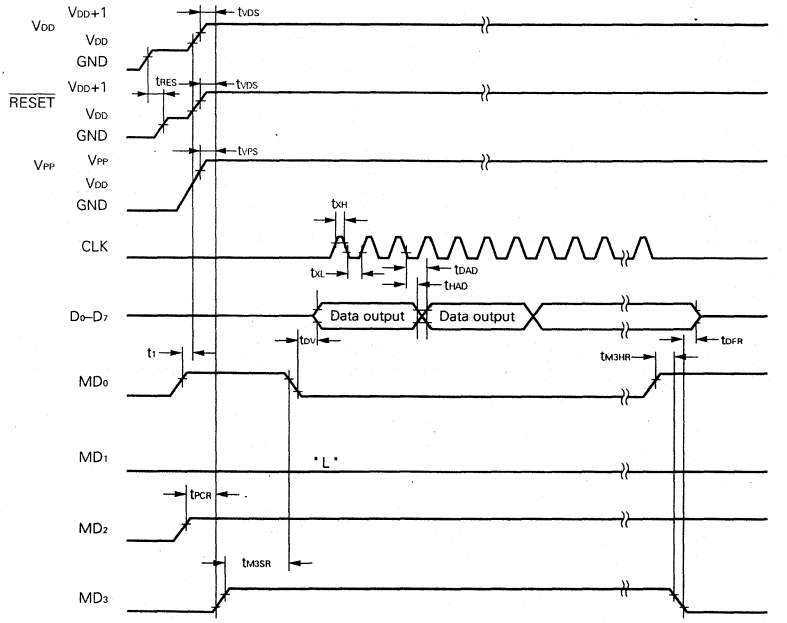
Note 1. Symbols for corresponding μPD27C256A (The μPD27C256A is used only for maintenance)

2. Internal address signal is incremented by one at the falling edge of the third CLK input.

Write Program Memory Timing

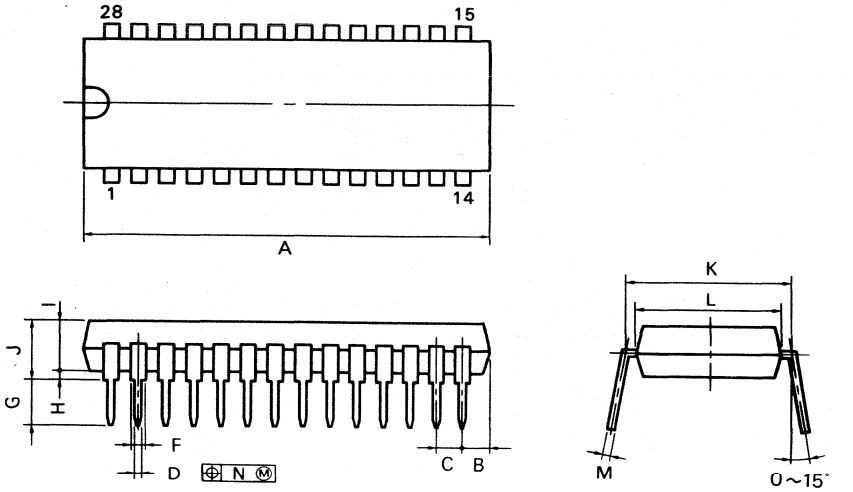


Read Program Memory Timing



5. PACKGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

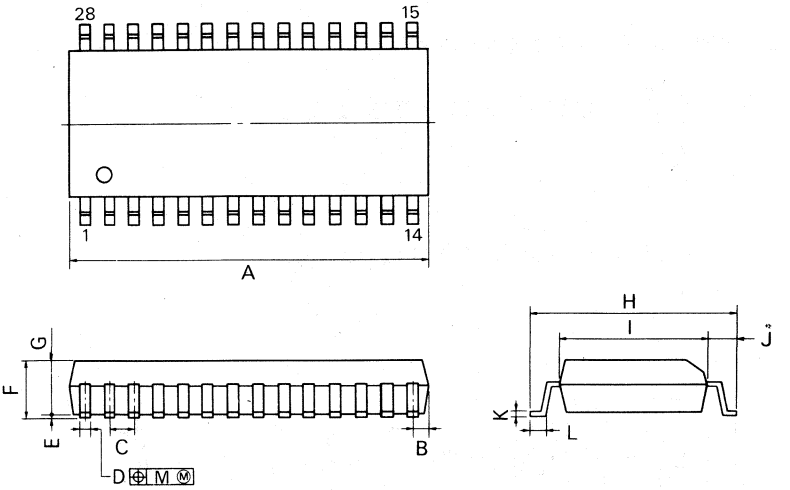
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

6. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) shall be met when soldering the μPD17P136A.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 6-1 Recommended Soldering Conditions

Product	Package	Recommended conditions
μPD17P136ACT	28-pin plastic shrink DIP (400 mil)	• Wave soldering • Partial heating method
μPD17P136AGT	28-pin plastic SOP (375 mil)	• Partial heating • Method

Table 6-2 Soldering Conditions

Soldering process	Soldering conditions
Partial heating method	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Soldering temperature: 260 °C or below Flow time: 10 seconds or below

Caution **Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).**

Remark For details of the recommended soldering conditions, refer to our document **"SMT Manual" (IEI-1207)**.

APPENDIX A. MICROCONTROLLER FAMILY FOR SMALL HOME ELECTRIC APPLIANCES

Item \ Product	μPD17134A	μPD17135A	μPD17136A	μPD17137A	μPD17P136A	μPD17P137A
ROM Size	1024 × 16 bits (Mask ROM)		2048 × 16 bits (Mask ROM)		2048 × 16 bits (One-time PROM)	
RAM Size	112 × 4 bits					
Number of I/O Port Lines	22 lines (Including 8 N-ch open drain lines)					
A/D converter input	4 channels					
Timer	3 timers { 8-bit timers: 2 (timer 0, timer 1); Basic interval timer: 1 (BTM) }					
Serial Interface	1 channel					
Stack	5 levels					
System Clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation
Instruction execution time	8 μs: @2 MHz	2 μs: @8 MHz	8 μs: @2 MHz	2 μs: @8 MHz	8 μs: @2 MHz	2 μs: @8 MHz
Standby Function	HALT mode /STOP mode					
Power-on/power-down reset	Provided					
Package	2.7 to 5.5 V (When A /D converter is used: V_{DD} = 5 V ±10 %)					
Supply Voltage	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)					

I/O: Input/output

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES
4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17135A is a 4-bit single-chip microcontroller containing 4 channels of 8-bit A/D converters, 3 channels of timers, an AC zerocross detector, a power-on reset circuit, and a serial interface.

For the CPU, the μPD17135A employs a 17K architecture using general registers. The new architecture allows operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (one word) long, allowing programming to be done efficiently.

Since the μPD17135A has on-chip A/D converters and an AC zerocross detector, it is suitable for electronic control of electric home appliances. The μPD17P137A, a one-time PROM product (can be written to only once) is available for evaluation of the μPD17135A and μPD17137A and for small-scale production.

FEATURES

- 17K architecture : General register
- Program memory (ROM) : 1024 x 16 bits
- Data memory (RAM) : 112 x 4 bits
- Instruction execution time : 2 μs (at 8 MHz: Ceramic oscillation)
- 8-bit A/D convertor : 4 channels
  Absolute accuracy: ±1.5 LSB or lower (V_{DD} 5 V ±10 %)
- Timer function : 3 channels
- 3-wire serial interface : 1 channel
- Input/output pins : 22 pins (including 1 general input pin and 1 sensor input pin)
- Power-on/power-down reset circuit

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17135ACT-xxx	28-pin plastic shrink DIP (400 mil)	Standard
μPD17135AGT-xxx	28-pin plastic SOP (375 mil)	Standard

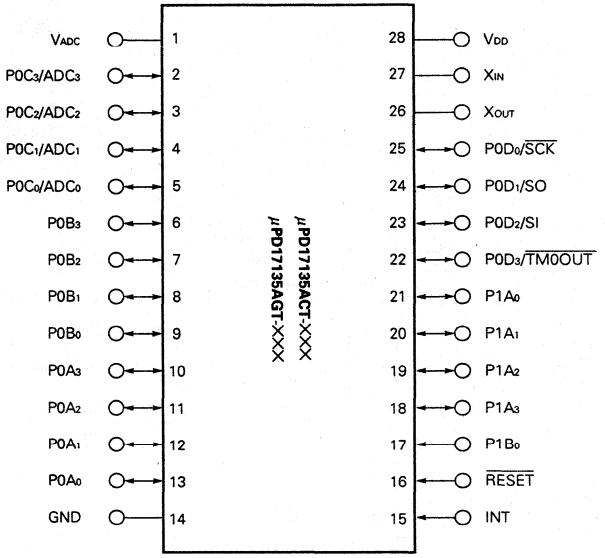
CHARACTERISTICS OF μPD17135A

Item	Description
ROM	1024 x 16 bits
RAM	112 x 4 bits (The stack is separate from data memory.)
Stack	5 address stacks, 3 interrupt stacks
Number of I/O ports	22 { • 20 I/O ports • 1 general input port • 1 input port for sensing an interrupt or AC zerocross
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ±1.5 LSB or less at a power voltage 5 V ±10 %
Timer	3 channels { • 2 channels for 8-bit timers (They can be used together as one 16-bit timer.) • 1 channel for a 7-bit basic interval timer (can be used as a watchdog timer)
Serial interface	1 channel (3-wire type)
Interrupt	• Up to 3 levels of multiple hardware interrupt • 1 external interrupt { • Shared with the input from the AC zerocross detection circuit • Rising-edge detection, falling-edge detection • Detection of the rising edge, falling edge, or both edges can be selected. • With the sense input • 4 internal interrupts { • Timer 0 • Timer 1 • Basic interval timer • Serial interface
Execution time of an instruction	2 μs at 8 MHz clock, ceramic oscillation
Standby function	STOP/HALT
Operating power voltage	• 2.7 to 5.5 V • 4.5 to 5.5 V (when the power-on/power-down reset functions are used)
Package	• 28-pin plastic shrink DIP • 28-pin plastic SOP
One-time PROM	μPD17P137A

I/O: input/output

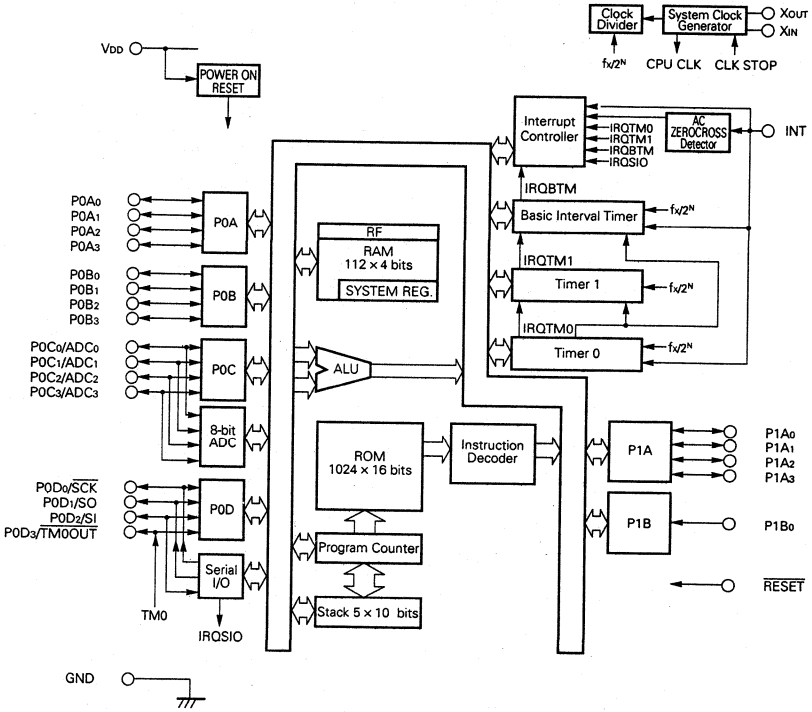
PIN CONFIGURATION (Top View)

28-pin plastic shrink DIP
28-pin plastic SOP



ADC0-ADC3	: Analog input for the A/D converter
RESET	: Reset input
TM0OUT	: Timer 0 carry output
INT	: External interrupt input
SI	: Serial data input
SO	: Serial data output
SCK	: Serial clock input/output
XIN, XOUT	: System clock oscillation
P0A0-P0A3	: Port 0A
P0B0-P0B3	: Port 0B
P0C0-P0C3	: Port 0C
P0D0-P0D3	: Port 0D
P1A0-P1A3	: Port 1A
P1B0	: Port 1B
VADC	: Analog power supply
VDD	: Power supply
GND	: Ground

BLOCK DIAGRAM



1. PINS

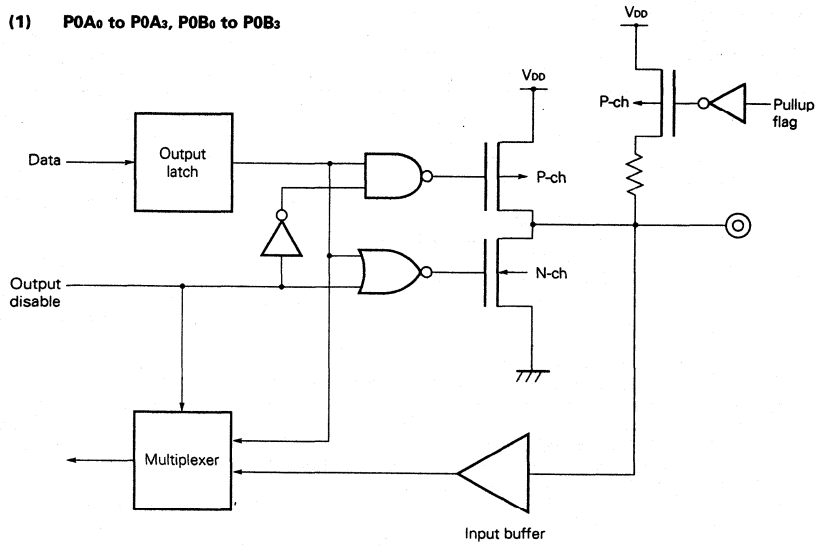
1.1 PIN FUNCTIONS

PIN No.	PIN NAME	FUNCTION	OUTPUT	AFTER POWER-ON OR RESET
1	V_{ADC}	Power voltage for the A/D converter and for the circuit generating reference voltage	–	–
2 to 5	$P0C_3/ADC_3$ to $P0C_0/ADC_0$	Pin for port 0C and A/D converter • $P0C_3$ to $P0C_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • ADC_3 to ADC_0 · Analog input for the A/D converter	CMOS push-pull	Input (P0C)
6 to 9	$P0B_3$ to $P0B_0$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
10 to 13	$P0A_3$ to $P0A_0$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
14	GND	Ground	–	–
15	INT	Input of external interrupt requests and release of standby mode	–	Input
16	$\overline{RESET}$	System reset input pin	–	Input
17	$P1B_0$	Port 1B • 1-bit input port • Pull-up resistor incorporation specifiable by mask option	Input	Input
18 to 21	$P1A_3$ to $P1A_0$	Port 1A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input
22	$P0D_3/\overline{TM0OUT}$	Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input/output. • $P0D_3$ to $P0D_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{TM0OUT}$ · Timer 0 carry output	N-ch open-drain	Input
23	$P0D_2$/SI	• SI · Serial data input		
24	$P0D_1$/SO	• SO · Serial data output		
25	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ · Serial clock input/output		
26 27	X_{OUT} X_{IN}	For system clock oscillation. The ceramic resonator is connected.	–	–
28	V_{DD}	Power supply	–	–

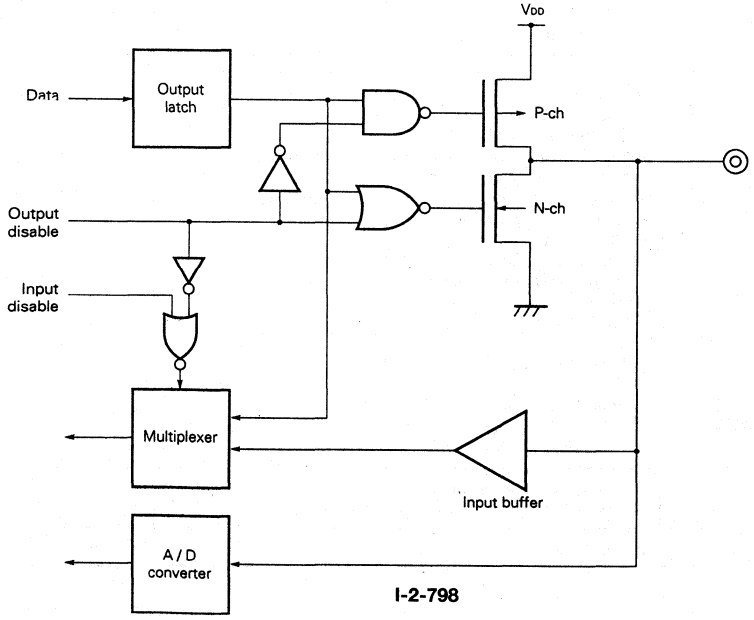
1.2 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

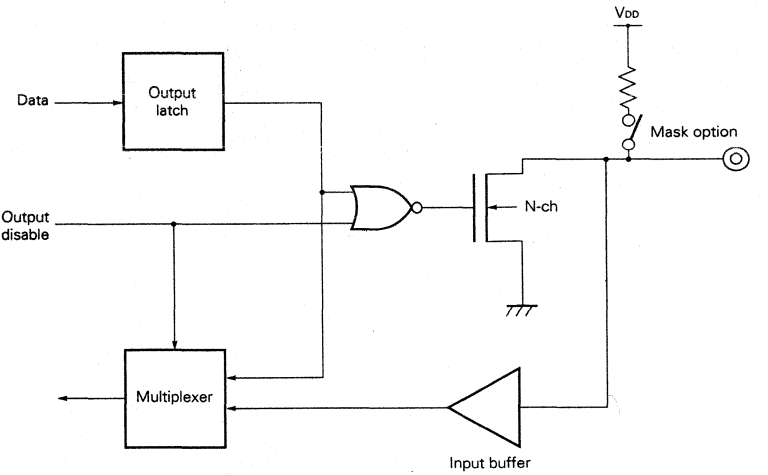
(1) $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$



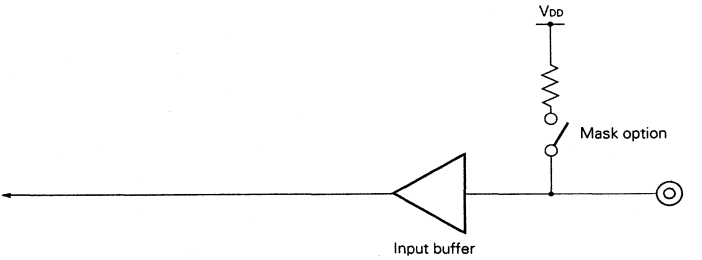
(2) $P0C_0$/ADC_0 to $P0C_3$/ADC_3



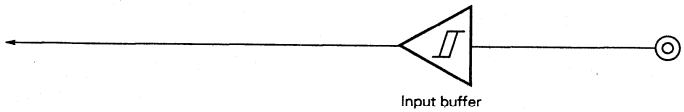
(3) $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_3$



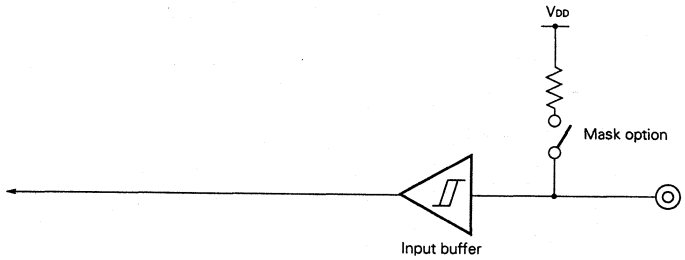
(4) $P1B_0$



(5) INT



(6) $\overline{\text{RESET}}$



1.3 HANDLING UNUSED PINS

To prevent malfunctions, connect the unused pins as follows:

Table 1-1 Handling Unused Pins

Pin			Handling
Port[Note 1]	Input mode	P0A, P0B, P0C, P0D, P1A, P1B0	To be connected to the V_{DD} or GND pin
	Output mode	P0A, P0B, P0C (CMOS port)	Open
		P0D, P0A (N-ch open-drain port)	Open (0s are output on the pins.)
INT			To be connected to the V_{DD} or GND pin
V_{ADC}			To be connected to the V_{DD} pin[Note 2]

Note 1. When a pull-up resistor is not incorporated.

2. Connect the V_{ADC} pin to the V_{DD} pin even when the A/D converter is not used.

22. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			–0.3 to +7.0	V
Analog Supply Voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V		–0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$ X_{IN}, X_{OUT}		–0.3 to V_{DD}+0.3	V
		P0D, P1A	**Note 1**	–0.3 to V_{DD}+0.3	
			Note 2	–0.3 to +11.0	
Output Voltage	V_O	P0A, P0B, P0C		–0.3 to V_{DD}+0.3	V
		P0D, P1A	**Note 1**	–0.3 to V_{DD}+0.3	
			Note 2	–0.3 to +11.0	
High-Level Output Current	I_{OH}	Each of P0A, P0B, and P0C		–15	mA
		Total of all pins		–30	
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C and P1B		15	mA
		Each of P0D and P1A		30	
		Total of all pins		100	
Operating Temperature	T_{opt}			–40 to +85	°C
Storage Temperature	T_{stg}			–65 to +150	°C
Power Dissipation	P_d	T_a = 85 °C		180	mW

Note 1. When a built-in pull-up resistor is selected as mask option

2. When N-ch open-drain input/output is selected

RECOMMENDED POWER VOLTAGE RANGE (T_a = –40 to +85 °C)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CPU Note 3	2.7		5.5	V	Oscillator frequency: fx = 400 kHz to 4 MHz
	4.5		5.5	V	Oscillator frequency: fx = 400 kHz to 8 MHz
A/D Converter	4.5		5.5	V	Absolute accuracy: ±1.5 LSB or less
Zerocross Detection Circuit	4.5		5.5	V	Zerocross accuracy: Azx = ±120 mV or less
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (from 0 to 2.7 V): 8192 x 16/fx or less (fx = 400 kHz to 4 MHz)

Note 3. Excluding the A/D converter, zerocross detection circuit, and power-on/power-down reset circuits

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, Ta = -40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0D, P1A	**Note 1**
				9			**Note 2**
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $\overline{SCK}$, SI, INT	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P1A, $\overline{RESET}$, $\overline{SCK}$, SI, INT	
High-Level Output Voltage	V_{OH}			V_{DD}–0.3	V	P0A, P0B, P0C[Note 3]	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1.0 mA
				V_{DD}–0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OH} = –0.5 mA
Low-Level Output Voltage	V_{OL1}			0.3	V	P0A, P0B, P0C, P0D, P1A [Note 3]	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA
				0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA
	V_{OL2}			1.0	V	P0D, P1A, I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V
				2.0	V		V_{DD} = 2.7 to 4.5 V
High-Level Input Leakage Current	I_{LIH1}			3	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	P0D, P1A, V_{IN} = 9V [Note 2]	
Low-Level Input Leakage Current	I_{LIL}			–5	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			3	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	P0D, P1A, V_{OUT} = 9 V [Note 2]	
Low-Level Output Leakage Current	I_{LOL}			–5	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = 0 V	
Built-In Pull-Up Resistor	R_{PULL}	50	100	200	kΩ	P0A, P1B, P1B, $\overline{RESET}$	

Note 1. When a built-in pull-up resistor is selected as mask option

2. When N-ch open-drain input/output is selected

3. When a built-in pull-up resistor is not selected by the software

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Power Supply Current [Note]	I_{DD1}		2.0	4.5	mA	Operation mode	f_X = 8.0 MHz V_{DD}=5 V ±10 %
			1.3	3.0	mA		f_X = 4.0 MHz V_{DD}=5 V±10 %
			0.5	1.5	mA		f_X = 2.0 MHz V_{DD}=3 V±10 %
			0.9	1.5	mA	f_X = 455 kHz	V_{DD} = 5 V ±10 %
			0.3	1.0	mA		V_{DD} = 3 V ±10 %
	I_{DD2}		1.0	2.0	mA	HALT mode	f_X = 8.0 MHz V_{DD} = 5 V ±10 %
			0.7	1.5	mA		f_X = 4.0 MHz V_{DD} = 5 V±10 %
			0.3	1.0	mA		f_X = 2.0 MHz V_{DD}= 3 V ±10 %
			0.7	1.2	mA	f_X = 455 kHz	V_{DD} = 5 V±10 %
			0.3	0.9	mA		V_{DD} = 3 V ±10 %
	I_{DD3}		3.0	10	μA	STOP mode	V_{DD} = 5 V ±10 %
			2.0	10	μA		V_{DD} = 3 V ±10 %

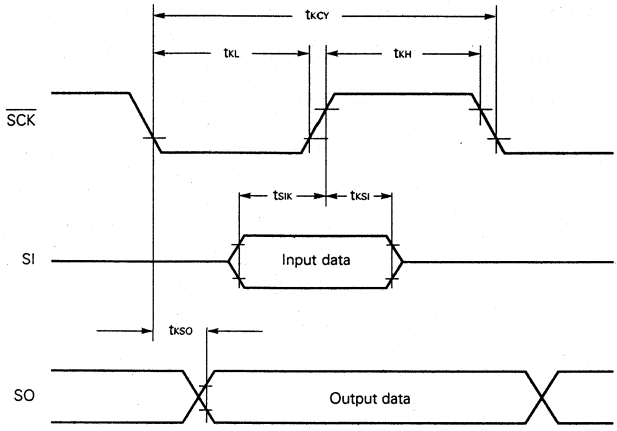
Note When neither the A/D converter nor zero cross detection circuit is used, the current which flows through the built-in pull-up resistor is excluded.

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

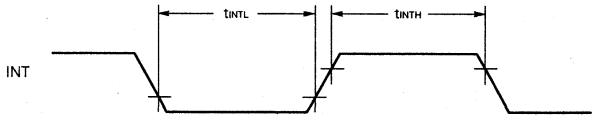
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Internal Clock Cycle Time	t_{CY}	1.9		41	μs	V_{DD} = 4.5 to 5.5 V	
		3.9		41	μs		
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		16			μs		Output
		10			μs		Input
		32			μs		Output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		t_{KCY}/2-6			μs		Output
		5.0			μs		Input
		t_{KCY}/2-12			μs		Output
SI Setup Time (Referred to $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI Hold Time (Referred to $\overline{SCK}$↑)	t_{KSI}	100			ns		
SO Output Delay Time (Referred to $\overline{SCK}$↓)	t_{KSO}			4.5	μs		
Interrupt Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	VDD = 4.5 to 5.5 V	
		50			μs		
$\overline{RESET}$ Low Level Width	t_{REL}	10			μs	VDD = 4.5 to 5.5 V	
		50			μs		

Remark t_{CY} = 16/fx (fx: frequency of system clock oscillator)

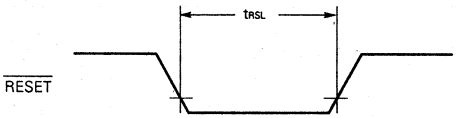
Serial transfer timing



Interrupt input timing

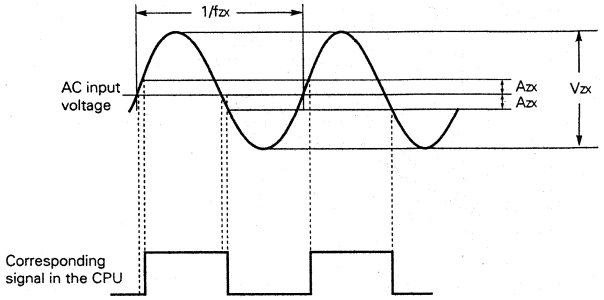


$\overline{\text{RESET}}$ input timing



ZEROCROSS DETECTION INPUT CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V_{P-P}	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	fzx	40	50 or 60	1000	Hz	
Zerocross Accuracy	Azx		40	±120	mV	50 Hz or 60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by Azx in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C, V_{ADC} = V_{DD} ±0.5 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		8	8	8	bit	
Absolute Accuracy Note1				±1.5	LSB	V_{ADC} = V_{DD}
ADC Circuit Current	I_{ADC}		1.5	2.0	mA	
Conversion Time Note 2	t_{CONV}			400/fx	s	

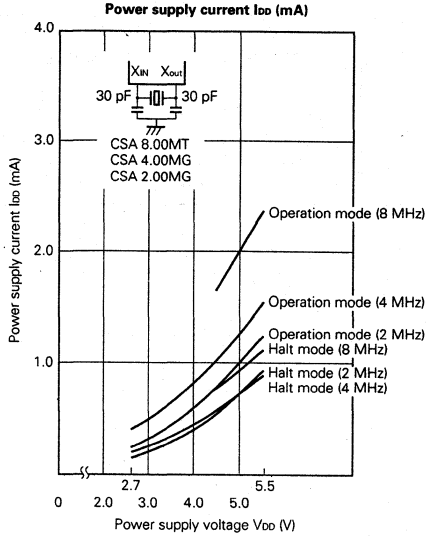
Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)
2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at fx = 2 MHz, 200 μs)

CHARACTERISTICS OF THE POWER-ON/POWER-DOWN RESET CIRCUITS (T_a = −40 to +85 °C)

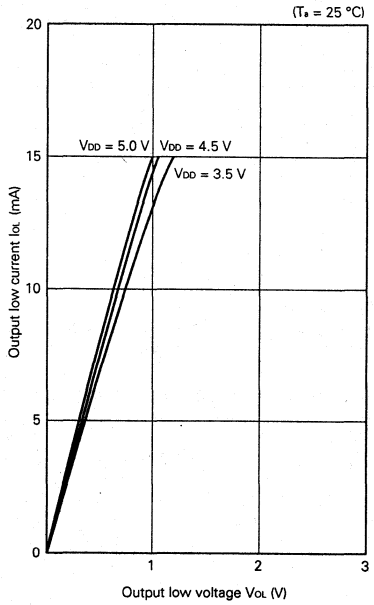
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Time It Takes for the Power to Rise to the Voltage Level That Enables Power- On Reset	t_{POR}			8192 x 16/fx	s	V_{DD} = 0 → 2.7 The power voltage (V_{DD}) must change from ground level to 2.7 V. fx = 400 kHz to 4 MHz
Low Voltage to be Detected by the Power-Down Reset Circuit	V_{PDR}		3.5	4.5	V	When PDRESEN = 1 fx = 400 kHz to 4 MHz

23. CHARACTERISTIC CURVES (FOR REFERENCE)

Power supply current I_{DD} (mA)

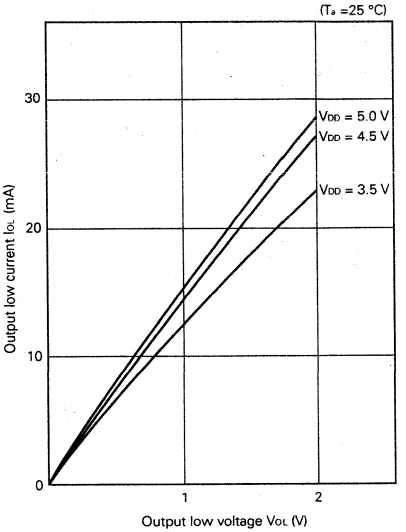


I_{OL} vs V_{OL} (P0A, P0B, P0C, P1B)



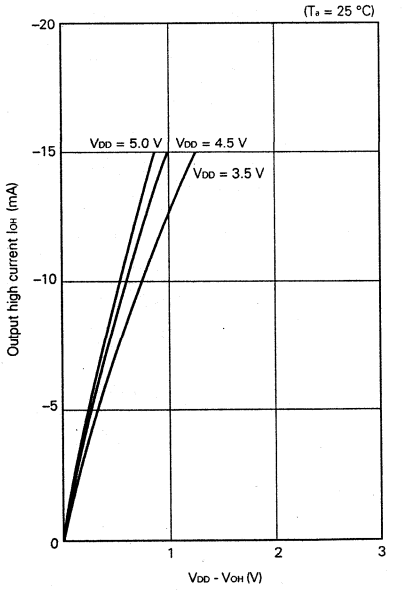
Note Absolute maximum rating of output current is 15 mA per pin.

I_{OL} vs V_{OL} (P0D, P1A)



Note Absolute maximum rating of output current is 30 mA per pin.

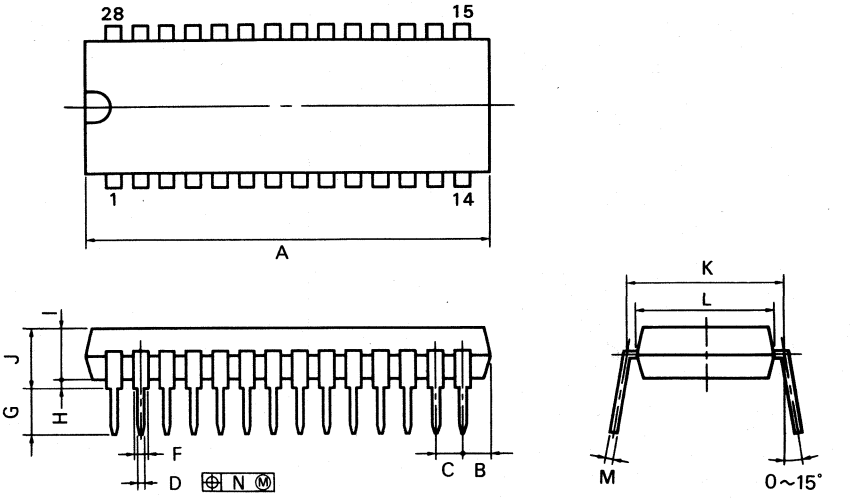
I_{OH} vs (V_{DD}- V_{OH})



Note Absolute maximum rating of output current is -15 mA pert pin

24. PACKAGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

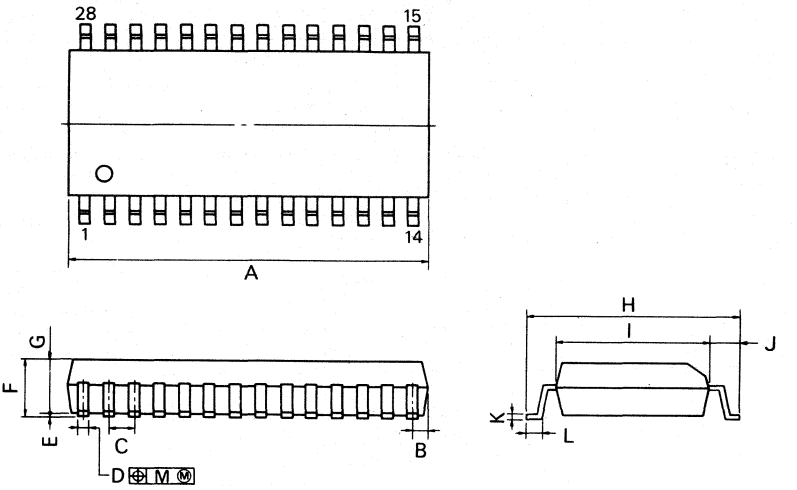
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

25. MICROCONTROLLER FUNCTION FOR SMALL HOME ELECTRIC APPLIANCES

Item	μPD17134A	μPD17135A	μPD17136A	μPD17137A	Remarks
ROM Size	1024 x 16 bits		2048 x 16 bits		
RAM Size	112 x 4 bits				
Number of I/O Port Lines	22 lines (including one input line and one sense input line)				Including 8 N-ch open drain lines
A/D Converter Input	4 channels				Also used as port pins
Timer	3 timers				8 bits: 2 channels, 7 bits: 1 channel (Basic interval timers)
Serial Interface	1 channel				Also used as port pin
Stack	5 levels				
Power-On/Power-Down Reset	Provided (valid only when V_{DD} = 5 V ±10 %)				
System Clock	RC oscillation	Ceramic/ crystal oscillation	RC oscillation	Ceramic/ crystal oscillation	
Instruction Execution Time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby Function	Provided				STOP/HALT
Power Supply	2.7 to 5.5 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
One Time PROM Product	μPD17P136A	μPD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output

26. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) shall be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 26-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17135ACT-xxx	28-pin plastic shrink DIP (400 mil)	• Wave soldering • Partial heating method
μPD17135AGT-xxx	28-pin plastic SOP (375 mil)	• IR30-00 • VP15-00 • WS60-00 • Partial heating method

Table 26-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30-00	Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or below (210 °C or higher) Number of reflow processes: 1
VP15-00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow processes: 1
WS60-00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow processes: 1
Partial heating method	Terminal to be heated	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

Remark For details of the recommended soldering conditions, refer to our document **"SMT Manual" (IEI-1207)**

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES
4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17137A is a 4-bit single-chip microcontroller containing an 8-bit A/D converter (4 channels), 3 timers, an AC zerocross detector, a power-on reset circuit, and a serial interface.

For the CPU, the μPD17137A employs a 17K architecture using general registers. The new architecture allows operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (1 word) long, allowing programming to be done efficiently.

Since the μPD17137A has on-chip A/D converters and an AC zerocross detector, it is suitable for electronic control of electric home appliances. The μPD17137A, a one-time PROM product (can be written to only once) is available for evaluation of the μPD17135A and μPD17137A and for small-scale production.

FEATURES

- 17K architecture : General registers
- Program memory (ROM) : 2048 x 16 bits
- Data memory (RAM) : 112 x 4 bits
- Instruction execution time : 2 μs (at 8 MHz: Ceramic oscillation)
- 8-bit A/D convertor : 4 channels
  Absolute accuracy: ±1.5 LSB or lower (V_{DD} = 5 V ±10 %)
- Timer function : 3 channels
- 3-wire serial interface : 1 channel
- Input/output pins : 22 pins (including 1 general input pin and 1 sensor input pin)
- Power-on/power-down reset circuit : V_{DD} = 5 V ±10 % (at 400 kHz to 4 MHz)
- Operates on low voltage : V_{DD} = 2.7 to 5.5 V

ORDERING INFORMATION

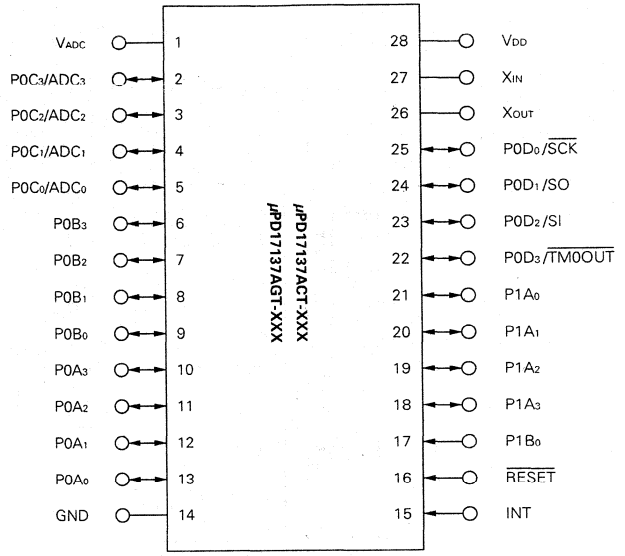
Order Code	Package	Quality Grade
μPD17137ACT-xxx	28-pin plastic shrink DIP (400 mil)	Standard
μPDI7137AGT-xxx	28-pin plastic SOP (375 mil)	Standard

CHARACTERISTICS OF μPD17137A

Item	Description
ROM	2048 x 16 bits
RAM	112 x 4 bits (The stack is separated from data memory.)
Stack	5 address stacks, 3 interrupt stacks
Number of I/O ports	22 { • 20 I/O ports • 1 general input port • 1 input port for sensing an interrupt or AC zero-cross
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ± 1.5 LSB or less at a power voltage of 5 V ± 10 %
Timer	3 channels { • 2 channels for 8-bit timers (They can be used together as one 16-bit timer.) • 1 channel for a 7-bit basic interval timer (can be used as a watchdog timer.)
Serial interface	1 channel (3-wire type)
Interrupt	• Up to 3 levels of multiple hardware interrupts • 1 external interrupt { • Shared with the input from the AC zerocross detection circuit • Rising-edge detection, falling edge detection • Detection of the rising edge, falling edge, or both edges can be selected with the sense input • 4 internal interrupts { • Timer 0 • Timer 1 • Basic interval timer • Serial interface
Execution time of an instruction	2 μs at 8 MHz clock, ceramic oscillation
Standby function	STOP/HALT
Operating power voltage	• 2.7 to 5.5 V • 4.5 to 5.5 V (When the power-on/power-down reset functions are used)
Package	• 28-pin plastic shrink DIP • 28-pin plastic SOP
One-time PROM	μPD17P137A

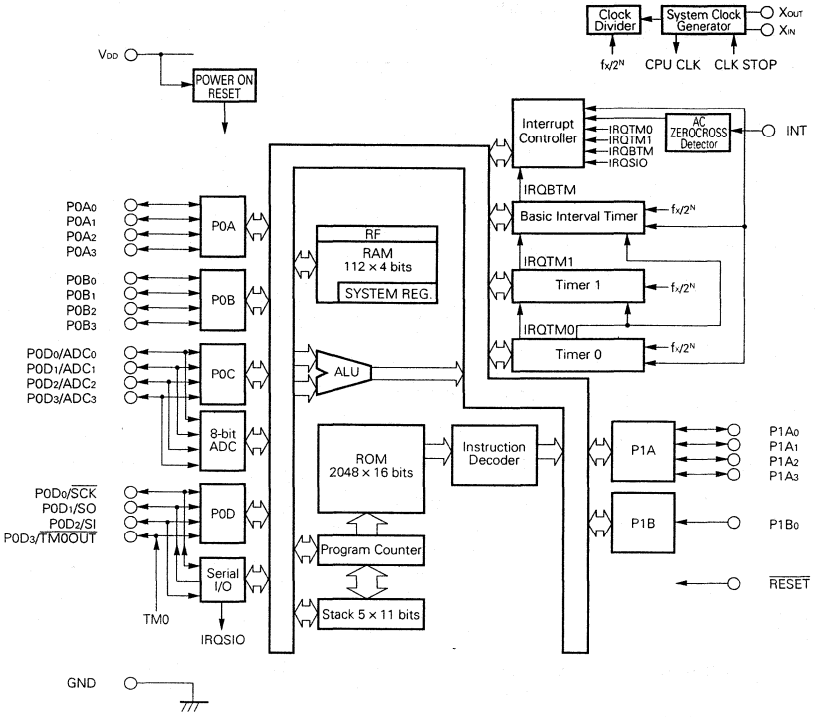
PIN CONFIGURATION (Top View)

28-PIN PLASTIC SHRINK DIP
28-PIN PLASTIC SOP



ADC0-ADC3:	Analog input
RESET:	Reset input
Tm0OUT:	Timer 0 carry output
INT:	External interrupt input
SI:	Serial data input
SO:	Serial data output
SCK:	Serial clock input/output
XIN, XOUT:	System clock oscillation
P0A0-P0A3:	Port 0A
B0B0-P0B3:	Port 0B
P0C0-P0C3:	Port 0C
P0D0-P0D3:	Port 0D
P1A0-P1A3:	Port 1A
P1B0:	Port 1B
VADC:	Analog power supply
VDD:	Power supply
GND:	Ground

BLOCK DIAGRAM



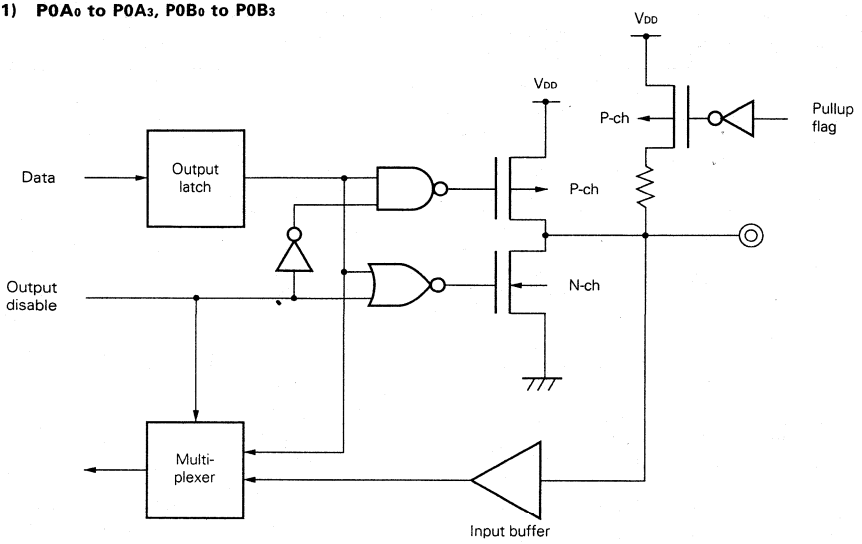
1.1 PIN FUNCTIONS

PIN NO.	Pin name	Function	Output	After power-on or set
1	V_{ADC}	Power voltage for the A/D converter and for the circuit generating reference voltage	Input	—
2 to 5	$P0C_3/ADC_3$ to $P0C_0/ADC_0$	Pin for port OC and A/D converter • $P0C_3$ to $P0C_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • ADC_3 to ADC_0 · Analog input for the A/D converter	CMOS push-pull	Input (P0C)
6 to 9	$P0B_3$ to $P0B_0$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
10 to 13	$P0A_3$ to $P0A_0$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
14	GND	Ground	—	—
15	INT.	Input of external interrupt requests and release of standby mode	Input	Input
16	$\overline{RESET}$	System reset input pin	Input	Input
17	$P1B_0$	Port 1B • 1-bit input/output port • Pull-up resistor incorporation specifiable by mask option	Input	Input
18 to 21	$P1A_3$ to $P1A_0$	Port 1A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input
22	$P0D_3/\overline{TM0OUT}$	Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input/output. • $P0D_3$ to $P0D_0$ · 4-bit input/output port · Input/output setting allowed in units of 1 bit • $\overline{TM0OUT}$ · Timer 0 carry output	N-ch open-drain	Input
23	$P0D_2/SI$	• SI · Serial data input		
24	$P0D_1/SO$	• SO · Serial data output		
25	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ · Serial clock input/output		
26 27	X_{OUT} X_{IN}	For system clock oscillation. The ceramic resonator is connected.	—	—
28	V_{DD}	Power supply	—	—

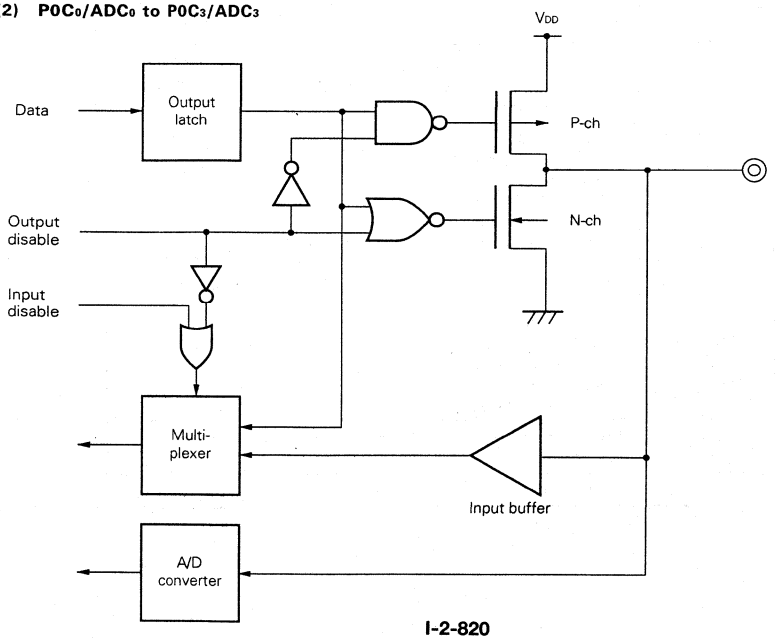
1.2 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

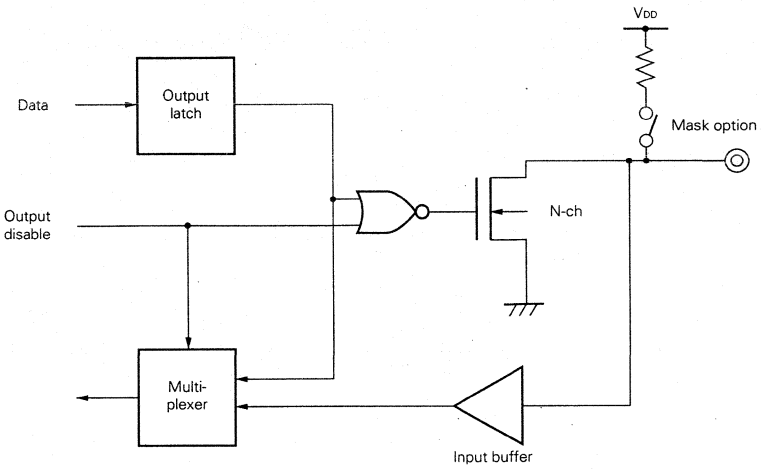
(1) $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$



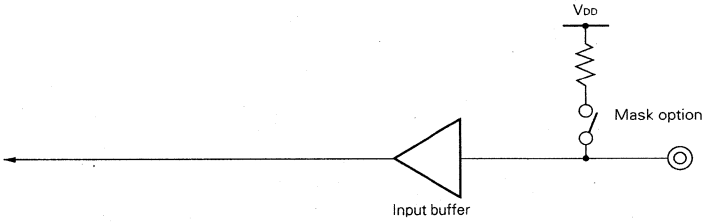
(2) $P0C_0/ADC_0$ to $P0C_3/ADC_3$



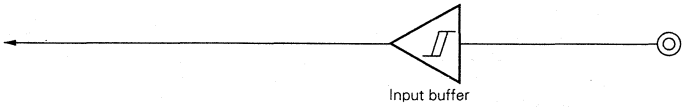
(3) $P0D_0$ to $P0D3$, $P1A_0$ to $P1A_3$



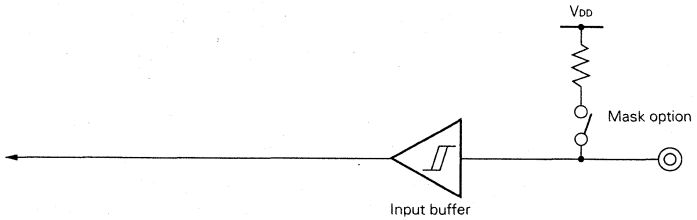
(4) $P1B_0$



(5) INT



(6) $\overline{\text{RESET}}$



1.3 HANDLING UNUSED PINS

To prevent malfunctions, connect the unused pins as follows:

Table 1-1 Handling Unused Pins

Pin			Handling
Port Note 1	Input mode	P0A, P0B, P0C, P0D, P1A, P1B0	To be connected to the V_{DD} or GND pin
	Output mode	P0A, P0B, P0C (CMOS port)	Open
		P0D, P1A (N-ch open-drain port)	Open (0s are output on the pins.)
INT			To be connected to the V_{DD} or GND pin
V_{ADC}			To be connected to the V_{DD} pin Note 2

Note 1. When a pull-up resistor is not incorporated.

2. Connect the V_{ADC} pin to the V_{DD} pin even when the A/D converter is not used.

22. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

ABSOLUTE MAXIMUM RATING (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS		RATING	UNIT
Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V		−0.3 to +7.0	V
Input Voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$, X_{IN}, X_{OUT}		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} +0.3	
			Note 2	−0.3 to +11	
Output Voltage	V_O	P0A, P0B, P0C		−0.3 to V_{DD} +0.3	V
		P0D, P1A	**Note 1**	−0.3 to V_{DD} +0.3	
			Note 2	−0.3 to +11.0	
High-Level Output Current	I_{OH}	Each of P0A, P0B, and P0C		−15	mA
		Total of all pins		−30	
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, and P1B		15	mA
		Each of P0D and P1A		30	
		Total of all pins		100	
Operating Temperature	T_{opt}			−40 to +85	°C
Storage Temperature	T_{stg}			−65 to +150	°C
Power Dissipation	P_d	T_a = 85°C		180	mW

Note 1. When a built-in pull-up resistor is selected as mask option.
2. When N-ch open-drain input/output is selected.

RECOMMENDED POWER VOLTAGE RANGE (T_a = −40 to +85 °C)

CHARACTERISTICS	MIN	TYP.	MAX.	UNIT	CONDITIONS
CPU **Note**	2.7		5.5	V	Oscillatior frequency: f_X = 400 kHz to 4 MHz
	4.5		5.5	V	Oscillator frequency: f_X = 400 kHz to 8 MHz
A/D Converter	4.5		5.5	V	Absolute accuracy: ±1.5 LSB or less
Zerocross Detection Circuit	4.5		5.5	V	Zerocoross accuracy: A_{ZX} = ±120 mV or less
Power-On/Power-Down Reset Circuit	4.5		5.5	V	Rising time of the power voltage (from 0 to 2.7 V): 8192 x 16/f_X or less

Note Excluding the A/D converter, zerocross detection circuit, and power-on/power-down reset circuits.

DC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0D, P1A	**Note 1**
				9			**Note 2**
	V_{IH3}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $\overline{SCK}$, SI, INT	
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B	
	V_{IL2}	0		0.2 V_{DD}	V	P0D, P1A, $\overline{RESET}$, $\overline{SCK}$, SI, INT	
High-Level Output Voltage	V_{OH}			V_{DD} −0.3	V	P0A, P0B, P0C **Note 3**	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1.0 mA
				V_{DD} −0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OH} = −0.5 mA
Low-Level Output Voltage	V_{OL1}			0.3	V	P0A, P0B, P0C, P0D, P1A **Note 3**	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA
				0.3	V		V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA
	V_{OL2}			1.0	V	P0D, P1A I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V
				2.0	V		V_{DD} = 2.7 to 4.5 V
High-Level Input Leakage Current	I_{LIH1}			3	μA	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = V_{DD}	
	I_{LIH2}			10	μA	P0D, P1A, V_{IN} = 9 V **Note 2**	
Low-Level Input Leakage Current	I_{LIL}			−5	μA	P0A, P0B, P0C, P0D, P1A, P0B, V_{IN} = 0 V	
High-Level Output Leakage Current	I_{LOH1}			3	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = V_{DD}	
	I_{LOH2}			10	μA	P0D, P1A, V_{OUT} = 9 V **Note 2**	
Low-Level Input Leakage Current	I_{LOL}			−5	μA	P0A, P0B, P0C, P0D, P1A, V_{OUT} = 0 V	
Built-in Pull-Up Resistor	R_{PULL}	50	100	200	kΩ	P0A, P0B, P1B, $\overline{RESET}$	

Note 1. When a built-in pull-up resistor is selected as the mask option.

2. When N-ch open-drain input/output is selected.

3. When a built-in pull-up resistor is not selected by the software.

CHARACTERISTICS	SYMBOL	MIN	TYP.	MAX.	UNIT	CONDITIONS		
Power Supply Current [Note]	I_{DD1}		2.0	4.5	mA	Operation mode	f_X = 8.0 MHz V_{DD} = 5 V ±10 %	
			1.3	3.0	mA		f_X = 4.0 MHz V_{DD} = 5 V ±10 %	
			0.5	1.5	mA		f_X = 2.0 MHz V_{DD} = 3 V ±10 %	
			0.9	1.5	mA		f_X = 455 kHz	V_{DD} = 5 V ±10 %
			0.3	1.0	mA			V_{DD} = 3 V ±10 %
	I_{DD2}		1.0	2.0	mA	HALT mode	f_X = 8.0 MHz	V_{DD} = 5 V ±10 %
			0.7	1.5	mA		f_X = 4.0 MHz	V_{DD} = 5 V ±10 %
			0.3	1.0	mA		f_X = 2.0 MHz	V_{DD} = 3 V ±10 %
			0.7	1.2	mA		f_X = 455 kHz	V_{DD} = 5 V ±10 %
			0.3	0.9	mA			V_{DD} = 3 V ±10 %
	I_{DD3}		3.0	10	μA	STOP mode	V_{DD} = 5 V ±10 %	
			2.0	10	μA		V_{DD} = 3 V ±10 %	

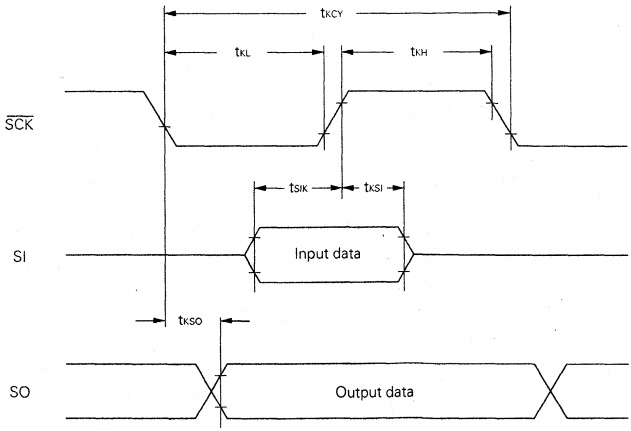
Note When neither the A/D converter nor zerocross detection circuit is used, and excluding the current which flows through the built-in pull-up resistor

AC CHARACTERISTICS (V_{DD} = 2.7 to 5.5 V, T_a = −40 to +85 °C)

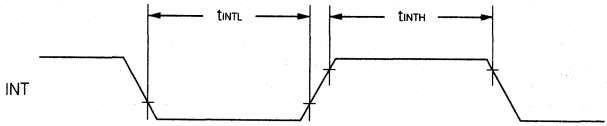
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Internal Clock Cycle Time	t_{CY}	6.6		41	μs	V_{DD} = 4.5 to 5.5 V	
		3.9		41	μs		
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		16			μs		Output
		10			μs		Input
		32			μs		Output
$\overline{SCK}$ Hgh/Low Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 4.5 to 5.5 V	Input
		t_{KCY}/2-6			μs		output
		5.0			μs		Input
		t_{KCY}/2-12			μs		Output
SI Setup Time (Referred to $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI Hold Time (Referred to $\overline{SCK}$↑)	t_{KSI}	100			ns		
SO Output Delay Time (Referred to $\overline{SCK}$↓)	t_{KSO}			4.5	μs		
Interrupt Input High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μs	V_{DD} = 4.5 to 5.5 V	
		50			μs		

Remark t_{CY} = 16/f_X (f_X: Frequency of system clock oscillator)

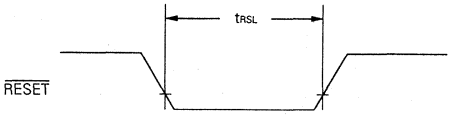
SERIAL TRANSFER TIMING



INTERRUPT INPUT TIMING

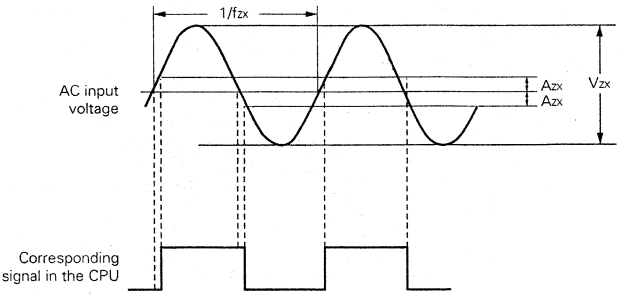


$\overline{\text{RESET}}$ INPUT TIMING



ZEROCROSS DETECTION INPUT CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to +85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V_{P-P}	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	f_{ZX}	40	50 or 60	1000	Hz	
Zerocross Accuracy	A_{ZX}		40	±120	mV	50 Hz or 60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by A_{ZX} in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_a = −40 to 85 °C, V_{ADC} = V_{DD} ±0.5 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Resolution		8	8	8	bit	
Absolute accuracy Note 1				±1.5	LSB	V_{ADC} = V_{DD}
ADC circuit current	I_{ADC}		1.5	2.0	mA	
Conversion time Note 2	t_{CONV}			400/fx	s	

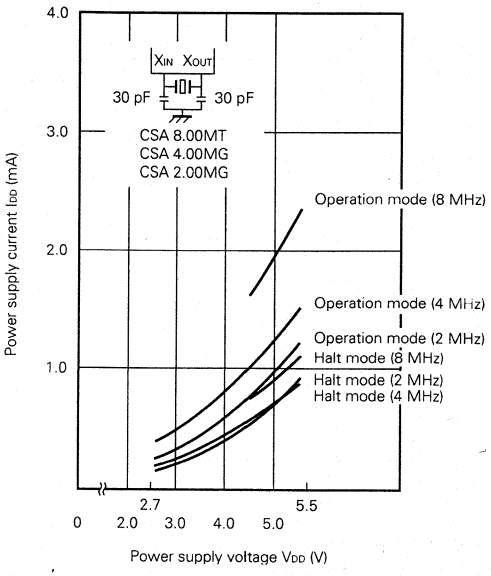
Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at fx = 8 MHz, 50 μs)

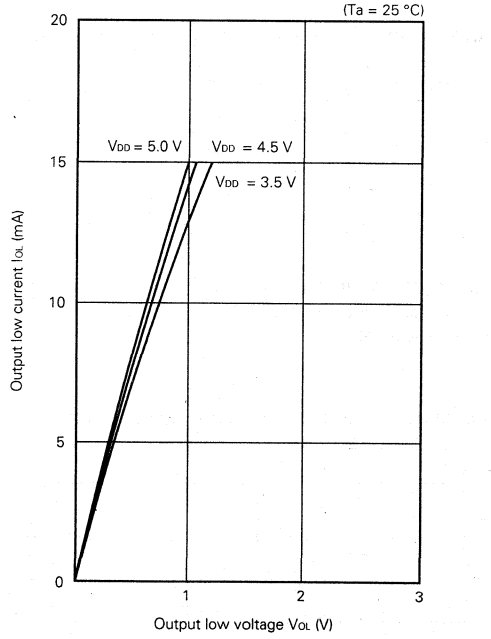
CHARACTERISTICS OF THE POWER-ON AND POWER-DOWN RESET CIRCUITS (T_a = −40 to 85 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Time it takes for the power to rise to the voltage level that enables power-on reset	t_{PORT}			8192 x 16/fx	s	The power voltage (V_{DD}) must change from ground level to 2.7 V. fx = 400 kHz to 4 MHz
Low voltage to be detected by the power-down reset circuit	V_{PDR}		3.5	4.5	V	When PDRESETN = 1 fx = 400 kHz to 4 MHz

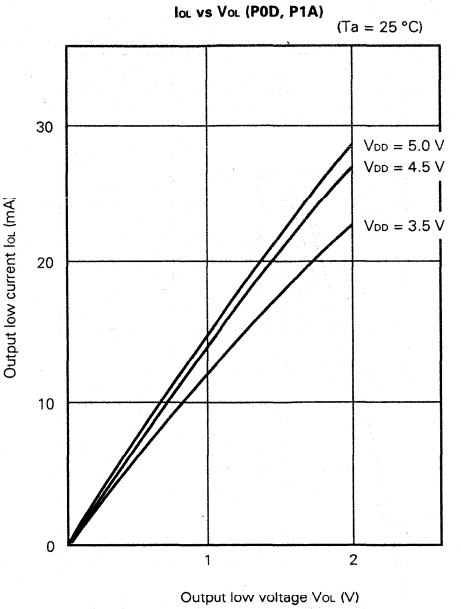
23. CHARACTERISTIC CURVES (FOR REFERENCE)



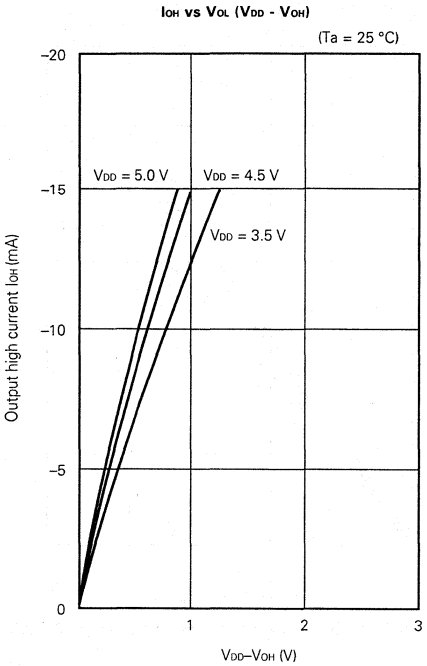
IOL vs VOL (P0A, P0B, P0C, P1B)



Note Absolute maximum rating of output current is 15 mA per pin.



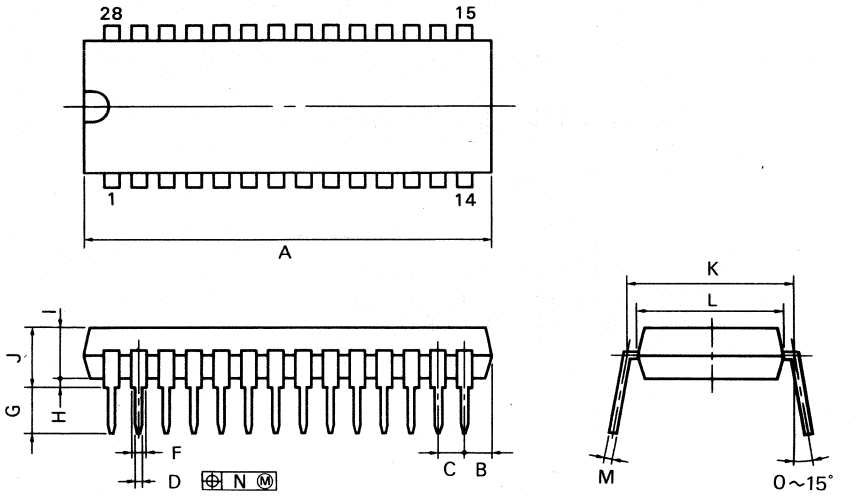
Note Absolute maximum rating of output current is 30 mA per pin.



Note Absolute maximum rating of output current is -15 mA per pin.

24. PACKAGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

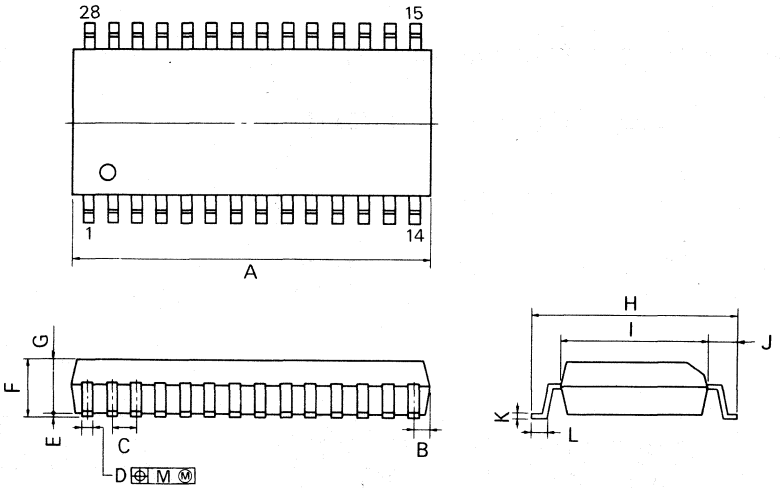
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

25. MICROCONTROLLER FUNCTIONS FOR SMALL HOME ELECTRIC APPLIANCES

A/D converter	μPD17134A	μPD17135A	μPD17136A	μPD17137A	Remarks
ROM Size	1024 x 16 bits		2048 x 16 bits		
RAM Size	112 x 4 bits				
Number of I/O Port Lines	22 lines (including one input line and one sense input line)				Including 8 N-ch open drain lines
A/D Converter Input	4 channels				Also used as port pin
Timer	3 timers				8 bits: 2 channels, 7 bits: 1 channel (basic interval timers)
Serial Interface	1 channel				Also used as port pin
Stack	5 levels				
Power-On Power-Down Reset	Provided (valid only when V_{DD} = 5 V ±10 %)				
System Clock	RC oscillation	Ceramic/crystal oscillation	RC oscillation	Ceramic/crystal oscillation	
Instruction Execution Time	8 μs at 2 MHz	2 μs at 8 MHz	8 μs at 2 MHz	2 μs at 8 MHz	
Standby Function	Provided				STOP/HALT
Power Supply	2.7 to 5.5 V				5 V ±10 % for A/D
Package	28-pin shrink DIP 28-pin SOP				
One Time PROM Product	μPD17P136A	μPD17P137A	μPD17P136A	μPD17P137A	

I/O: Input/output.

26. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) shall be met when soldering the μPD17137A.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 26-1 Recommended Soldering Conditions

Product	Package	Symbol
μPD17137ACT-xxx	28-pin plastic shrink DIP (400 mil)	• When soldering • Partial heating method
μPD17137AGT-xxx	28-pin plastic SOP (375 mil)	• IR30–00 • VP15–00 • WS60–00 • Partial heating method

Table 26-2 Soldering Conditions

Symbol	Soldering process	Soldering conditions
IR30–00	Infrared ray reflow	Peak package's surface temperature: 230 °V Reflow time: 30 seconds or below (210 °C or higher) Number of reflow processes: 1
VP15–00	VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or below (200 °C or higher) Number of reflow processes: 1
WS60–00	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below Number of flow processes: 1
Partial heating method	Terminal to be heated	Terminal temperature: 300 °C or below Flow time: 10 seconds or below
Wave soldering	Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below

Caution **Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).**

Remark For details of the recommended soldering conditions, refer to our document **"SMT Manual" (IEI–1207).**

MICROCONTROLLER FOR SMALL HOME ELECTRIC APPLIANCES 4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P137A is a one-time PROM version of the μPD17137A, in which the internal mask ROM of the μPD17137A is replaced with a one-time PROM that can be written to just once.

Since a user program can be written on the PROM, this microcontroller is suited for trial manufacture during μPD17135A, μPD17137A system development, or multiple device production.

The reader also should refer to the publications on the μPD17137A.

FEATURES

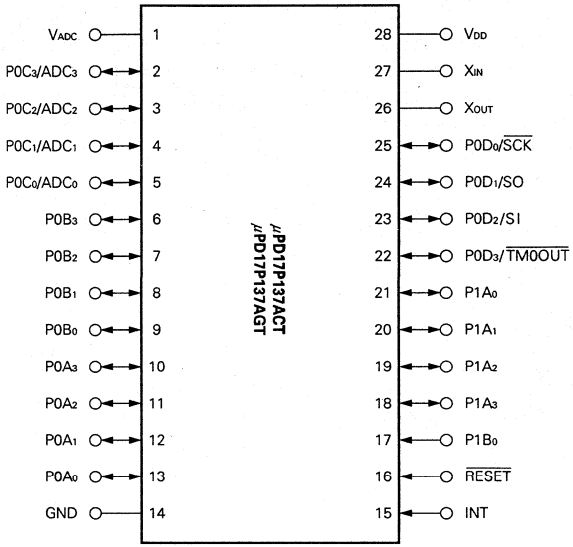
- Pin compatible with the μPD17137A (except for PROM programming function)
- Internal one-time PROM : 2048 × 16 bits
- Operating supply voltage : 2.7 to 5.5 V

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P137ACT	28-pin plastic shrink DIP (400 mil)	Standard
μPD17P137AGT	28-pin plastic SOP (375 mil)	Standard

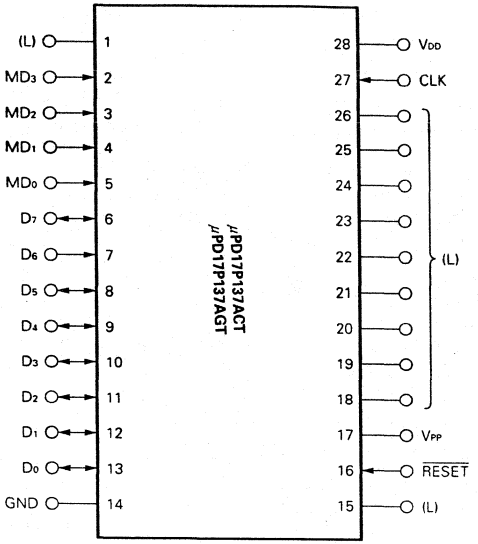
PIN CONFIGURATION (Top View)

(1) Normal operating mode



ADC0-ADC3	:	Analog input for A/D converters	P0D0-P0D3	:	Port 0D
RESET	:	Reset input	P1A0-P1A3	:	Port 1A
TM0OUT	:	Timer 0 carry output	P1B0	:	Port 1B
INT	:	External interrupt input	CLK	:	Clock input for address update
SI	:	Serial data input	MD0-MD3	:	Operating mode selection
SO	:	Serial data output	D0-D7	:	Data input/output
SCK	:	Serial clock input/output	VADC	:	Analog power supply
XIN, XOUT	:	System clock oscillation	VPP	:	Program voltage
P0A0-P0A3	:	Port 0A	VDD	:	Positive power supply
P0B0-P0B3	:	Port 0B	GND	:	Ground
P0C0-P0C3	:	Port 0C			

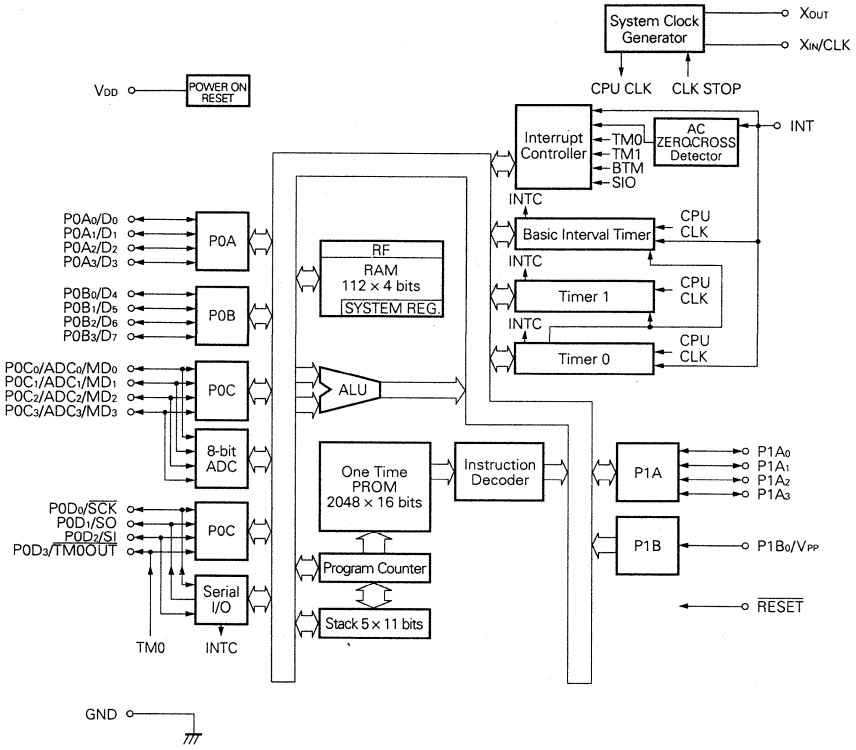
(2) Program memory write/verify mode



Cautions **Symbols in parentheses denote the processing for the pins not to be used in the program memory write/verify mode.**

L: Connect these pins separately to the GND pin through pull-down resistors.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT	AFTER POWER-ON OR RESET
1	V_{ADC}	Power for the A/D converter	–	–
2	$P0C_3/ADC_3$	Pin for port 0C and A/D converter • $P0C_3$ - $P0C_0$ • 4-bit input/output port • Input/output setting allowed in units of 1 bit • ADC_3 - ADC_0 • Analog input for the A/D converter	CMOS push-pull	Input (P0C)
|	|			
5	$P0C_0/ADC_0$			
6	$P0B_3$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0B)
|	|			
9	$P0B_0$			
10	$P0A_3$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program	CMOS push-pull	Input (P0A)
|	|			
13	$P0A_0$			
14	GND	Ground	–	–
15	INT	Input of external interrupt requests and release of standby mode	–	–
16	$\overline{RESET}$	System reset input pin	–	–
17	$P1B_0$	Port 1B • 1-bit input/output port • Pull-up resistor incorporation specifiable by mask option	–	Input
18	$P1A_3$	Port 1A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by mask option	N-ch open-drain	Input
|	|			
21	$P1A_0$			

PIN No.	SYMBOL	FUNCTION	OUTPUT	AFTER POWER-ON OR RESET
22 23 24 25	$P0D_3/\overline{TM0OUT}$ $P0D_2/SI$ $P0D_1/SO$ $P0D_0/\overline{SCK}$	Pin for port 0D, timer 0 carry output, serial data input, serial data output, and serial clock input/output. • $P0D_3$ - $P0D_0$ • 4-bit input/output port • Input/output setting allowed in units of 1 bit • $\overline{TM0OUT}$ • Timer 0 carry output • SI • Serial data input • SO • Serial data output • $\overline{SCK}$ • Serial clock input/output	N-ch open-drain	Input
26 27	X_{OUT} X_{IN}	For system clock oscillation. For ceramic oscillation.	–	–
28	V_{DD}	Positive power supply	–	–

1.2 PROGRAM MEMORY WRITE/VERIFY MODE

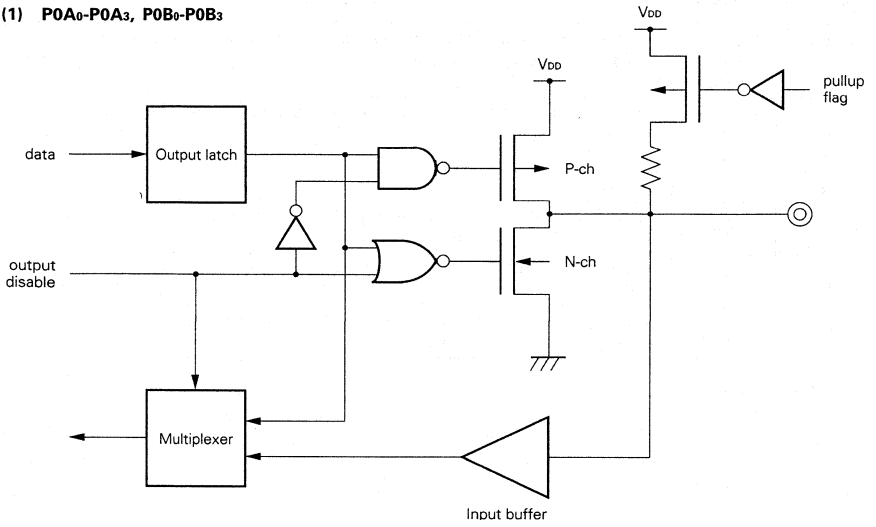
PIN NO.	SYMBOL	FUNCTION	I/O
2 I 5	MD_3 I MD_0	Input pins used as operation mode selection pins when writing to program memory or verifying its contents	Input
6 I 13	D_7 I D_0	Input/output pins for 8-bit data used when writing to program memory or verifying its contents	I/O
14	GND	Ground	–
17	V_{PP}	+12.5 V is applied to this program voltage pin when writing to program memory or verifying its contents.	–
27	CLK	Input pin for address update clock used when writing to program memory or verifying its contents	Input
28	V_{DD}	+6 V is applied to this positive power supply pin when writing to program memory or verifying its contents.	–

I/O: Input/output

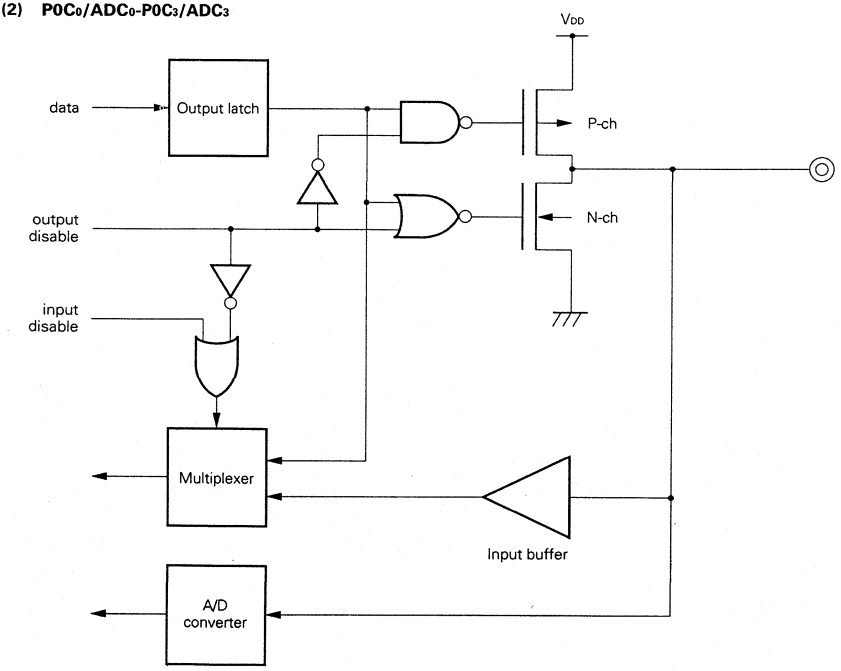
1.3 PIN EQUIVALENT CIRCUIT

The equivalent circuit of each μPD17P137A pin is shown below; some part of the circuit is simplified.

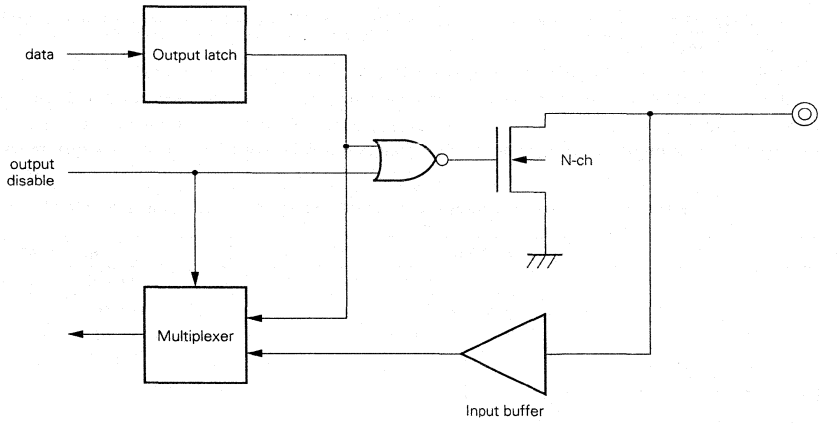
(1) $P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$



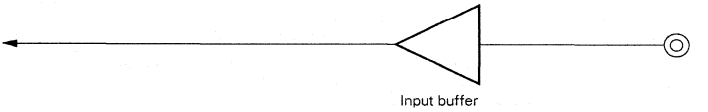
(2) $P0C_0$/ADC_0-$P0C_3$/ADC_3



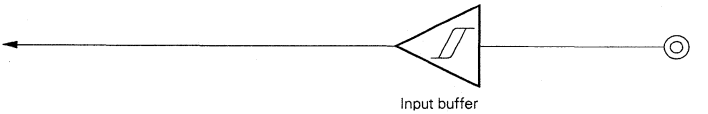
(3) $P0D_0$-POD_3, $P1A_0$-$P1A_3$



(4) $P1B_0$



(5) INT, $\overline{\text{RESET}}$



2. DIFFERENCES AMONG THE μPD17135A, μPD17137A, AND μPD17P137A

The μPD17P137A is a one-time PROM version of the μPD17137A, in which the internal mask ROM is replaced with a one-time PROM.

Table 2-1 lists the differences among the μPD17135A, μPD17137A, and μPD17P137A.

The μPD17P137A has the same CPU functions and internal peripheral hardwares as those of μPD17135A and μPD17137A except for its program memory, program size, address register size, and mask option. The μPD17P137A can be used for evaluation of programs during μPD17135A, μPD17137A system development.

Table 2-1 Differences among the μPD17135A, μPD17137A, and μPD17P137A

Item	μPD17135A	μPD17137A	μPD17P137A
ROM	Mask ROM		One-time ROM
	1024 × 16 bits (0000H-03FFH)	2048 × 16 bits (0000H-07FFH)	
Program counter (PC)	10 bits	11 bits	
Address register (AR)			
Address stack register			
Pull-up resistors of pins P0D, P1A, P1B, and $\overline{\text{RESET}}$	Mask option		None
Connection pin	V_{PP} pin and operation mode selection pins are not provided.		V_{PP} pin and operation mode selection pins are provided.
Supply voltage	2.7 to 5.5 V (when A/D converter is used: 5 V ±10 %)		
Package	28-pin shrink DIP 28-pin SOP		

3. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P137A internal program memory consists of a 2048 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the CLK pin.

Table 3-1 Pins Used when Writing to Program Memory or Verifying its Contents

SYMBOL	Function
V_{PP}	+12.5 V is applied to this program voltage pin when writing to program memory or verifying its contents.
V_{DD}	+6 V is applied to this positive power supply pin when writing to program memory or verifying its contents.
CLK	Input pin for address update clock used when writing to program memory or verifying its contents. Increment the program memory address by one on reception of four pulses on this CLK pin.
MD_0-MD_3	Input pins used as operation mode selection pins when writing to program memory or verifying its contents
D_0-D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

3.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), the μPD17P137A enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 to MD_3 pins as follows. Set the $\overline{RESET}$ pin and the other unused pins to GND level by means of pull-down resistors.

Table 3-2 Operating Mode Specification

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

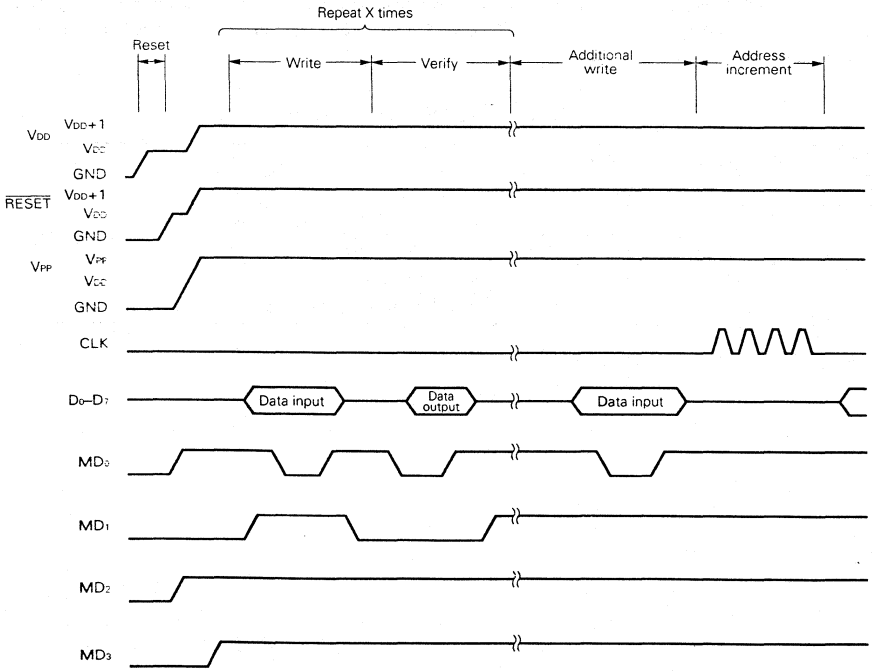
Remark ×: Don't care. L (low) or H (high)

3.2 WRITING TO PROGRAM MEMORY

The procedure for writing to program memory is described below; high-speed write is possible.

(1) Pull low the levels on all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Write data in 1 ms write mode.
(8) Select program inhibit mode.
(9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
(10) Perform additional write for (number of repetitions of steps (7) to (9)) × 1 ms.
(11) Select program inhibit mode.
(12) Increment the program memory address by one on reception of four pulses on the CLK pin.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Select program memory address clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn power off.

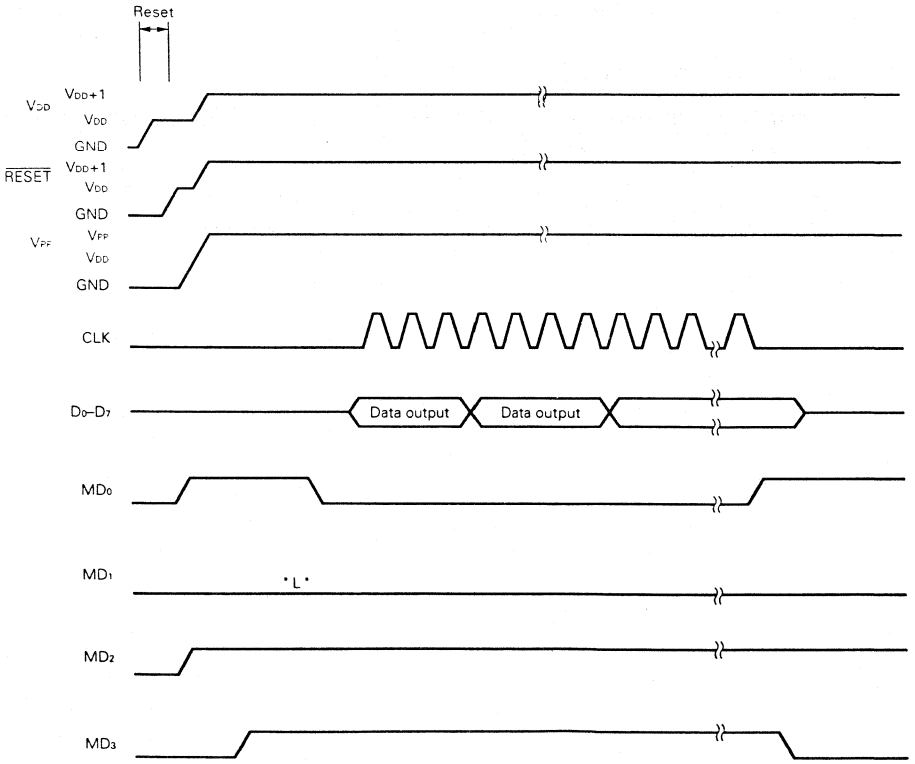
The timing for PROM writing steps (2) to (12) is shown below.



3.3 READING PROGRAM MEMORY

(1) Pull low the levels of all unused pins to GND by means of resistors. Bring CLK to low level.
(2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
(3) Wait 10 μs. Then apply 5 V to V_{PP}.
(4) Set the mode selection pins to program memory address clear mode.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Select program inhibit mode.
(7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the CLK pin.
(8) Select program inhibit mode.
(9) Select program memory address clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn power off.

The timing for PROM reading steps (2) to (9) is shown below.



4. ELECTRICAL CHARACTERISTICS (OBJECTIVES)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Supply Voltage	V_{DD}		−0.3 to +7.0	V
Input Voltage	V_I	P0D, P1A	−0.3 to +11.0	V
		All pins except pins above	−0.3 to V_{DD} +0.3	V
Output Voltage	V_O	P0D, P1A	−0.3 to +11.0	V
		All pins except pins above	−0.3 to V_{DD} + 0.3	V
High Level Output Current	I_{OH}	1 pin	−5.0	mA
		Sum of all pins	−20.0	mA
Low Level Output Current	I_{OL}	1 pin P0D, P1A	30.0	mA
		1 pin Other than pins above	5	mA
		Sum of all pins	100.0	mA
Operating Temperature	T_{opt}		−25 to +75	°C
Storage Temperature	T_{stg}		−65 to +150	°C
Power Consumption	P_D	T_a = 75 °C	180	mW

RECOMMENDED OPERATION RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Voltage	V_{DD}	2.7		5.5	V	
Oscillator Frequency	f_X	4.5		5.5	V	A/D converter is used.
		0.4		8.0	MHz	

DC CHARACTERISTICS 1 (T_a = −25 to +75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	RESET, P0D, P1A
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B
Low Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	RESET, P0D, P1A
	V_{IL2}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B
High Level Output Current	I_{OH}	1.0	2.0		mA	V_{DS} = 0.3 V **Note 1**
Low Level Output Current	I_{OL}	1.0	2.0		mA	V_{DS} = 0.3 V P0A, P0B, P0C **Note 1**
Low Level Output Voltage	V_{OL}			1.0	V	I_{OL} = 15 mA, P0D, P1A
High Level Input Leakage Current	I_{LIH1}			3.0	μA	Other than V_{IN} = V_{DD}, X_{IN}, X_{OUT}
	I_{LIH2}			10.0	μA	V_{IN} = V_{DD}, X_{IN}, X_{OUT},
Low Level Input Leakage Current	I_{LIL1}			−3.0	μA	Other than V_{IN} = 0 V, X_{IN}, X_{OUT},
	I_{LIL2}			−10.0	μA	V_{IN} = 0 V, X_{IN}, X_{OUT},
High Level Output Leakage Current	I_{LOH1}			3.0	μA	Other than V_{OUT} = V_{DD}, P0D, P1A
	I_{LOH2}			3.0	μA	V_{OUT} = V_{DD}, P0D, P1A **Note 2**
	I_{LOH3}			10.0	μA	V_{OUT} = 9 V, P0D, P1A **Note 3**
Low Level Output Leakage Current	I_{LOL}			−3.0	μA	V_{OUT} = 0 V
Internal Pull-up Resistor	R_{PULL}	50	100	200	kΩ	RESET, P0A, P0B, P0D, P1A
Low-Voltage Detection Voltage	V_{RES}		3.45	4.45	V	
Supply Current **Note 4**	I_{DD1}	Under evaluation			Operation mode	f_{CC} = 8.0 MHz
						f_{CC} = 4.0 MHz
						f_{CC} = 455 kHz
	I_{DD2}				HALT mode	f_{CC} = 8.0 MHz
						f_{CC} = 4.0 MHz
						f_{CC} = 455 kHz
	I_{DD3}				STOP mode	

Note 1. V_{DS}: Voltage drop at the ports

2. When the pull-up resistor which is built in the N-ch open drain is selected

3. When the pull-up resistor which is built in the N-ch open drain is not selected

4. When the A/D converter is not operating. Excluding the current which flows through the internal pull-up resistor

DC CHARACTERISTICS 2 (T_a = −25 to +75 °C, V_{DD} = 2.7 to 4.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$, P0D, P1A
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	P0A, P0B, P0C, P1B
Low Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$, P0D, P1A
	V_{IL2}	0		0.3 V_{DD}	V	P0A, P0B, P0C, P1B
High Level Output Current	I_{OH}	Under evaluation				V_{DS} = 0.3 V **Note 1**
Low Level Output Current	I_{OL}					V_{DS} = 0.3 V P0A, P0B, P0C **Note 1**
Low Level Output Voltage	V_{OL}					I_{OL} = 15 mA, P0D, P1A
High Level Input Leakage Current	I_{LIH1}			3.0	μA	Other than V_{IN} = V_{DD}, X_{IN}, X_{OUT}
	I_{LIH2}			10.0	μA	V_{IN} = V_{DD}, X_{IN}, X_{OUT},
Low Level Input Leakage Current	I_{LIL1}			−3.0	μA	Other than V_{IN} = 0 V, X_{IN}, X_{OUT},
	I_{LIL2}			−10.0	μA	V_{IN} = 0 V, X_{IN}, X_{OUT},
High Level Output Leakage Current	I_{LOH1}			3.0	μA	Other than V_{OUT} = V_{DD}, P0D, P1A
	I_{LOH2}			3.0	μA	V_{OUT} = V_{DD}, P0D, P1A **Note 2**
	I_{LOH3}			10.0	μA	V_{OUT} = 9 V, P0D, P1A **Note 3**
Low Level Output Leakage Current	I_{LOL}			−3.0	μA	V_{OUT} = 0 V
Internal Pull-up Resistor	R_{PULL}	50	100	200	kΩ	$\overline{\text{RESET}}$, P0A, P0B, P0D, P1A
Supply Current **Note 4**	I_{DD1}	Under evaluation				Operation mode, f_{CC} = 8.0 MHz
						Operation mode, f_{CC} = 4.0 MHz
						Operation mode, f_{CC} = 455 kHz
	I_{DD2}					HALT mode, f_{CC} = 8.0 MHz
						HALT mode, f_{CC} = 4.0 MHz
						HALT mode, f_{CC} = 455 kHz
	I_{DD3}					STOP mode

Note 1. V_{DS}: Voltage drop at the ports

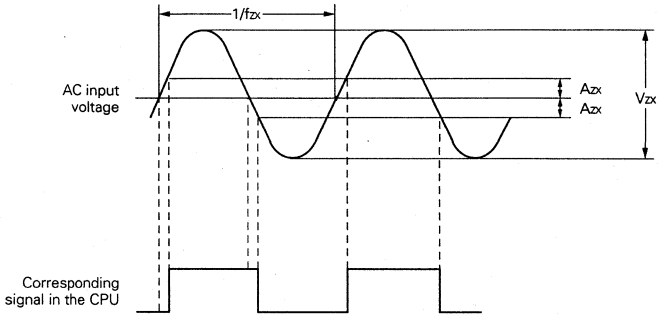
2. When the pull-up resistor which is built in the N-ch open drain is selected
3. When the pull-up resistor which is built in the N-ch open drain is not selected
4. When the A/D converter is not operating. Excluding the current which flows through the internal pull-up resistor.

AC CHARACTERISTICS (T_a = −25 to +75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{KCY}	2.0			μs	At data input
		10.0				At data output
$\overline{SCK}$ High/Low Level Width	t_{KH}, t_{KL}	1.0			μs	At data input
		5.0				At data output
SI Setup Time (with respect to $\overline{SCK}$)	t_{SIK}	100			ns	
SI Hold Time (with respect to $\overline{SCK}$)	t_{KSI}	100			ns	
SO Output Delay Time (with respect to $\overline{SCK}$)	t_{KSO}			4.5	μs	C_L = 100 pF
INT High/Low Level Width	t_{INTH}, t_{INTL}	10			μs	
$\overline{RESET}$ Low Level Width	t_{RSL}	10			μs	

ZEROCROSS CHARACTERISTICS (T_a = –25 to +75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Zerocross Detection Input Level	V_{ZX}	1.0		3.0	V	AC input, coupling capacity of 1 μF
Zerocross Detection Input Frequency	f_{ZX}	40	50/60	1000	Hz	
Zerocross Accuracy	A_{ZX}		±120		mV	50/60 Hz



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by A_{ZX} in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D CONVERTER CHARACTERISTICS (T_a = –25 to +75 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		8	8	8	bit	
Absolute accuracy **Note 1**				±1.5	LSB	$V_{ADC} = V_{DD}$
ADC circuit current	I_{AREF}		1.5	2.0	mA	
Conversion time	t_{CONV}			400/f_x	s	**Note 2**

Note 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (at f_x = 8 MHz, 50 μs)

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CLK
	V_{IH2}	V_{DD}–0.5		V_{DD}	V	CLK
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output Voltage High	V_{OH}	V_{DD}–1.0			V	I_{OH} = –1 mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{PP} Power Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Cautions 1. V_{PP} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{PP} on and must be off after V_{PP} off.

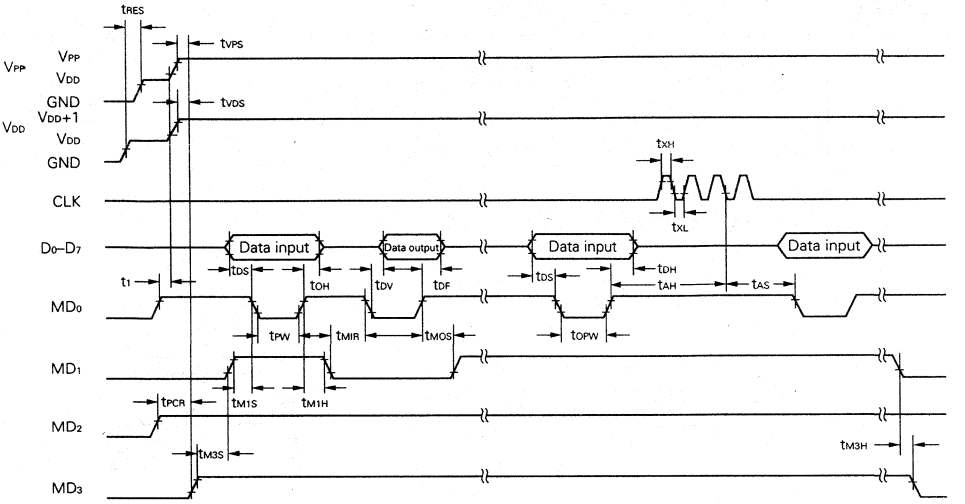
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	Note 1	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Setup Time to MD0 ↓ **Note 2**	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time to MD0 ↓	t_{M1S}	t_{OES}	2			μs	
Data Setup Time to MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address Hold Time to MD0 ↑ **Note 2**	t_{AH}	t_{AH}	2			μs	
Data Hold Time to MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time from MD0 ↑→	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1 ↑	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time from MD0 ↑→	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time to MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recovery Time to MD0 ↓	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High, Low Level Range	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			2	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time to MD1 ↑	t_{M3S}	–	2			μs	
MD3 Hold Time to MD1 ↓	t_{M3H}	–	2			μs	
MD3 Setup Time to MD0 ↓	t_{M3SR}	–	2			μs	Read program memory
Data Output Delay Time from Address **Note 2**	t_{DAD}	t_{ACC}	2			μs	Read program memory
Data Output Hold Time from Address **Note 2**	t_{HAD}	t_{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0 ↑	t_{M3HR}	–	2			μs	Read program memory
Data Output Float Delay Time from MD3 ↓→	t_{DFR}	–	2			μs	Read program memory
Reset Setup Time	t_{RES}		10			μs	

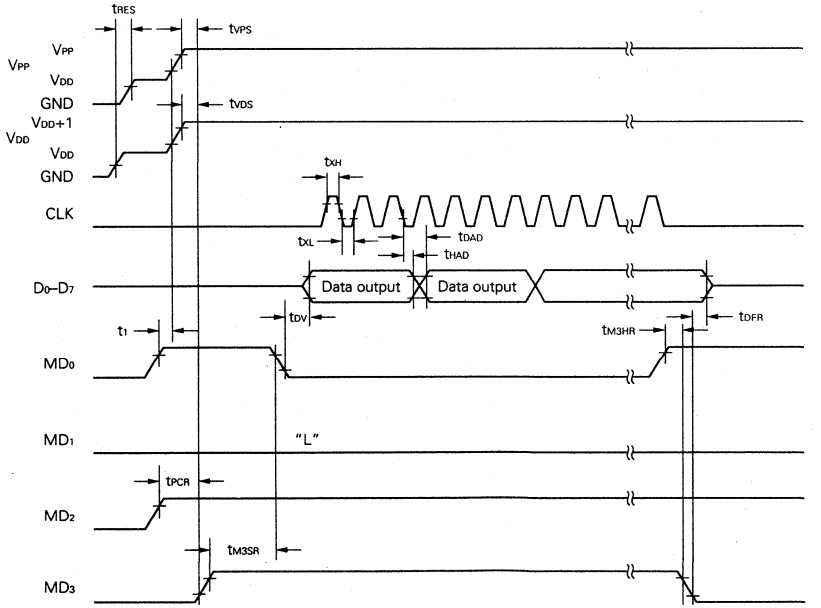
Note 1. Symbols for corresponding μPD27C256A.

2. Internal address signal is incremented by one at the falling edge of the third CLK input.

Write program memory timing

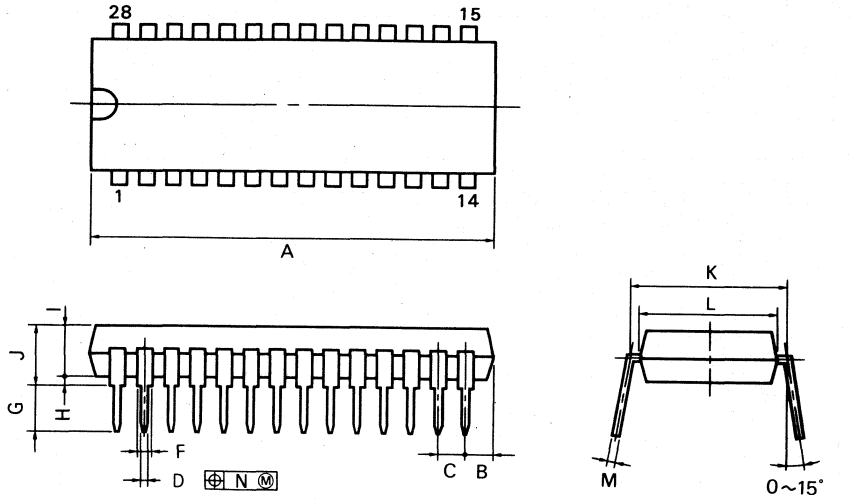


Read program memory timing



5. PACKAGE DIMENSIONS

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

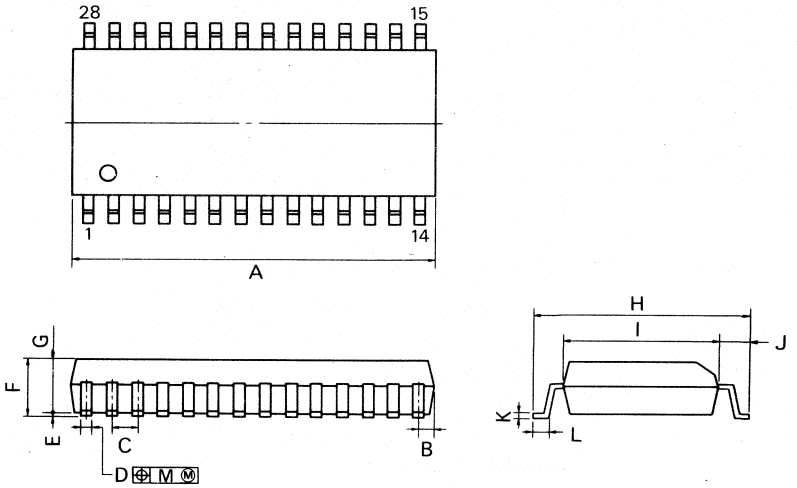
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

28PIN PLASTIC SOP (375 mil)



P28GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.008}_{-0.008}$
M	0.12	0.005

APPENDIX A. MICROCONTROLLER FAMILY FOR SMALL HOME ELECTRIC APPLIANCES

Item \ Product	μPD17134A	μPD17135A	μPD17136A	μPD17137A	μPD17P136A	μPD17P137A
ROM size	1024 × 16 bits (Mask ROM)		2048 × 16 BITS (Mask ROM)		2048 × 16 bits (One-time PROM)	
RAM size	112 × 4 bits					
Number of I/O port lines	22 lines (Including 8 N-ch open drain lines)					
Analog input	4 channels					
Timer	3 timers					
Serial interface	1 channel					
Stack	5 levels					
Power-on reset	Provided					
System clock	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation	RC oscillation	Ceramic oscillation
Standby function	HALT mode/STOP mode					
Supply voltage	V_{DD} = 2.7 to 5.5 V (When A/D converter is used: V_{DD} = 5 V ±10 %)					
Package	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)					

I/O: Input/output

4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17156 is a 4-bit single-chip microcontroller containing an 8-bit A/D converter (8 channels), 8-bit timers (3 channels) a serial interface, and a power-on/power-down reset circuit in one chip.

For the CPU, the μPD17156 employs the 17K architecture instead of the accumulator scheme. This enables operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (one word) long, enabling efficient programming.

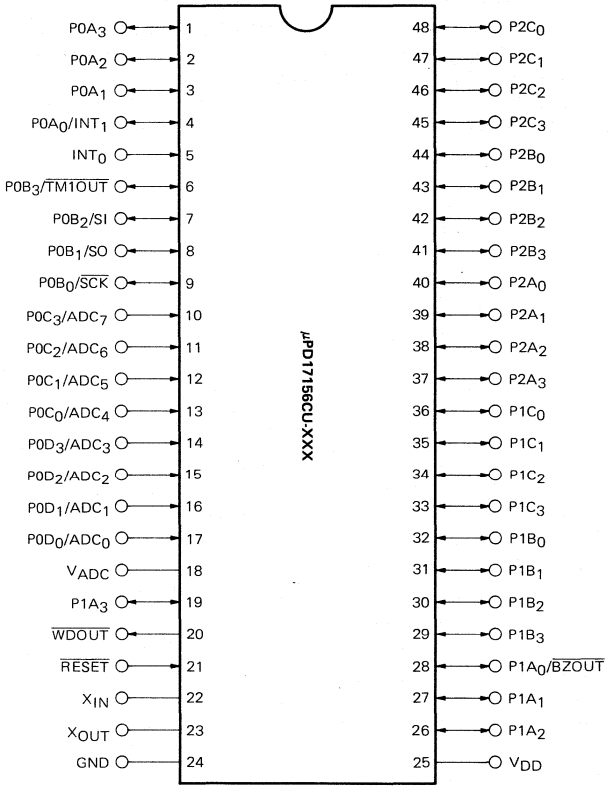
The μPD17P158, a one-time PROM that can be written to just once, is available for evaluating programs for the μPD17156 and for small production.

FEATURES

- 17K architecture: General registers
- Program memory (ROM): 6144 x 16 bits
- Data memory (RAM): 336 x 4 bits
- Input/output pin: 32 pins
- Input pin: 9 pins
- 8-bit A/D converter: 8 channels
  Absolute accuracy
  ±1.5 LSB or less
- 8-bit timer: 3 channels
- 7-bit basic interval timer: 1 channel. Can be used as 8-bit watchdog timer.
  An overflow output pin is provided for the watchdog timer.
- 3-wire serial interface: 1 channel
- Audible tone output: 0.5, 1, 2, or 4 kHz can be selected (during operation with an 8 MHz clock).
- Stack level: 7 levels (interrupt: 3 levels)
- Vectored interrupt: 2 external interrupt pins (INT_0 and INT_1)
  6 internal interrupt pins ($Timer_0$, $Timer_1$, $Timer_2$, basic interval timer, serial interface, and A/D converter)
- Instruction execution time: 2 μs (at 8 MHz: Ceramic or quartz resonator)
- Standby function (HALT/STOP)
- On-chip power-on/power-down reset circuit
- Operating voltage: 4.5 to 6.0 V

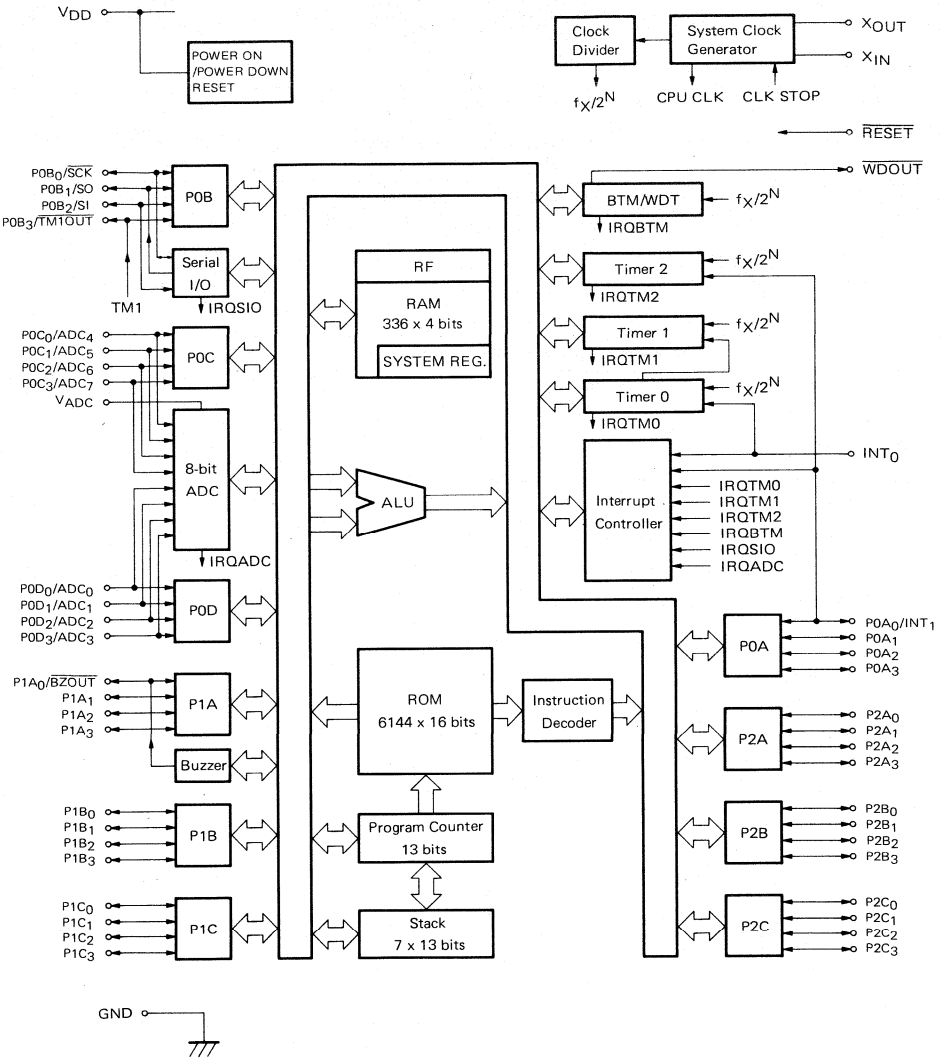
PIN CONFIGURATION (Top View)

48-pin plastic shrink DIP



$P0A_0$-$P0A_3$:	Port 0A (N-ch open-drain input/output)	SI:	Serial data input
$P0B_0$-$P0B_3$:	Port 0B (N-ch open-drain input/output)	SO:	Serial data output
$P0C_0$-$P0C_3$:	Port 0C (Input)	$\overline{SCK}$:	Serial clock input/output
$P0D_0$-$P0D_3$:	Port 0D (Input)	ADC_0-ADC_7:	Analog input for the A/D converters
$P1A_0$-$P1A_3$:	Port 1A (N-ch open-drain input/output)	V_{ADC}:	Analog power supply
$P1B_0$-$P1B_3$:	Port 1B (CMOS push-pull input/output)	$\overline{BZOUT}$:	Audible tone output
$P1C_0$-$P1C_3$:	Port 1C (CMOS push-pull input/output)	$\overline{WDOUT}$:	Watchdog timer output
$P2A_0$-$P2A_3$:	Port 2A (CMOS push-pull input/output)	$\overline{RESET}$:	Reset input
$P2B_0$-$P2B_3$:	Port 2B (CMOS push-pull input/output)	X_{IN}, X_{OUT}:	To be connected to the system clock resonator
$P2C_0$-$P2C_3$:	Port 2C (CMOS push-pull input/output)	V_{DD}:	Power supply
INT_0, INT_1:	External interrupt input	GND:	Ground
$\overline{TM1OUT}$:	Timer 1 carry output		

BLOCK DIAGRAM



MICROCONTROLLER FAMILY FOR HOME ELECTRIC APPLIANCES

Item	μPD17156[Note 1]	μPD17158[Note 2]	Remarks
ROM size	6144 x 16 bits	8192 x 16 bits	
RAM size	336 x 4 bits		
Number of I/O pins	41 pins (Including 9 input pins)		Including 12 N-ch open drain lines
A/D converter	8 channels (resolution of 8 bits)		Also used as port pins
Timer	4 timers { Three 8-bit timers (TM0, TM1, and TM2); One 7-bit basic interval timer (BTM) }		The BTM can also be used as 8-bit watchdog timer (WDT).
3-wire serial interface	1 channel		Also used as port pin
Stack	7 levels		
System clock	A ceramic or quartz resonator is used.		
Instruction execution time	2 μs at (8 MHz)		
Standby function	HALT, STOP		
Power-on/power-down reset function	Voltage at which power-on/power-down reset occurs: 3.5 V (TYP.)		
Operating voltage	4.5 to 6.0 V		
Package	48-pin shrink DIP (600 mil)		
One-time PROM version	μPD17P158		

I/O: Input/output

Note 1. Under development

2. Planned

4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17P158 is a one-time PROM version of the μPD17156, whose internal mask ROM is replaced with a one-time PROM, and is therefore suitable for evaluation of programs for the μPD17156 or for small-scale production.

The μPD17P158 is a 4-bit single-chip microcontroller containing an 8-bit A/D converter (8 channels), 8-bit timers (3 channels), a serial interface, and a power-on/power-down reset circuit in one chip.

For the CPU, the μPD17P158 employs the 17K architecture instead of the accumulator scheme. This enables operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (one word) long, enabling efficient programming.

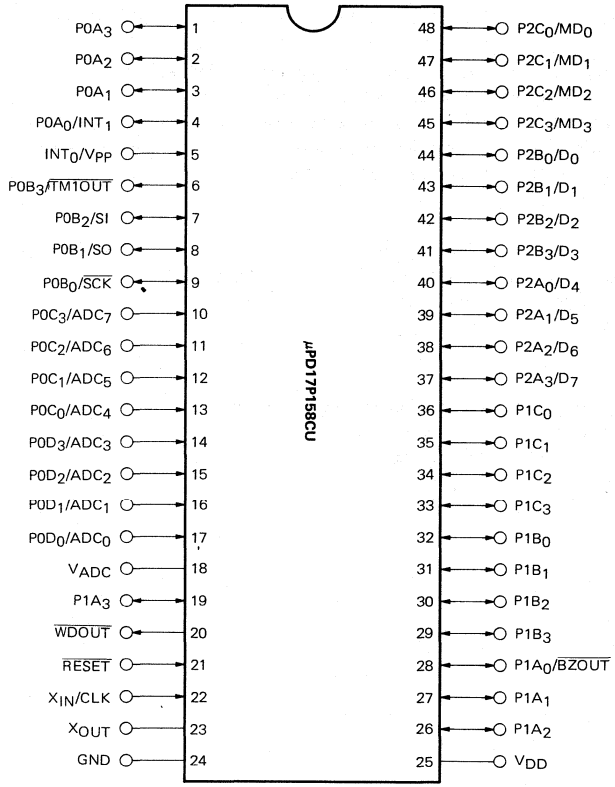
FEATURES

- 17K architecture: General registers
- Can be used for evaluation of programs for the μPD17156 and μPD17158[Note]
- Program memory (PROM): 8192 x 16 bits
- Data memory (RAM): 336 x 4 bits
- 8-bit A/D converter: 8 channels
- 8-bit timer: 3 channels
- 7-bit basic interval timer: 1 channel. Can be used as 8-bit watchdog timer.
- 3-wire serial interface: 1 channel
- Instruction execution time: 2 μs (at 8 MHz: Ceramic or crystal resonator)
- Operating voltage: 4.5 to 6.0 V

Note Planned

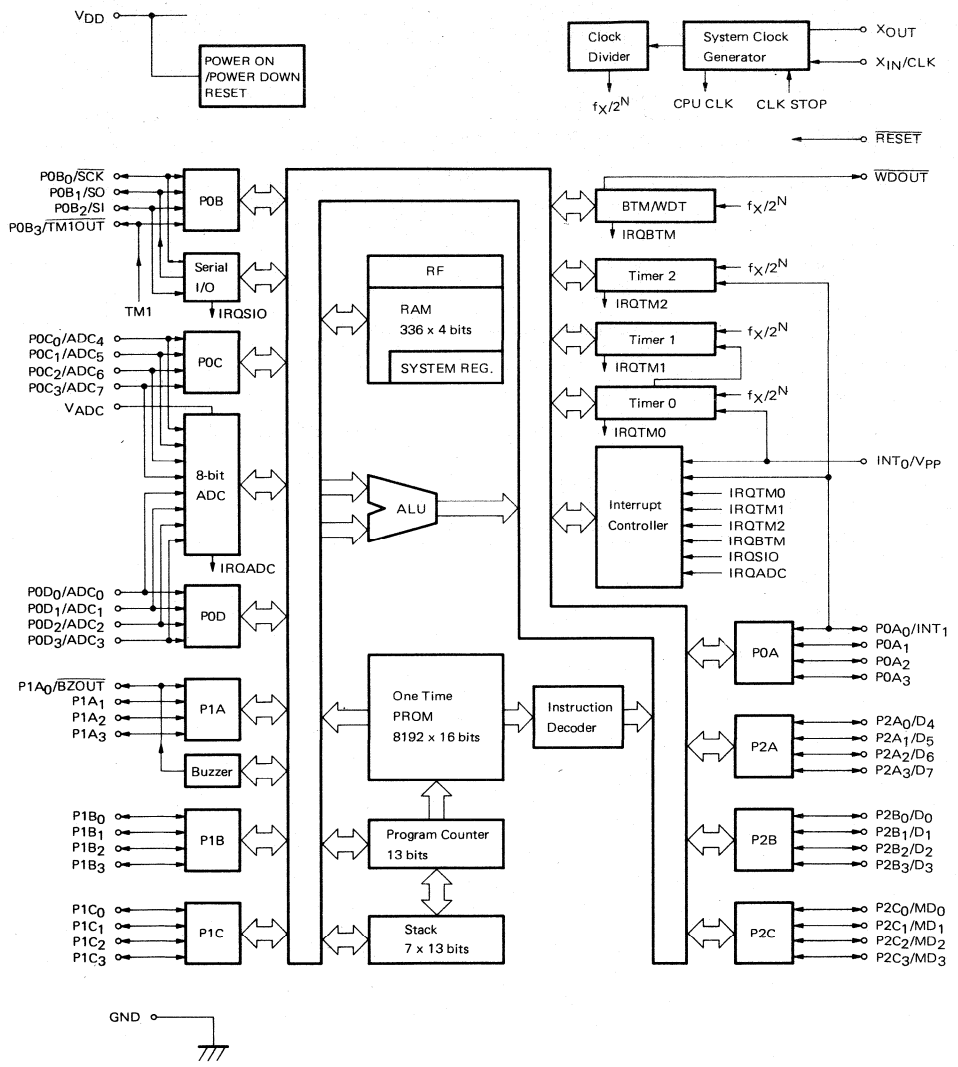
PIN CONFIGURATION (Top View)

48-pin plastic shrink DIP



$P0A_0$-$P0A_3$:	Port 0A (N-ch open-drain input/output)
$P0B_0$-$P0B_3$:	Port 0B (N-ch open-drain input/output)
$P0C_0$-$P0C_3$:	Port 0C (Input)
$P0D_0$-$P0D_3$:	Port 0D (Input)
$P1A_0$-$P1A_3$:	Port 1A (N-ch open-drain input/output)
$P1B_0$-$P1B_3$:	Port 1B (CMOS push-pull input/output)
$P1C_0$-$P1C_3$:	Port 1C (CMOS push-pull input/output)
$P2A_0$-$P2A_3$:	Port 2A (CMOS push-pull input/output)
$P2B_0$-$P2B_3$:	Port 2B (CMOS push-pull input/output)
$P2C_0$-$P2C_3$:	Port 2C (CMOS push-pull input/output)
INT_0, INT_1:	External interrupt input
$\overline{TM1OUT}$:	Timer 1 carry output
SI:	Serial data input
SO:	Serial data output
$\overline{SCK}$:	Serial clock input/output
ADC_0-ADC_7:	Analog input for the A/D converter
V_{ADC}:	Analog power supply
$\overline{BZOUT}$:	Audible tone output
$\overline{WDOUT}$:	Watchdog timer output
$\overline{RESET}$:	Reset input
X_{IN}, X_{OUT}:	To be connected to the system clock resonator
V_{DD}:	Positive power supply
GND:	Ground
CLK:	Address update clock input
MD_0-MD_3:	Operating mode selection
D_0-D_7:	Data input/output
V_{PP}:	PROM power supply

BLOCK DIAGRAM



MICROCONTROLLER FAMILY FOR HOME ELECTRIC APPLIANCES

Item	μPD17156[Note 2]	μPD17158[Note 2]	μPD17P158[Note 1]
ROM size	6144 x 16 bits (Mask ROM)	8192 x 16 bits (Mask ROM)	8192 x 16 bits (One-time PROM)
RAM size	336 x 4 bits		
Number of I/O pins	41 pins (Including 9 input pins and 12 N-ch open drain pins)		
A/D converter	8 channels (resolution of 8 bits)		
Timer	4 timers { Three 8-bit timers (TM0, TM1, and TM2) One 7-bit basic interval timer (BTM)		
3-wire serial interface	1 channel		
Stack	7 levels		
System clock	A ceramic or crystal resonator is used.		
Instruction execution time	2 μs (at 8 MHz)		
Standby function	HALT, STOP		
Power-on/power-down reset function	Voltage at which power-on/power-down reset occurs: 3.5 V (TYP.)		
Operating voltage	4.5 to 6.0 V		
Package	48-pin plastic shrink DIP (600 mil)		

I/O: Input/output

Note 1. Under development

2. Planned

4-BIT SINGLE-CHIP MICROCONTROLLER WITH A/D CONVERTER AND LCD CONTROLLER/DRIVER FOR INFRARED REMOTE CONTROLLER

μPD17201A is a 4-bit single-chip microcontroller integrating an LCD controller/driver, A/D converter, and an infrared remote controller carrier generator circuit on a single chip.

This microcontroller employs the architecture of 17K and can execute transfer and arithmetic operations with a single 16-bit instruction between data memory addresses and between the data memory and a peripheral circuit.

μPD17201A is housed in a 80-pin plastic QFP.

FEATURES

- 17K architecture
- Program memory (ROM): 3072 × 16 bits
- Data memory (RAM): 336 × 4 bits
- Internal infrared remote controller carrier generator
- 4-channel 8-bit A/D converter
- Internal LCD controller/driver (can display up to 136 segments)
  Common pins: 4, segment pins: 34 (two of the common pins can also be used as segment pins)
  Internal LCD drive constant rising-voltage circuit: LCD drive voltage can be arbitrarily set at 2.4 to 5.4 V by external resistor
- I/O ports: 19
- Three-line serial interface
- Stack levels: 5 (3 interrupt levels)
- 8-bit timer: 1 channel
- Watch timer: 1 channel
- Instruction execution time: 4 μs (with 4 MHz ceramic oscillator/crystal resonator)
- Standby function (STOP, HALT): Watch display with 32.768 kHz crystal resonator in STOP mode
- Operating voltage range: 2.2 to 5.5 V

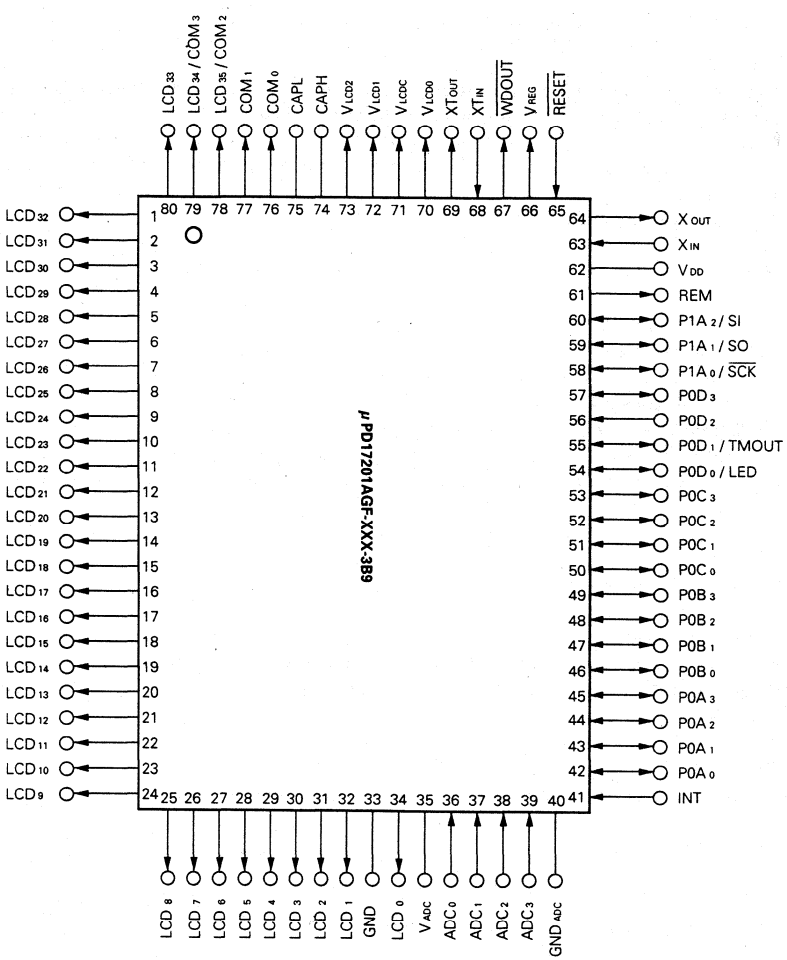
APPLICATIONS

Infrared remote controllers for air conditioners, and remote controllers with LCD

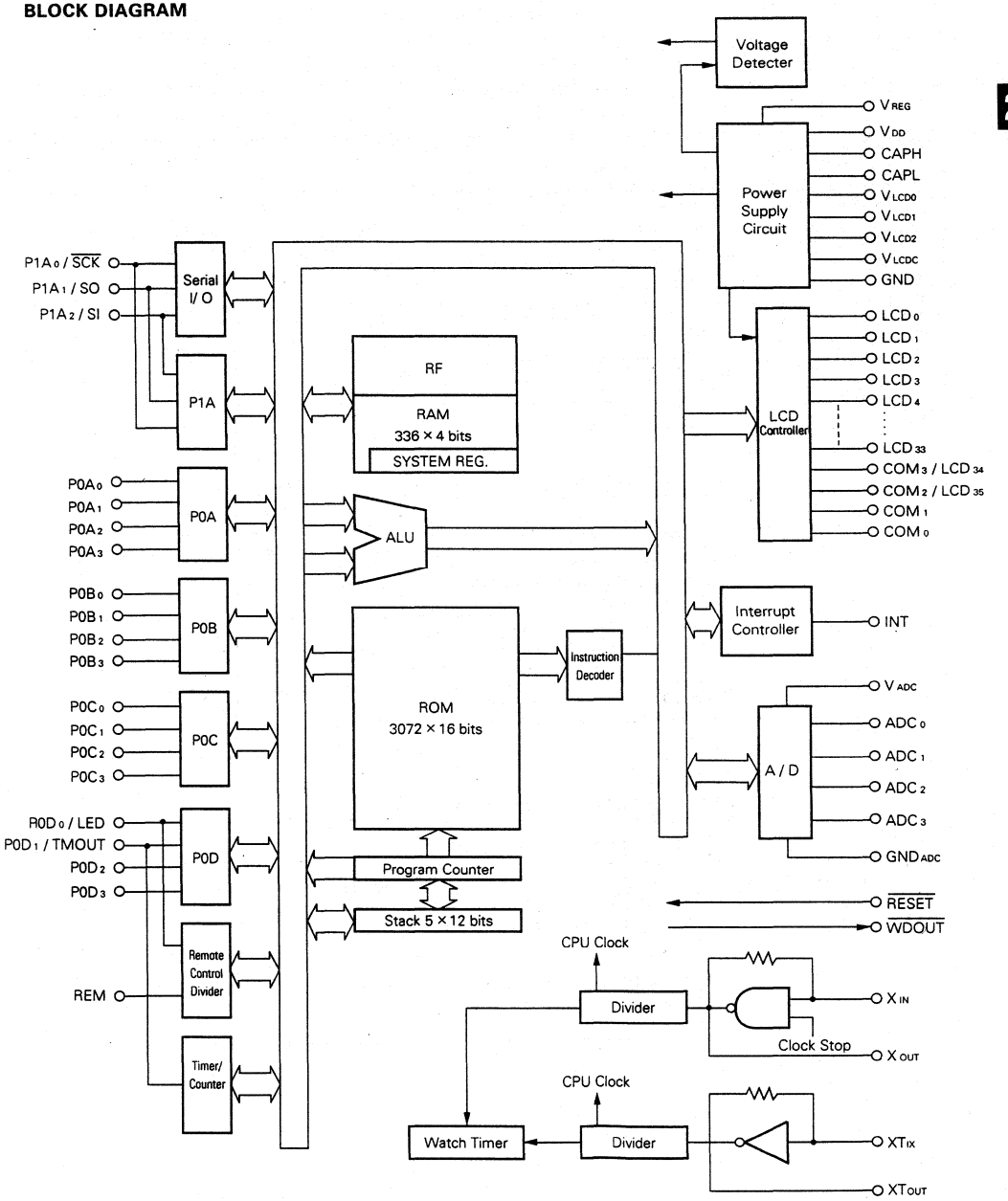
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17201AGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)	Standard

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN IDENTIFICATION

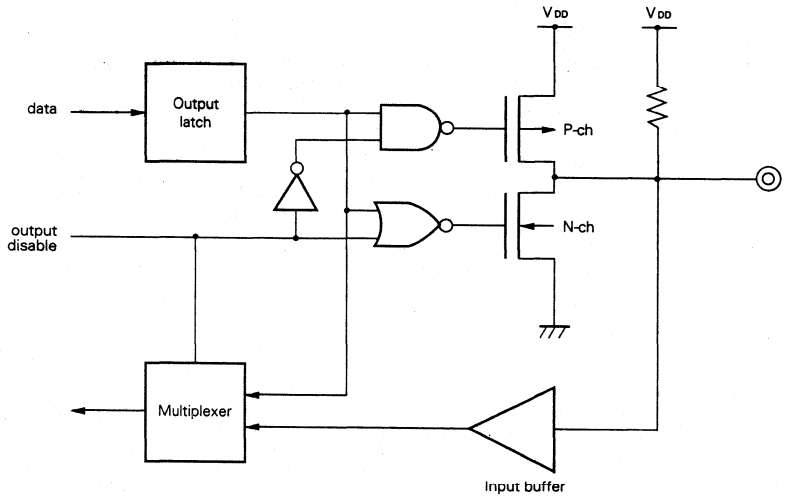
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	ON RESET
76 77 78 79 80 1 to 32 34	COM_0 COM_1 LCD_{35}/COM_2 LCD_{34}/COM_3 LCD_{33} LCD_{32} to LCD_1 LCD_0	Common signal and segment signal output pins of LCD driver. Segment signal or common signal outputs are selected by $LCDMD_3$ to $LCDMD_0$ of register file. • COM_0 to COM_3 • Common signal outputs of LCD driver • LCD_{35} to LCD_0 • Segment signal outputs of LCD driver	CMOS push-pull	OUTPUT (1/2 V_{DD})
33	GND	Ground	—	—
35	V_{ADC}	Positive power of A/D converter $V_{ADC} = V_{DD}$	—	—
36 to 39	ADC_0 to ADC_3	Analog inputs to A/D converter with 8-bit resolution	—	—
40	GND_{ADC}	Ground of A/D converter	—	—
41	INT	External interrupt request signal input. Generates interrupt request signal at rising edge of input signal	—	Input
42 to 45	$P0A_0$ to $P0A_3$	4-bit I/O port. Can be set in input or output mode in units of 4 bits (group I/O). Provided with pull-up resistor	CMOS push-pull	Input
46 to 49	$P0B_0$ to $P0B_3$	4-bit I/O port. Can be set in input or output mode in units of 4 bits (group I/O).	N-ch open-drain	Input
50 to 53	$P0C_0$ to $P0C_3$	4-bit I/O port. Can be set in input or output mode in units of 4 bits (group I/O).	N-ch open-drain	Input
54 55 56 57	$P0D_0$/LED $P0D_1$/TMOUT $P0D_2$ $P0D_3$	Port 0D, LED output, and 8-bit timer output. $P0D_0$ or LED output is selected by NRZEN of register file. $P0D_1$ or 8-bit timer output is selected by TMOE of register file. • $P0D_0$ to $P0D_3$ • 4-bit I/O port • Can be set in input or output mode in bit units (bit I/O) • LED • Visible LED drive output • TMOUT • 8-bit timer output	CMOS push-pull	Input

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	ON RESET
58 59 60	P1A0/$\overline{SCK}$ P1A1/SO P1A2/SI	Port 1A and serial interface. Port 1A or serial interface is selected by SIOEN of register file. • P1A0 to P1A2 • 3-bit I/O port • Can be set in input or output mode in units of 3 bits (group I/O) • $\overline{SCK}$, SO, SI • $\overline{SCK}$: serial clock I/O • SO: serial data output • SI: serial data input	CMOS push-pull	Input
61	REM	Infrared remote controller signal output. Drives infrared LED	CMOS push-pull	Low-level output
62	V_{DD}	Positive power	—	—
63 64	X_{IN} X_{OUT}	Connect 4 MHz ceramic or crystal oscillator for main clock oscillation	—	(Stops oscillation)
65	$\overline{RESET}$	System reset input	—	Input
66	V_{REG}	Output of voltage regulator for subclock oscillator. Connect 0.1 μF capacitor	—	—
67	$\overline{WDOUT}$	Overrunning detection output. Goes low when watchdog timer overflow or stack overflow occurs	CMOS push-pull	High-level output
68 69	XT_{IN} XT_{OUT}	Connect 32 kHz crystal oscillator for subclock oscillation	—	(Oscillates)
71	V_{LCDC}	Output to adjust LCD drive reference voltage	—	—
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	LCD drive reference voltage output • V_{LCD0}: Reference voltage output • V_{LCD1}: Doubler output (x2 voltage) • V_{LCD2}: Tripler output (x3 voltage)	—	—
74 75	CAPH CAPL	Connect voltage-raising capacitor for LCD cpacitor for LCD drive voltage	—	—

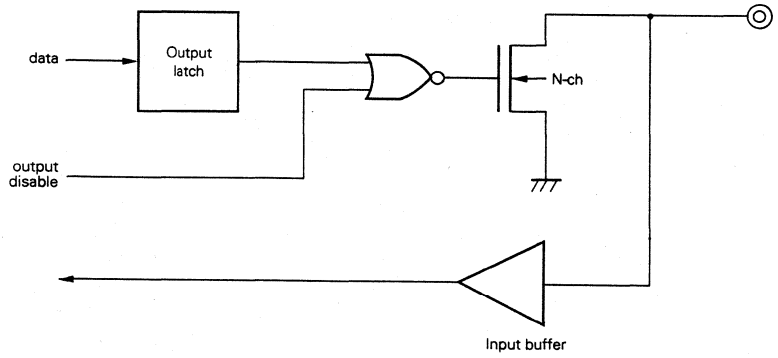
1.2 INPUT/ OUTPUT CIRCUIT

The equivalent input/output circuit of each μPD17201A's pin is shown below.

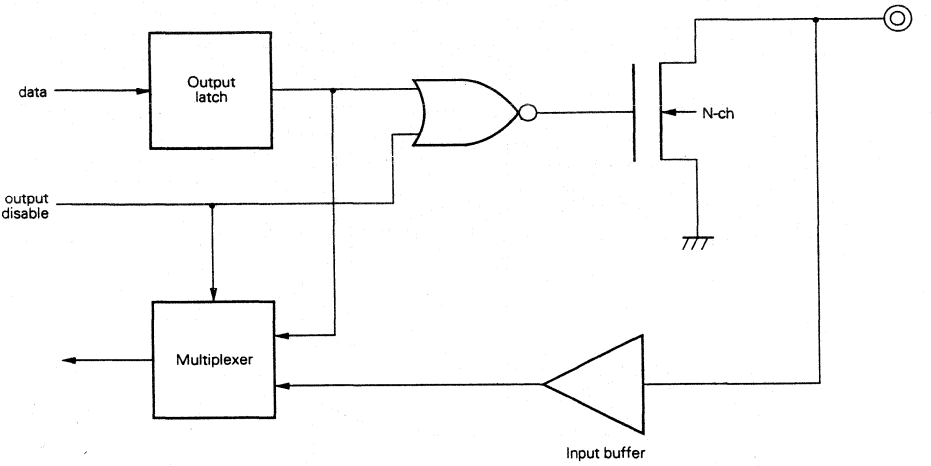
(1) P0A0 to P0A3



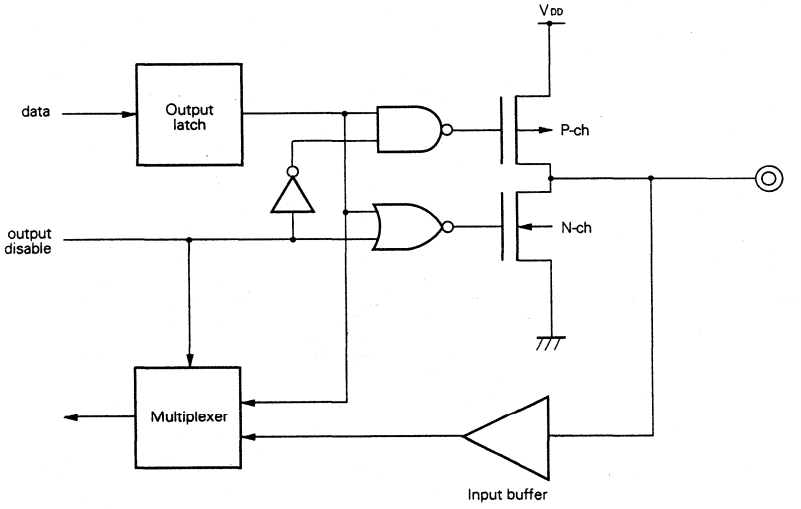
(2) P0B0 to P0B3



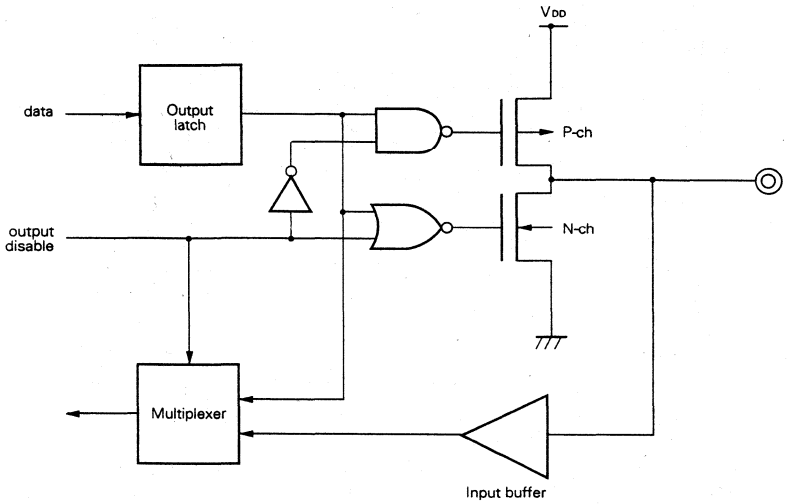
(3) $P0C_0$ to $P0C_3$



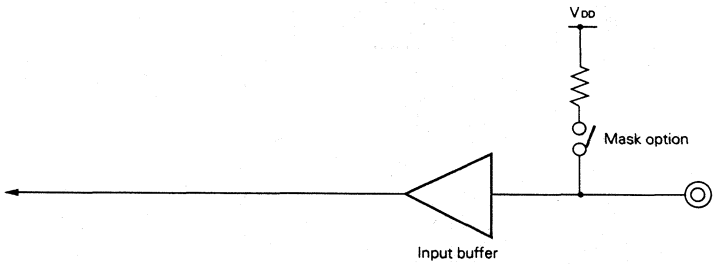
(4) $P0D_0$ to $P0D_3$



(5) P1A0 to P1A2



(6) $\overline{\text{RESET}}$



23. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a=25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	AV_{DD}			−0.3 to +7.0	V
Input Voltage	V_I			−0.3 to V_{DD}+0.3	V
Output Voltage	V_O			−0.3 to V_{DD}+0.3	V
High-Level Output Current		REM pin	Peak	−30	mA
			Effective	−20	mA
		1 pin (except REM)	Peak	−7.5	mA
			Effective	−5	mA
		All pins (except REM)	Peak	−22.5	mA
			Effective	−15	mA
Low-Level Output Current		1 pin	Peak	7.5	mA
			Effective	5	mA
		All pins (except REM)	Peak	22.5	mA
			Effective	15	mA
Operating Temperature	T_{opt}			−20 to +75	°C
Storage Temperature	T_{stg}			−40 to +125	°C

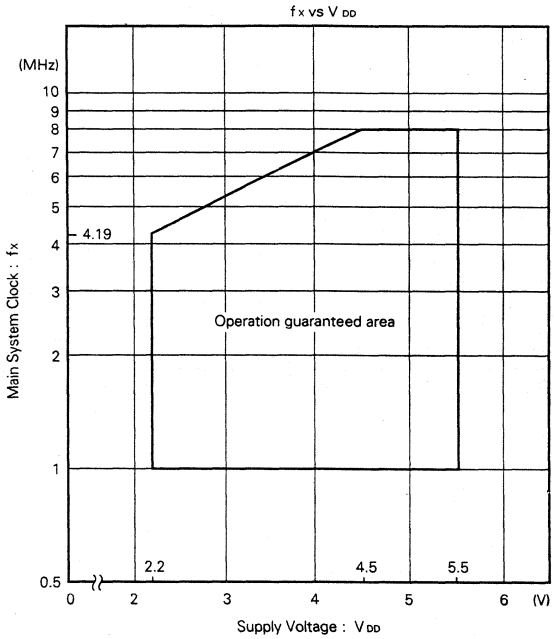
Note Effective value = Peak value × $\sqrt{\text{Duty}}$

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

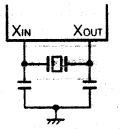
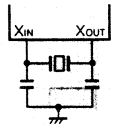
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input capacitance	C_{IN}			10	pF	INT, SI, $\overline{\text{RESET}}$ pins

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz
	V_{DD2}	4.5	5.0	5.5	V	System clock: f_X = 8 MHz
	V_{DD3}	2.0	3.0	5.5	V	System clock: f_{XT} = 32 kHz
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		KHz	



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

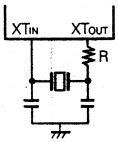
OSCILLATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic oscillator Note 3		Oscillation frequency (fx) Note 1		1.0	4.19	8.0	MHz
		Oscillation stabilization time Note 2	From when V_{DD} reaches the minimum oscillation voltage			4	ms
Crystal resonator Note 3		Oscillation frequency (fx) Note 1		1.0	4.19	8.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms

Note 1. The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2. The oscillation stabilization time is the time required for stabilizing the oscillation after V_{DD} is applied or the STOP mode is released.

3. The recommended oscillators are shown in the table described later.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS

OSCILLATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal Oscillator		Oscillation frequency (fXT)			32.768		kHz
		Oscillation stabilization time			5	10	s

Caution When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the following notations must be read and observed for wiring within the shaded area in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line.**
- **Capacitors used in the oscillators must always be grounded to Vss potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

RECOMMENDED OSCILLATORS

AMIN SYSTEM CLOCK: CERAMIC OSCILLATOR

Manufacturer	Product name	External capacitor (pF)		Oscillation voltage (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW	none	none	2.0	6.0	
	CST4.19MGW	none	none	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

Manufacturer	Frequency (MHz)	Retainer	External capacitor (pF)		Oscillation voltage (V)		Remarks
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Low-Voltage Detection Voltage 0	V_{DET0}	1.6	2.0	2.8	V		
Low-Voltage Detection Voltage 1	V_{DET1}	1.9	2.3	3.4	V		
High-Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{RESET}$, INT	
	V_{IH2}	0.7V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT	
Low-Level Input Voltage	V_{IL1}	0		0.2V_{DD}	V	$\overline{RESET}$, INT	
	V_{IL2}	0		0.3V_{DD}	V	Other than $\overline{RESET}$, INT	
High-Level Input Leakage Current	I_{LIH1}			20	μA	XT_{IN}, XT_{OUT}, X_{IN}, X_{OUT}	
	I_{LIH2}			3	μA	Other than above	
Low-Level Input Leakage Current	I_{LIL1}			−20	μA	XT_{IN}, XT_{OUT}, X_{IN}, X_{OUT}	
	I_{LIL2}			−3	μA	Other than above	
High-Level Output Current	I_{OH1}	−7	−15		mA	REM, V_{OH} = V_{DD} − 1.2 V	
	I_{OH2}	−0.3	−0.7		mA	**Note 1.** V_{OH} = V_{DD} − 0.3 V	
Low-Level Output Current	I_{OL}	0.5	0.9		mA	**Note 2.** V_{OL} = 0.3 V	
Internal Pull-up Resistor	R_{P0A}	100	200	350	kΩ	$P0A_0$-$P0A_3$	
	R_{RES}	24	47	94	kΩ	$\overline{RESET}$	
A/D Absolute Accuracy				±2	LSB		
A/D Resolution			8		BITS		
A/D Convertor Current Dissipation	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comparator mode	
Supply Current	I_{DD1}		0.8	2.0	mA	w/X (f_X = 4.19 MHz) w/o XT	Operation mode
	I_{DD2}		0.3	1.5	mA		HALT mode
	I_{DD3}		2.0	10.0	μA	V_{DD} = 3 V	STOP mode
	I_{DD4}		7.0	25	μA	w/o X or STOP w/XT (f_{XT} = 32.768 kHz)	Operation mode
	I_{DD5}		3.0	15	μA	V_{DD} = 3 V	HALT mode

Note 1. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, and $P1A_0$ to $P1A_2$ pins

2. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_2$ and REM pins

LCD CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
LCD Output Voltage Adjustable Range	V_{LCD0}	0.8		1.8	V	Value of external variable resistor: 0 to 2.2 MΩ
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 − C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 − C4 = 0.47 μF
LCD COMMON Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V
LCD SEGMENT Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ± 10 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Low-Voltage Detection Voltage 0	V_{DET0}	1.6	2.0	2.8	V		
Low-Voltage Detection Voltage 1	V_{DET1}	1.9	2.3	3.4	V		
High-Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{RESET}$, INT	
	V_{IH2}	0.7V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT	
Low-Level Input Voltage	V_{IL1}	0		0.2V_{DD}	V	$\overline{RESET}$, INT	
	V_{IL2}	0		0.3V_{DD}	V	Other than $\overline{RESET}$, INT	
High-Level Input Leakage Current	I_{LIH1}			20	μA	XT_{IN}, XT_{OUT}, X_{IN}, X_{OUT}	
	I_{LIH2}			3	μA	Other than above	
Low-Level Input Leakage Current	I_{LIL1}			−20	μA	XT_{IN}, XT_{OUT}, X_{IN}, X_{OUT}	
	I_{LIL2}			−3	μA	Other than above	
High-Level Output Current	I_{OH1}	−7	−15		mA	REM, V_{OH} = V_{DD} − 0.6 V	
	I_{OH2}	−0.8	−1.2		mA	**Note 1.** V_{OH} = V_{DD} − 0.3 V	
Low-Level Output Current	I_{OL}	1.0	1.5		mA	**Note 2.** V_{OL} = 0.3 V	
Internal Pull-up Resistor	R_{P0A}	140	200	350	kΩ	$P0A_0$-$P0A_3$	
	R_{RES}	27	47	94	kΩ	$\overline{RESET}$	
A/D Absolute Accuracy				±2	LSB		
A/D Resolution			8		BITS		
A/D Convertor Current Dissipation	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comarator mode	
Supply Current	I_{DD1}		1.8	5.0	mA	w/X (f_X = 4.19 MHz) w/o XT V_{DD} = 5 V	Operation mode
	I_{DD2}		0.6	2.0	mA		HALT mode
	I_{DD3}		2.6	20.0	μA		STOP mode
	I_{DD4}		10.5	40	μA	w/o X or STOP w/XT (f_{XT} = 32.768 kHz) V_{DD} = 5 V	Operation mode
	I_{DD5}		6.0	20	μA		HALT mode

Note 1. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, and $P1A_0$ to $P1A_2$ pins
2. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_2$ and REM pins

LCD CHARACTERISTICS (Ta = −20 to +75 °C, V_{DD} = 5 V ± 10 %)

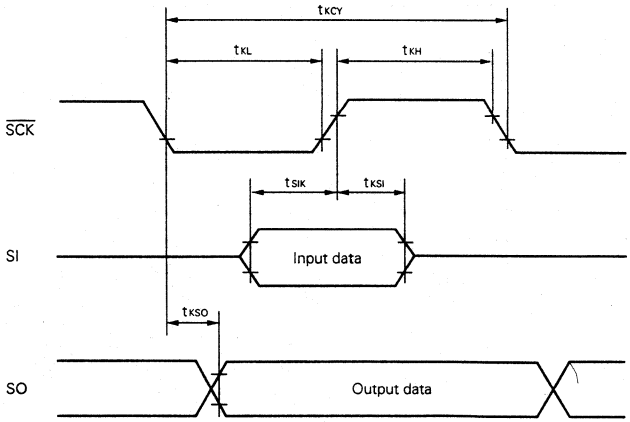
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
LCD Output Voltage Adjustable Range	V_{LCD0}	0.8		1.8	V	Value of external variable resistor: 0 to 2.2 MΩ
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 − C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 − C4 = 0.47 μF
LCD COMMON Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V
LCD SEGMENT Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V

AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

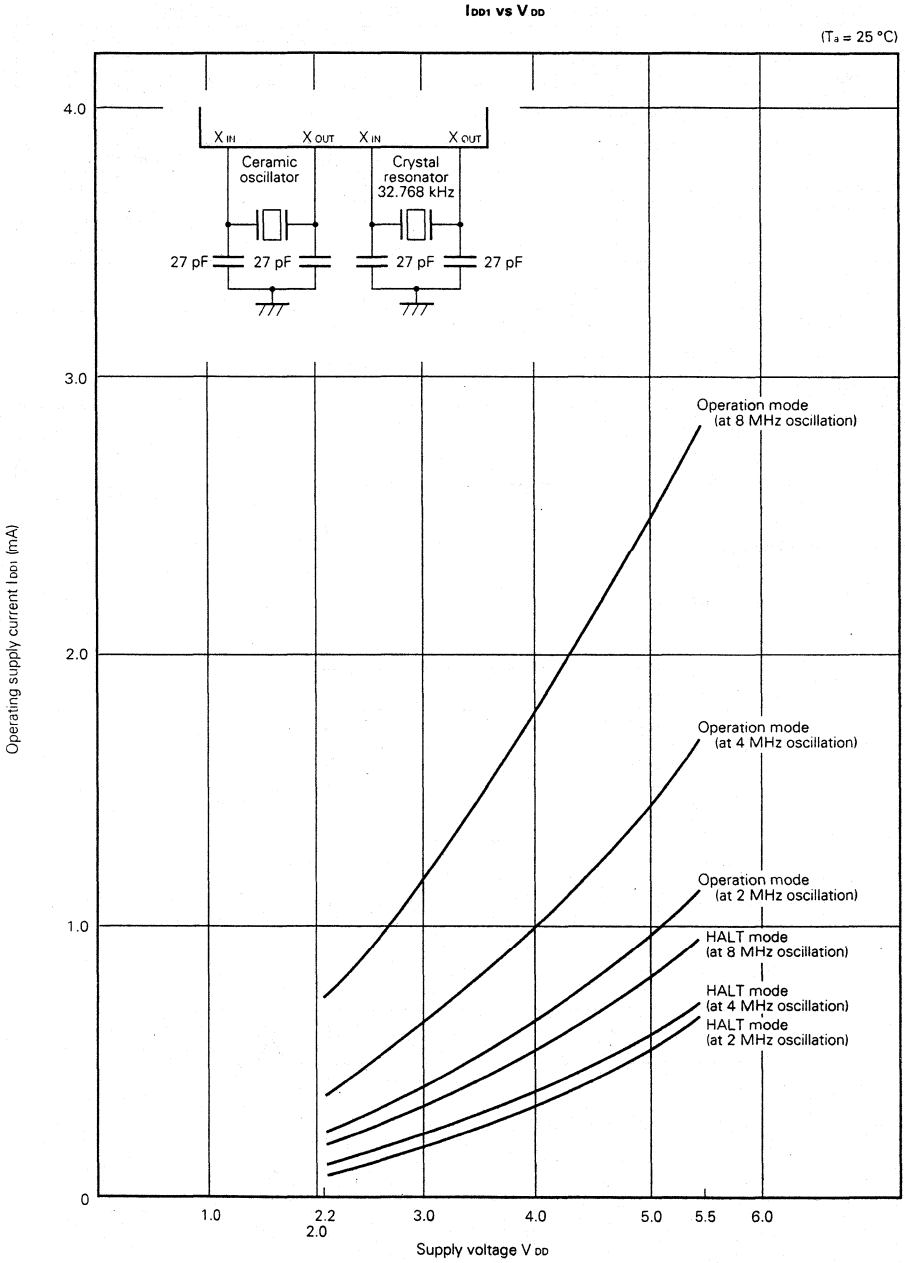
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
$\overline{SCK}$ Input Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 5 V± 10%	Data input
		10.0			μs		Data output
		5.0			μs		Data input
		13.0			μs		Data output
$\overline{SCK}$ Input High-/Low-Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 5 V± 10%	Data input
		5.0			μs		Data output
		2.5			μs		Data input
		6.5			μs		Data output
SI Setup Time (vs. $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI Hold Time (vs. $\overline{SCK}$↑)	t_{KSI}	100			ns		
$\overline{SCK}$↓ → SO Output Delay Time	t_{KSO}			4.5	μs	C_L = 100 pF	
INT High-Level Width	t_{IOH}	50			μs		
$\overline{RESET}$ Low-Level Width	t_{RSL}	50			μs		

Serial Transfer Timing

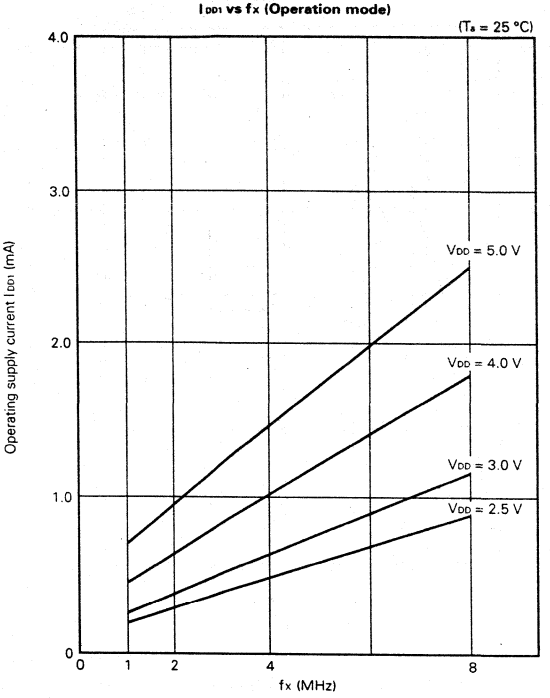
3-line serial I/O mode:



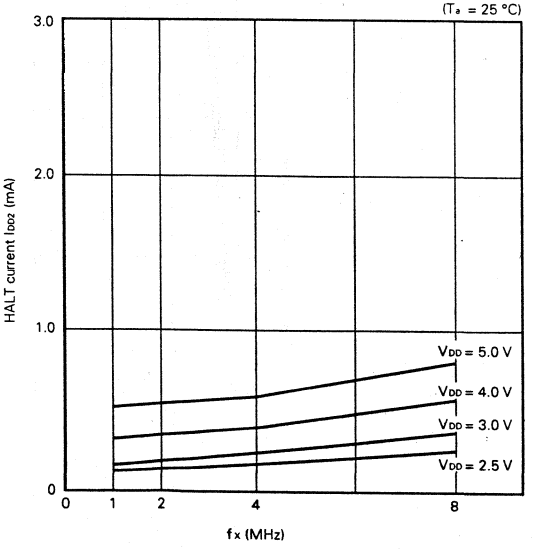
24. CHARACTERISTICS CURVE



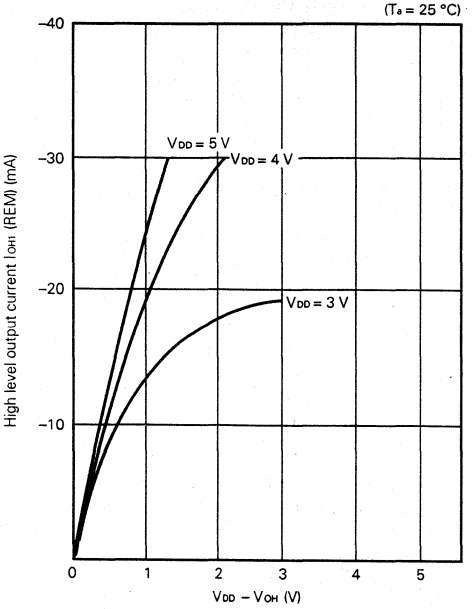
I_{DD1} vs fx (Operation mode)



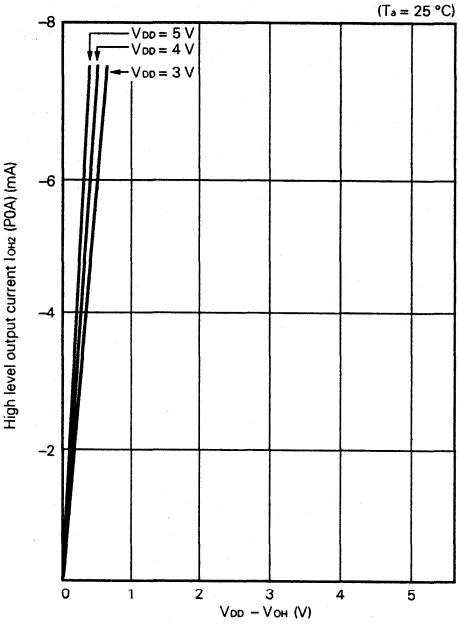
I_{DD2} vs fx (HALT mode)



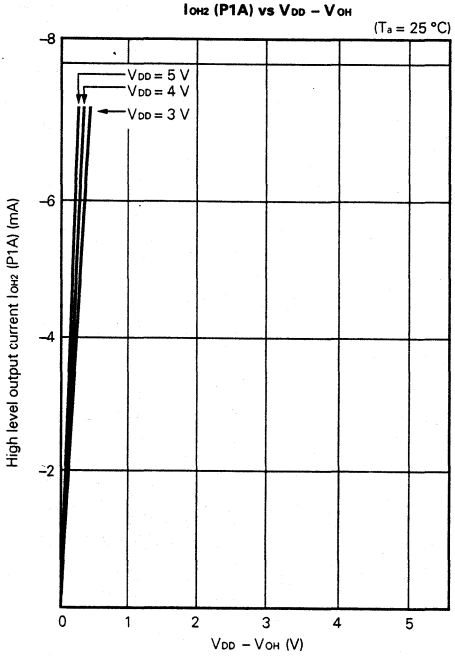
I_{OH1} (REM) vs $V_{DD} - V_{OH}$



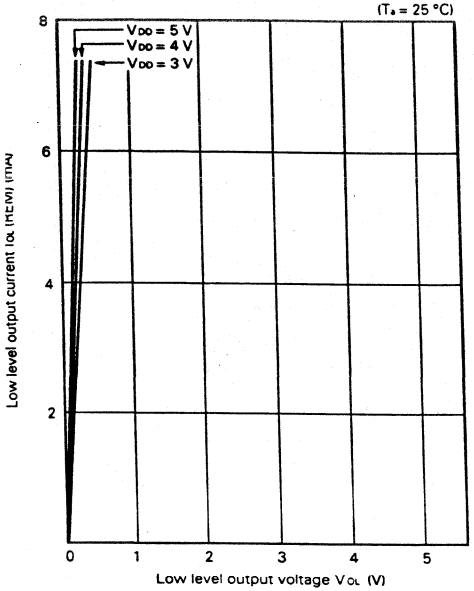
I_{OH2} (P0A) vs $V_{DD} - V_{OH}$



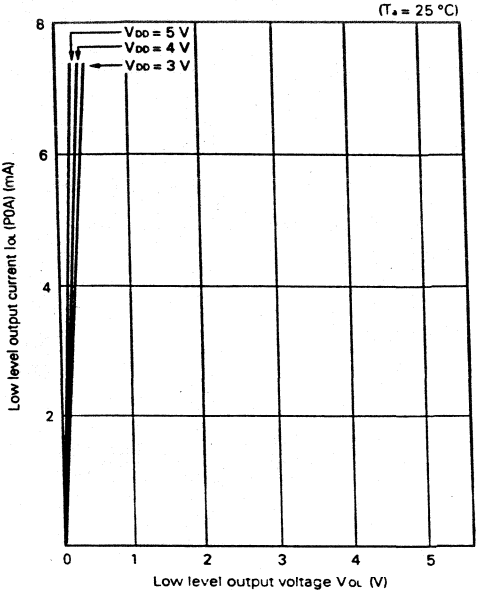
I_{OH2} (P1A) vs $V_{DD} - V_{OH}$



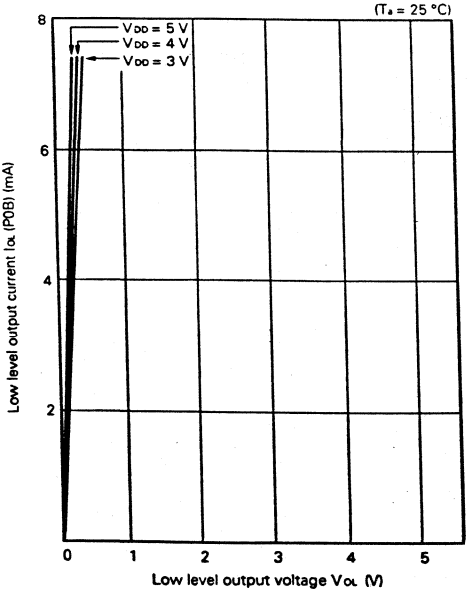
I_{OL} (REM) vs V_{OL}



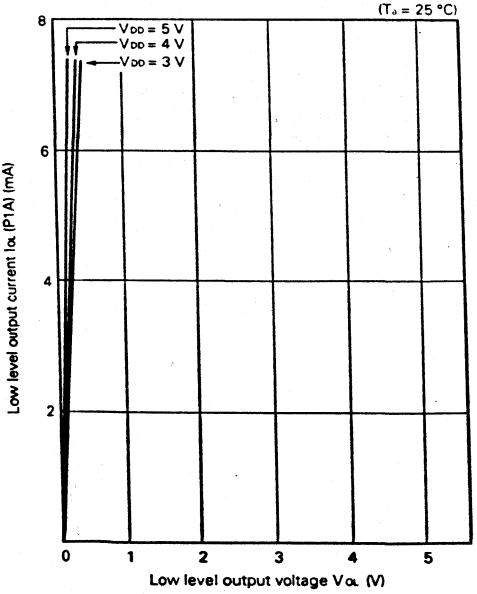
I_{OL} (P0A) vs V_{OL}



I_{OL} (P0B) vs V_{OL}

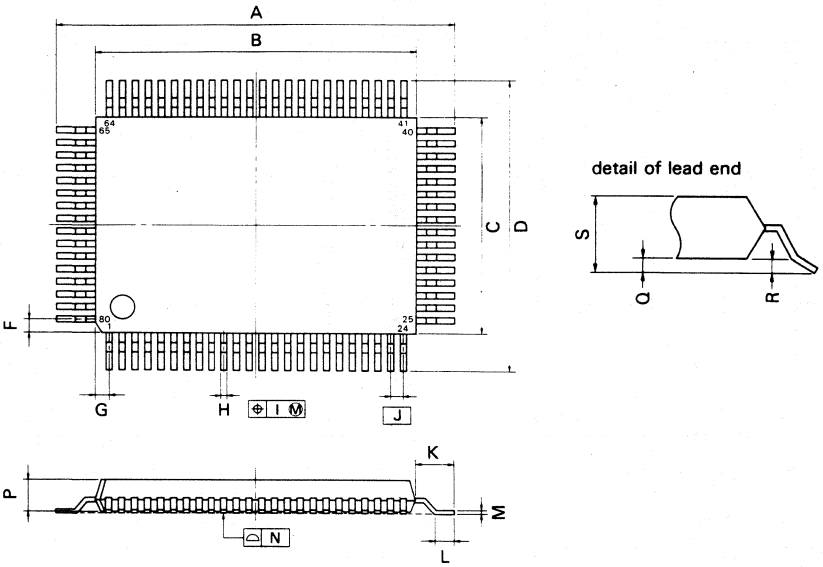


I_{OL} (P1A) vs V_{OL}



25. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×20)



S80GF-80-3B9

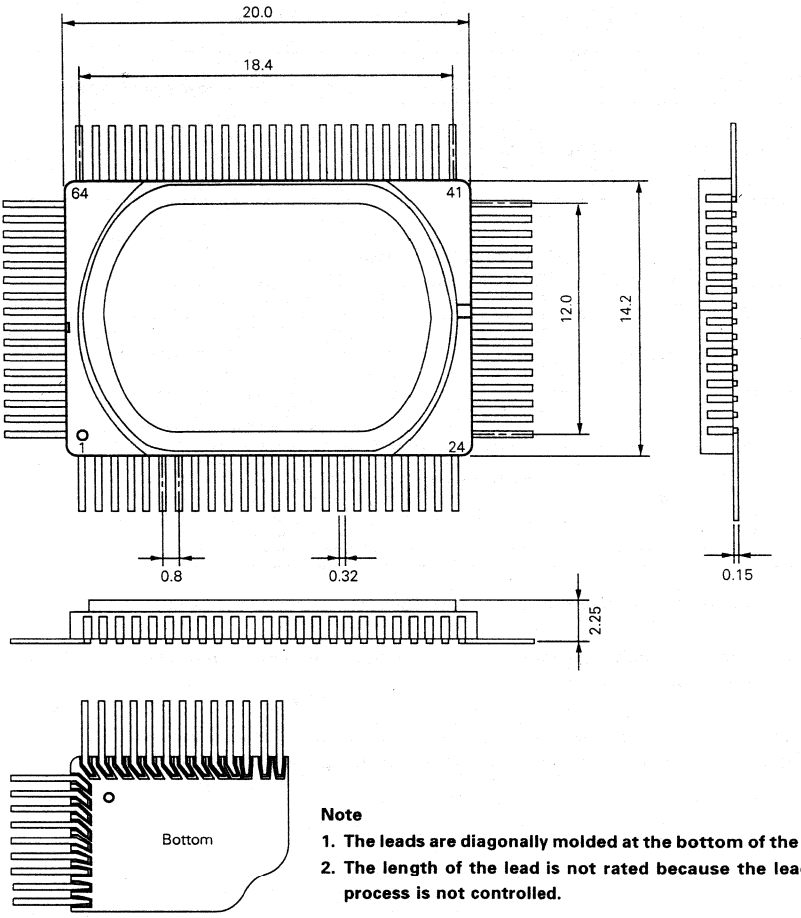
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{-0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{-0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{-0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

PACKAGE DIMENSION FOR ENGINEERING SAMPLE

80-PIN CERAMIC QFP (for reference) (Unit: mm)



Note

1. **The leads are diagonally molded at the bottom of the package.**
2. **The length of the lead is not rated because the lead cutting process is not controlled.**

26. RECOMMENDED SOLDERING CONDITIONS

Solder μPD17201A under the following conditions. For the soldering conditions and methods other than these, consult NEC.

Table 25-1 Recommended Soldering Conditions

Product name	Package	Symbol of recommended soldering condition
μPD17201AGF-xxx-3B9	80-pin plastic QFP (14 × 20 mm)	• IR30-162 • VP15-162 • WS60-162 • Partial heating

Table 25-2 Soldering Conditions

Symbol	Method	Conditions
IR30-162	Infrared reflow	Package peak temperature: 230 °C, time: 30 seconds max. (at 210 °C min.), number of times: once, storage days*: 2 days (after that, prebaking must be performed at 125 °C for 16 hours)
VP15-162	VPS	Package peak temperature: 215 °C, time: 40 seconds max. (at 200 °C min.), number of times: once, storage days*: 2 days (after that, prebaking must be performed at 125 °C for 16 hours)
WS60-162	Wave soldering	Solder bath temperature: 260 °C max., time: 10 seconds max., number of times: once, storage days*: 2 days (after that, prebaking must be performed at 125 °C for 16 hours)
—	Partial heating of pins	Pin temperature: 300 °C max., time: 10 seconds max.

* The storage days after the dry pack has been opened. The storage conditions are 25 °C and 65 % RH max.

Note Do not use different soldering methods together (however, the partial heating can be used with the other soldering methods).

Remarks For the details of the recommended soldering conditions of the surface mount type, refer to Information Material, "Surface Mount Device Mounting Manual" (IEI-1207).

APPENDIX A COMPARISON FOR μPD17201A RELATED PRODUCTS

Item \ Part number		μPD17201A	μPD17207	μPD17P207
ROM (bits)		3072 × 16	4096 × 16	
RAM (bits)		336 × 4		
Stack level		5 levels		
A / D converter		• 8-bit resolution × 4 chs • Capable of low-voltage operation: V_{DD} = 2.2 to 5.5 V		
Timer / counter		• 8-bit timer • Clock time (shared by watchdog timer)		
Serial interface		8-bit, 3-line serial interface: 1 ch		
Interrupt	Internal	Vectored interrupt: 1		
	External	Vectored interrupt: 3		
Remote control carrier generator		Provided		
Instruction execution time		4 μs (when 4 MHz, ceramic oscillator is used)		
Mask option		Provided		None
V_{PP}, PROM shared pin		None		Provided
Package		80-pin plastic QFP (14 × 20 mm)		

4-BIT SINGLE-CHIP MICROCONTROLLER WITH A/D CONVERTER AND LCD CONTROLLER/DRIVER FOR INFRARED REMOTE CONTROLLER

The μPD17207 is a 4-bit single-chip microcontroller integrating an LCD controller/driver, an A/D converter, and a carrier generator circuit for an infrared remote controller on a single chip.

This microcontroller employs the 17K architecture which enables arithmetic operations and data transfer between data memories or between data memory and a peripheral circuit by a single instruction. Each instruction of the μPD17207 is a 16-bit 1-word instruction.

The μPD17207 is housed in an 80-pin plastic quad flat package (QFP).

FEATURES

- 17K architecture
- Program memory (ROM) of 4096 × 16 bits
- Data memory (RAM) of 336 × 4 bits
- Built-in carrier generator for infrared remote controller
- Built-in 4-channel 8-bit A/D converter
- Built-in LCD controller/driver (enabling display of up to 136 segments) having 4 common pins (two of which can be used as segment pins), 34 segment pins, and an LCD driving voltage booster (by 2.4 to 5.4 V by external resistance)
- Abundant I/O ports available (19 ports)
- Built-in 3-line serial interface
- 5 stack levels (3 interrupt levels)
- 8-bit timer: 1 channel
- Clock timer: 1 channel
- Instruction executing time: 4 μs (with 4 MHz, ceramic oscillator/crystal resonator)
- Standby function (STOP and HALT) (In STOP mode, time can be displayed with a 32.768 kHz crystal resonator.)
- Wide operating voltage range: 2.2 to 5.5 V

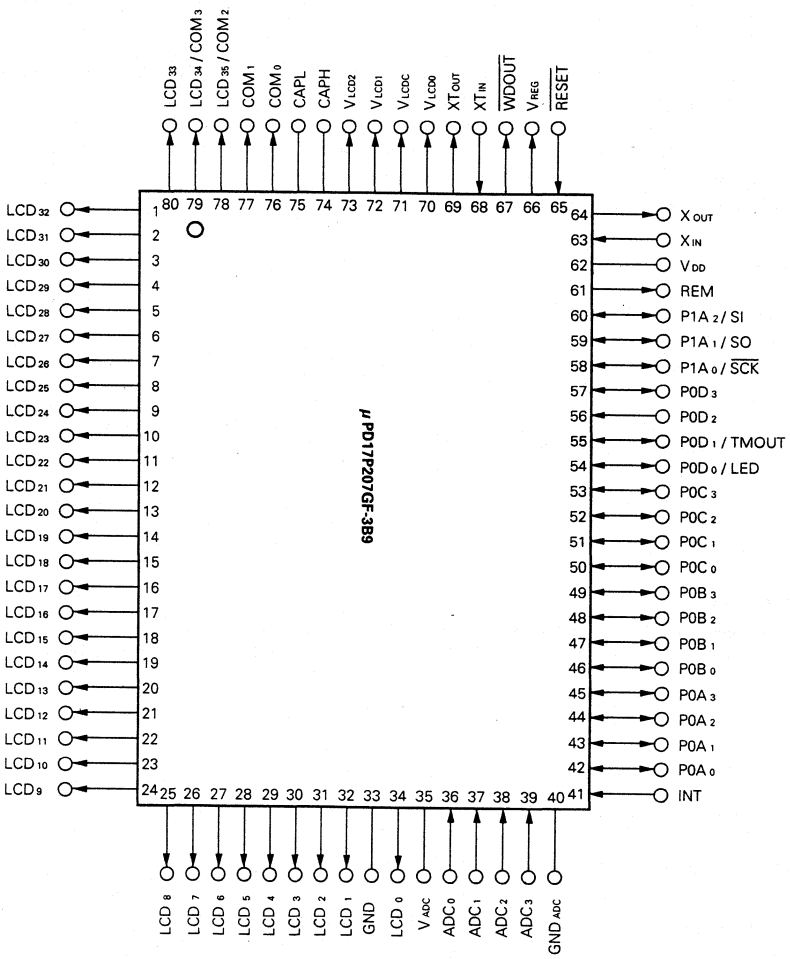
APPLICATIONS

- Infrared remote controller for air conditioner
- Infrared remote controller with LCD display

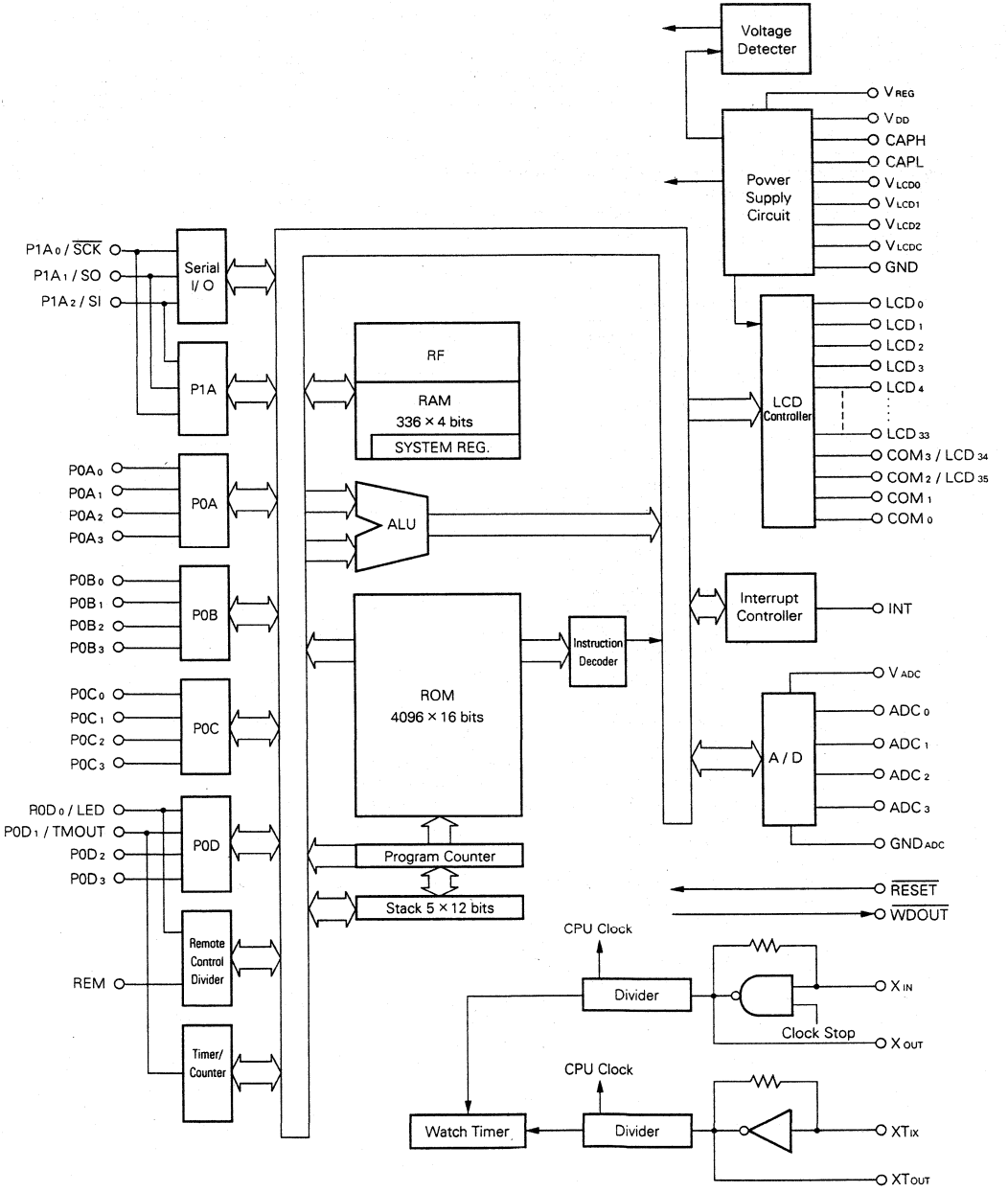
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17207GF-XXX-3B9	80-pin plastic QFP (14 mm × 20 mm)	Standard

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN IDENTIFICATION

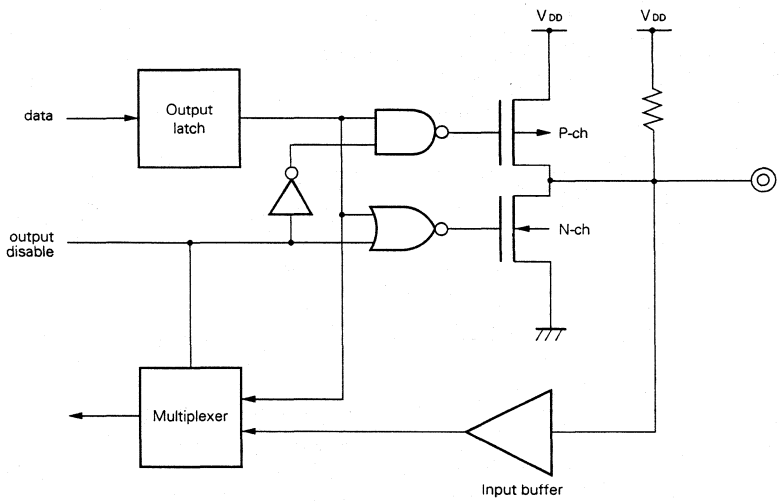
PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	ON RESET
76 77 78 79 80 1 to 32 34	COM_0 COM_1 LCD_{35}/COM_2 LCD_{34}/COM_3 LCD_{33} LCD_{32} to LCD_1 LCD_0	Common/segment signal outputs of the LCD driver. These common and segment signal outputs are selected by LCDMD3 to LCDMD0 of the register file. ● COM_0 to COM_3 • Common signal outputs of the LCD driver ● LCD_{35} to LCD_0 • Segment signal outputs of the LCD driver	CMOS, push-pull	Output (1/2 V_{DD})
33	GND	Device ground	—	—
35	V_{ADC}	Positive power supply of the A/D converter (V_{ADC} should be equal to V_{DD}.)	—	—
36 to 39	ADC_0 to ADC_3	Analog inputs of the A/D converter (8-bit resolution)	—	—
40	GND_{ADC}	Ground of the A/D converter	—	—
41	INT	External interrupt request signal (Input). The interrupt request is generated at the rising edge of this signal.	—	Input
42 to 45	$P0A_0$ to $P0A_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O). Each of these pins has a pull-up resistor.	CMOS, push-pull	Input
46 to 49	$P0B_0$ to $P0B_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O).	N-channel, open-drain	Input
50 to 53	$P0C_0$ to $P0C_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O).	N-channel, open-drain	Input
54 55 56 57	$P0D_0$/LED $P0D_1$/TMOUT $P0D_2$ $P0D_3$	Port 0D/LED output or port 0D/8-bit timer output. $P0D_0$ and LED outputs are switched by NRZEN of the register file. $P0D_1$ and 8-bit timer outputs are switched by TMOE of the register file. ● $P0D_0$ to $P0D_3$ • 4-bit I/O port • Enabling setting of inputs or outputs of each bit (Bitwise I/O) ● LED • Output to drive a visible-light LED ● TMOUT • Output of the 8-bit timer	CMOS, push-pull	Input

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	ON RESET
58 59 60	P1A0/$\overline{SCK}$ P1A1/SO P1A2/SI	Port 1A or serial interface. Port 1A and serial interface are switched by SIOEN of the register file. ● P1A0 to P1A2 • 3-bit I/O port • Enabling setting of inputs or outputs of 3 bits (Grouped I/O) ● $\overline{SCK}$, SO, SI $\overline{SCK}$: Serial clock I/O SO: Serial data output SI: Serial data input	CMOS, push-pull	Input
61	REM	Signal output to an infrared remote controller. This output drives infrared LEDs.	CMOS, push-pull	Low-level output
62	V_{DD}	Positive power supply.	—	—
63 64	X_{IN} X_{OUT}	These pins are connected to a 4 MHz ceramic or crystal oscillator for main clock oscillation.	—	(Oscillation stops.)
65	$\overline{RESET}$	Input of a system resetting signal.	—	Input
66	V_{REG}	Output of the voltage regulator for the subclock oscillation circuit. A capacitor of 0.1 μF should be connected to this pin.	—	—
67	$\overline{WDOUT}$	Output for detection of a program hung-up. This signal goes low when a watchdog timer and a stack overflows are generated.	CMOS, push-pull	High-level output
68 69	XT_{IN} XT_{OUT}	These pins are connected to a 32 kHz crystal oscillator for subclock oscillation.	—	(Oscillates.)
71	V_{LCDC}	Output to regulate the reference voltage to drive LCD.	—	—
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	Reference voltage outputs to drive LCD. • V_{LCD0}: Reference voltage output • V_{LCD1}: Doubler output (Two times the reference voltage) • V_{LCD2}: Tripler output (Three times the reference voltage)	—	—
74 75	CAPH CAPL	These pins are connected to a capacitor to boost the LCD drive voltage.	—	—

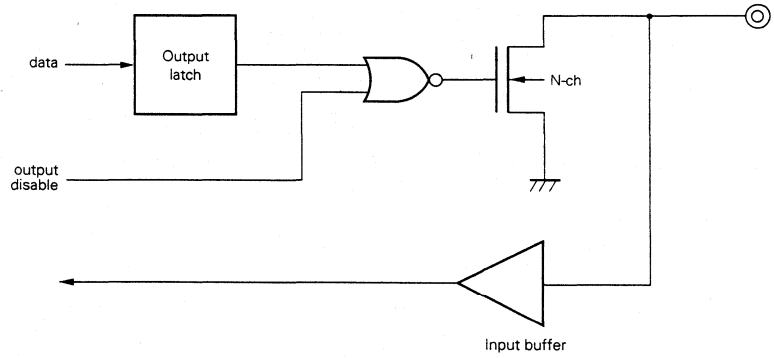
1.2 EQUIVALENT CIRCUITS OF PINS

Shown below are equivalent circuits (partially simplified) of the respective pins of the μPD17207.

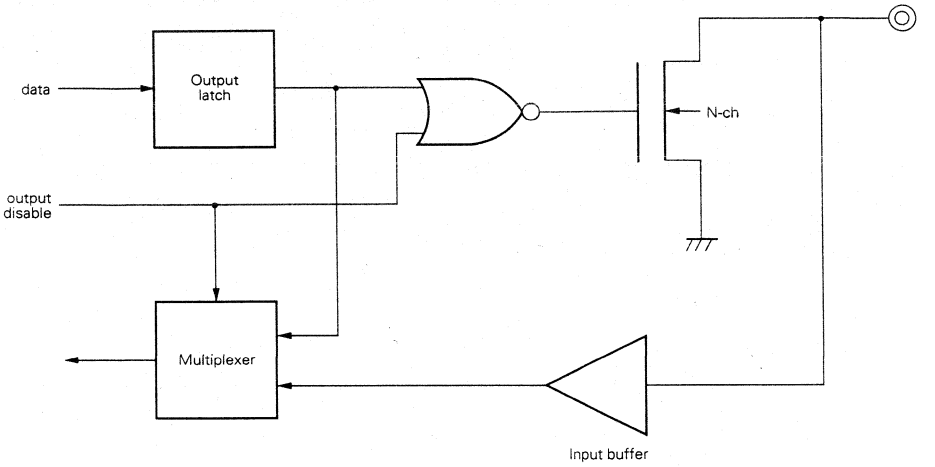
(1) $P0A_0$ to $P0A_3$



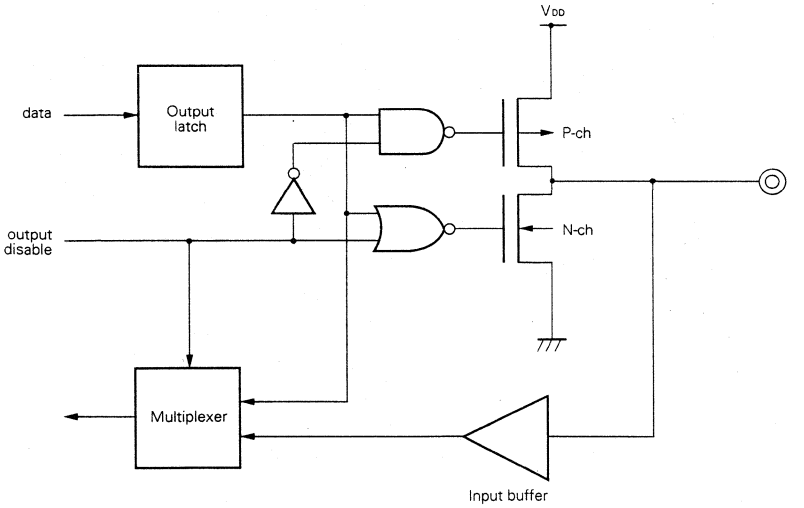
(2) $P0B_0$ to $P0B_3$



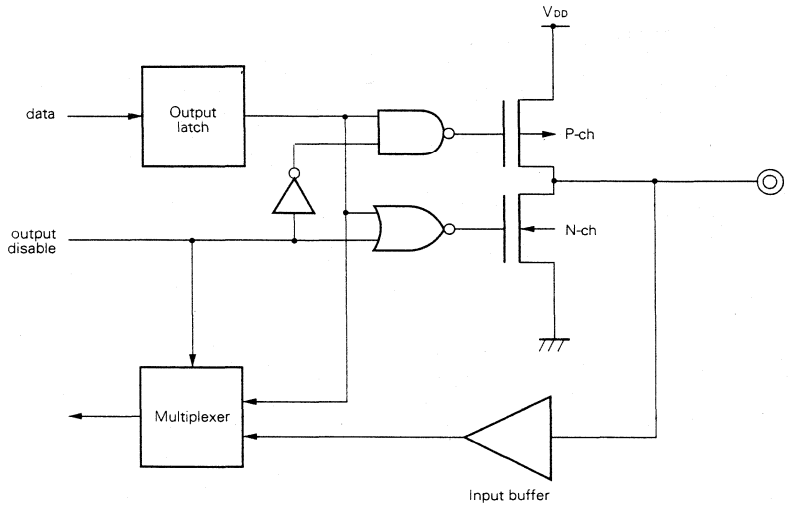
(3) $P0C_0$ to $P0C_3$



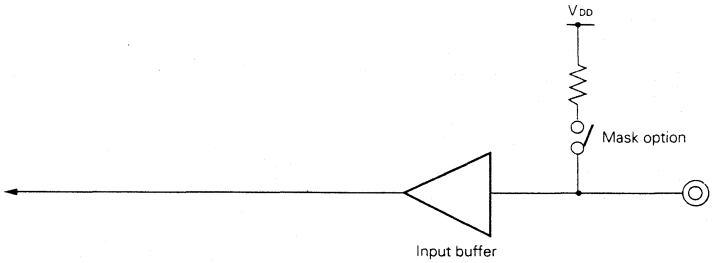
(4) $P0D_0$ to $P0D_3$



(5) $P1A_0$ to $P1A_2$



(6) $\overline{\text{RESET}}$



23. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	AV_{DD}			−0.3 to +7.0	V
Input Voltage	V_I			−0.3 to V_{DD} +0.3	V
Output Voltage	V_O			−0.3 to V_{DD} +0.3	V
High Output Current	I_{OH}	REM pin	Peak value	−30	mA
			Effective value	−20	mA
		One pin except REM	Peak value	−7.5	mA
			Effective value	−5	mA
		All pins except REM	Peak value	−22.5	mA
			Effective value	−15	mA
Low Output Current	I_{OL}	One pin except REM	Peak value	7.5	mA
			Effective value	5	mA
		All pins except REM	Peak value	22.5	mA
			Effective value	15	mA
Operating Temperature	T_{opt}			−20 to +75	°C
Storage Temperature	T_{stg}			−40 to +125	°C

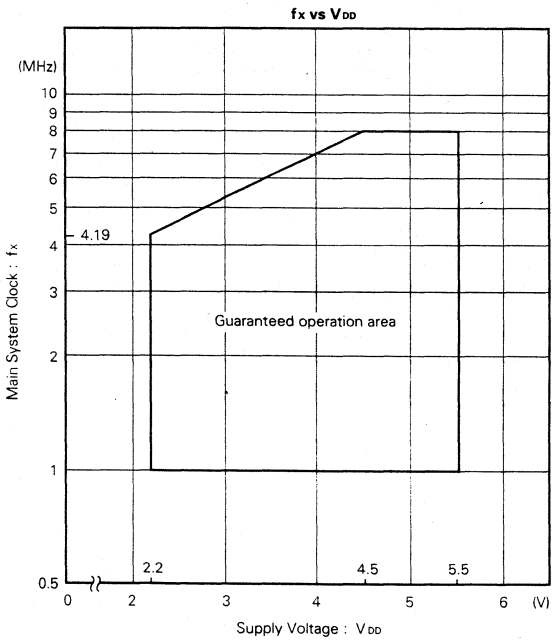
Note Effective value = Peak value × Duty

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

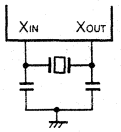
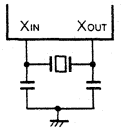
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			10	pF	INT, SI and $\overline{\text{RESET}}$ pins

RECOMMENDED OPERATING RANGES

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock f_X = 4 MHz
	V_{DD2}	4.5	5.0	5.5	V	System clock f_X = 8 MHz
	V_{DD3}	2.0	3.0	5.5	V	System clock f_{XT} = 32 kHz
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

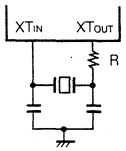
Resonator	Recommended constants	Item	Condition	MIN.	TYP.	MAX.	Unit
Ceramic Oscillator Note 3		Oscillation frequency (fx) Note 1		1.0	4.19	8.0	MHz
		Oscillation stabilization time Note 2	From when V_{DD} reaches the minimum oscillation voltage			4	ms
Crystal Oscillator Note 3		Oscillation frequency (fx) Note 1		1.0	4.19	8.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms

Note 1. The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2. The oscillation stabilization time is the time required for stabilizing the oscillation after V_{DD} is applied or the STOP mode is released.

3. The recommended oscillators are shown in the table described. later.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS

Resonator	Recommended constants	Item	Condition	MIN.	TYP.	MAX.	Unit
Crystal oscillator Note 3		Oscillation frequency (fXT)			32.768		kHz
		Oscillation stabilization time			5	10	s

Note When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the following notations must be read and observed for wiring within the shaded area in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line.**
- **Capacitors used in the oscillators must always be grounded to V_{SS} potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

RECOMMENDED OSCILLATORS

MAIN SYSTEM CLOCK OSCILLATOR (MADE OF CERAMIC)

Manufacturer	Part name	External capacitance (pF)		Oscillation voltage range (V)		Remarks
		C1	C2	MIN.	MAX.	
MURATA Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	Not required	Not required	2.0	6.0	Built-in capacitor
	CST4.00MGW	Not required	Not required	2.0	6.0	
	CST4.19MGW	Not required	Not required	2.0	6.0	
KYOCERA	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
TOKO	CRHF4.00	18	18	2.0	6.0	
DAISHINKU	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK OSCILLATOR (MADE OF CRYSTAL)

Manufacturer	Frequency (MHz)	Holder	External capacitance (pF)		Oscillation voltage range (V)		Remarks
			C1	C2	MIN.	MAX.	
KINSEKI	4.0	HC-49U-S	22	22	2.0	6.0	

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Low-Level Detection Voltage 0	V_{DET0}	1.6	2.0	2.8	V		
Low-Level Detection Voltage 1	V_{DET1}	1.9	2.3	3.4	V		
Input High Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ and INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ and INT pins	
Input Low Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ and INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ and INT pins	
High Input Leakage Current	I_{LIH1}			20	μA	X_{TIN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIH2}			3	μA	Other than X_{TIN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
Low Input Leakage Current	I_{LIL1}			−20	μA	X_{TIN}, XT_{OUT}, X_{IN} and X_{OUT} pins	
	I_{LIL2}			−3	μA	Other than X_{TIN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
High Output Current	I_{OH1}	−7	−15		mA	REM pin	V_{OH} = V_{DD} − 1.2 V
	I_{OH2}	−0.3	−0.7		mA	**Note 1**	V_{OH} = V_{DD} − 0.3 V
Low Output Current	I_{OL}	0.5	0.9		mA	**Note 2**	V_{OL} = 0.3 V
Built-in Pullup Resistor	R_{P0A}	100	200	350	kΩ	$P0A_0$ to $P0A_3$ pins	
	R_{RES}	24	47	94	kΩ	$\overline{\text{RESET}}$ pins	
A/D Absolute Precision				±2	LSB		
A/D Resolution			8		BITS		
A/D Converter Circuit Current	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comparator mode	
Supply Current	I_{DD1}		0.8	2.0	mA	X installed (f_X = 4.19 MHz) XT not installed V_{DD} = 3 V	RUN mode
	I_{DD2}		0.3	1.5	mA		HALT mode
	I_{DD3}		2.0	10.0	μA		STOP mode
	I_{DD4}		7.0	25	μA	X not installed or STOP XT installed (f_{XT} = 32 kHz) V_{DD} = 3 V	RUN mode
	I_{DD5}		3.0	15	μA		HALT mode

Note 1. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, and $P1A_0$ to $P1A_2$ pins

2. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_2$, and REM pins

LCD CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LCD Output Voltage Range	V_{LCD0}	0.8		1.8	V	External variable resistance (0 to 2.2 MΩ)
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 to C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 to C4 = 0.47 μF
LCD Common Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V
LCD Segment Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V±10 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Low-Level Detection Voltage 0	V_{DET0}	1.6	2.0	2.8	V		
Low-Level Detection Voltage 1	V_{DET1}	1.9	2.3	3.4	V		
Input High Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ and INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ and INT pins	
Input Low Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ and INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ and INT pins	
High Input Leakage Current	I_{LIH1}			20	μA	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIH2}			3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
Low Input Leakage Current	I_{LIL1}			−20	μA	XT_{IN}, XT_{OUT}, X_{IN} and X_{OUT} pins	
	I_{LIL2}			−3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
High Output Current	I_{OH1}	−7	−15		mA	REM pin	$V_{OH} = V_{DD} - 0.6$ V
	I_{OH2}	−0.8	−1.2		mA	**Note 1**	$V_{OH} = V_{DD} - 0.3$ V
Low Output Current	I_{OL}	1.0	1.5		mA	**Note 2**	V_{OL} = 0.3 V
Built-in Pullup Resistor	R_{P0A}	140	200	350	kΩ	$P0A_0$ to $P0A_3$ pins	
	R_{RES}	27	47	94	kΩ	$\overline{\text{RESET}}$ pins	
A/D Absolute Precision				±2	LSB		
A/D Resolution			8		BITS		
A/D Converter Circuit Current	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comparator mode	
Supply Current	I_{DD1}		1.8	5.0	mA	X installed (f_X = 4.19 MHz) XT not installed V_{DD} = 5 V	RUN mode
	I_{DD2}		0.6	2.0	mA		HALT mode
	I_{DD3}		2.6	20.0	μA		STOP mode
	I_{DD4}		10.5	40	μA	X not installed or STOP XT installed (f_{XT} = 32.768 kHz) V_{DD} = 5 V	RUN mode
	I_{DD5}		6.0	20	μA		HALT mode

Note 1. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, and $P1A_0$ to $P1A_2$ pins

2. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_2$, and REM pins

LCD CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V±10 %)

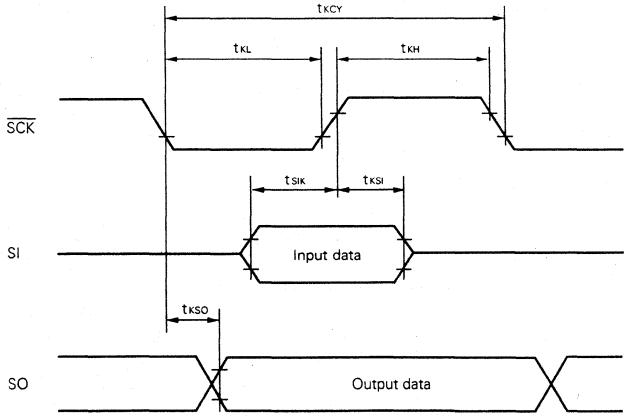
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
LCD Output Voltage Range	V_{LCD0}	0.8		1.8	V	External variable resistance (0 to 2.2 MΩ)
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 to C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 to C4 = 0.47 μF
LCD Common Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V
LCD Segment Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V

AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

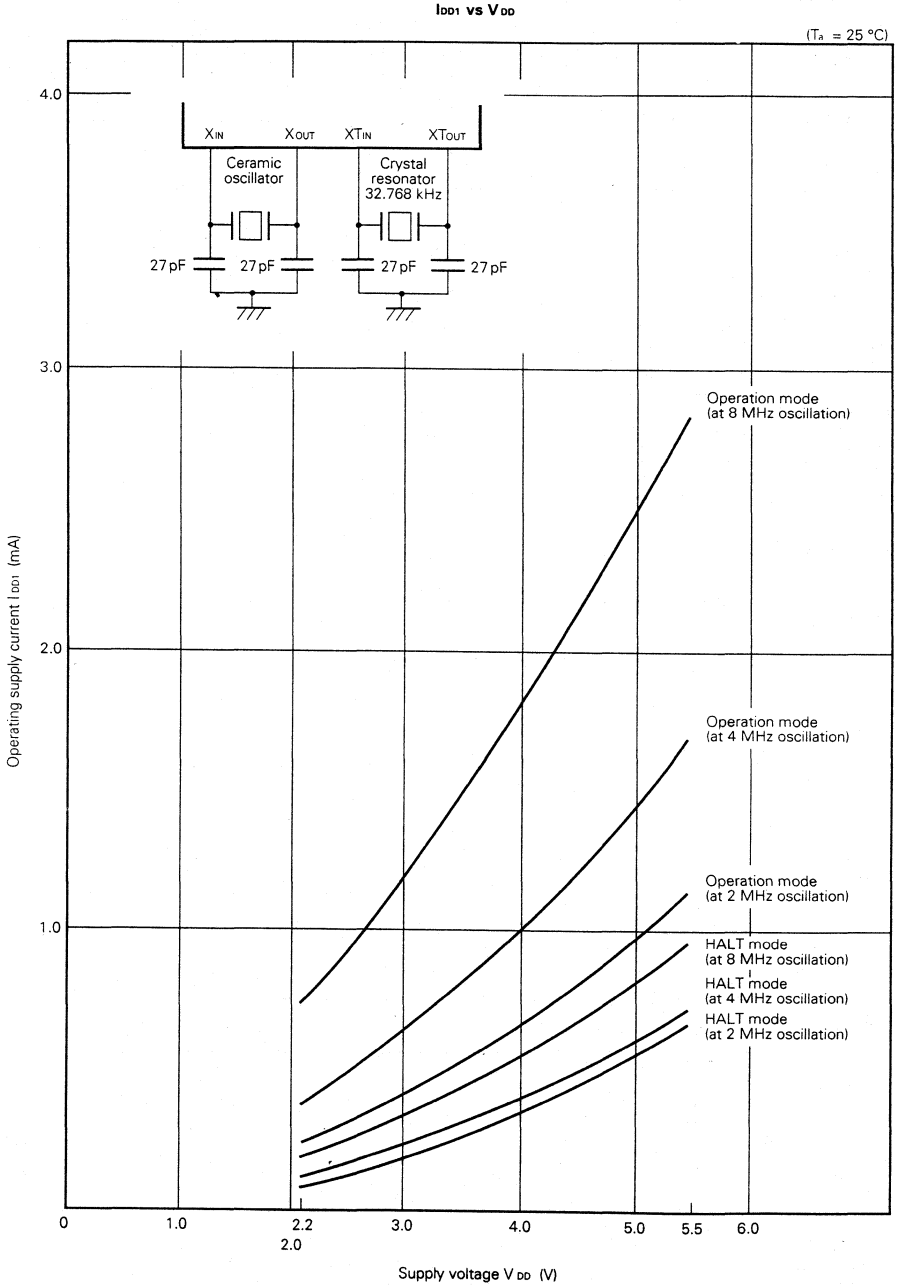
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
$\overline{SCK}$ input cycle time	t_{KCY}	2.0			μs	V_{DD} = 5 V±10 %	Data Input
		10.0			μs		Data Output
		5.0			μs		Data Input
		13.0			μs		Data Output
$\overline{SCK}$ input high- and low-widths	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 5 V±10 %	Data Input
		5.0			μs		Data Output
		2.5			μs		Data Input
		6.5			μs		Data Output
SI setup time (vs. $\overline{SCK}$↑)	t_{SIK}	100			ns		
SI hold time (vs. $\overline{SCK}$↑)	t_{KSI}	100			ns		
$\overline{SCK}$↓→ to SO output delay time	t_{KSO}			4.5	μs	C_L = 100 pF	
INT high-level width	t_{IOH}	50			μs		
$\overline{RESET}$ low-level width	t_{RSL}	50			μs		

Serial Transfer Timing

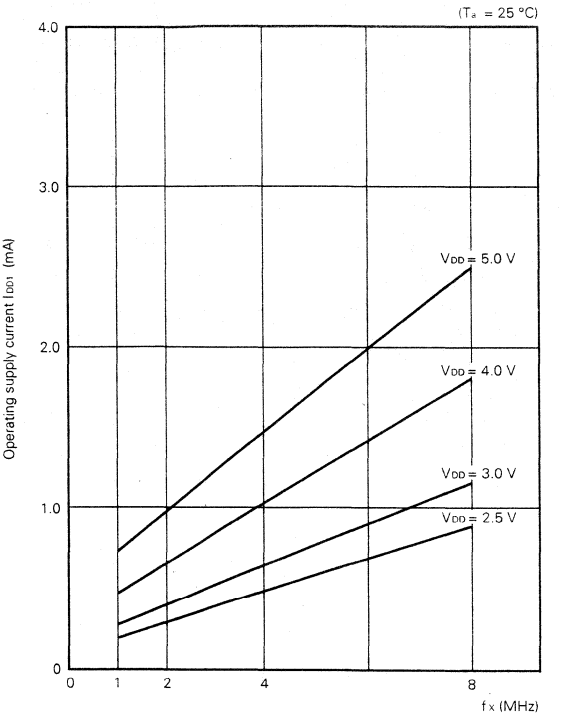
3-line Serial I/O Mode



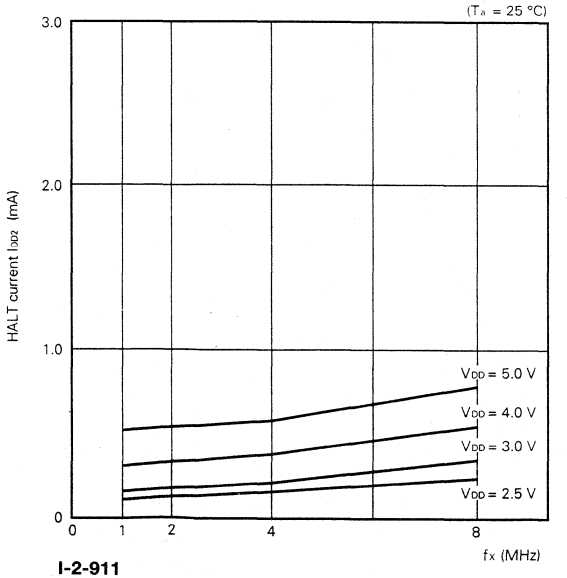
24. CHARACTERISTICS CURVE



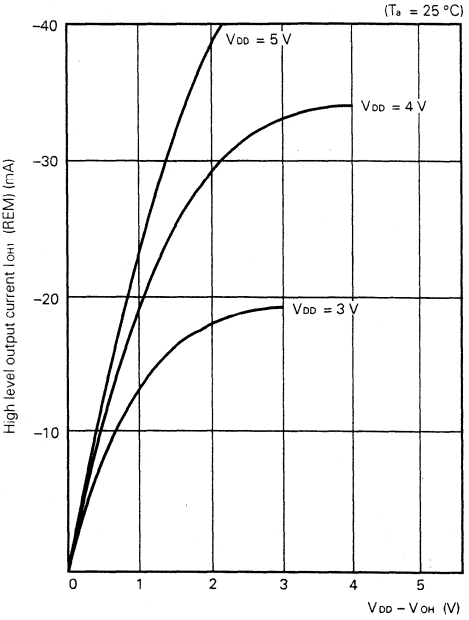
I_{DD1} vs f x (Operation mode)



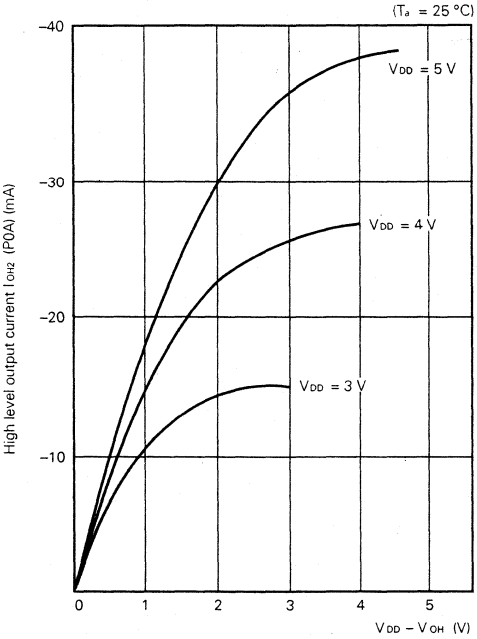
I_{DD2} vs f x (HALT mode)



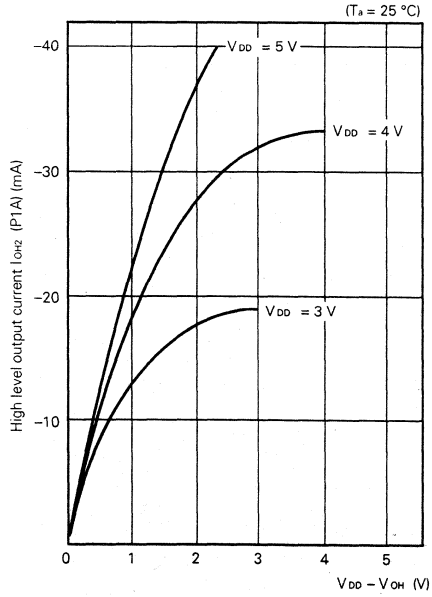
I_{OH1} (REM) vs $V_{DD} - V_{OH}$



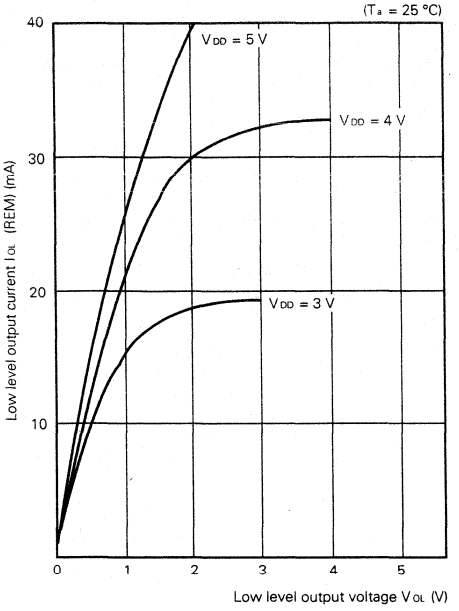
I_{OH1} (P0A) vs $V_{DD} - V_{OH}$



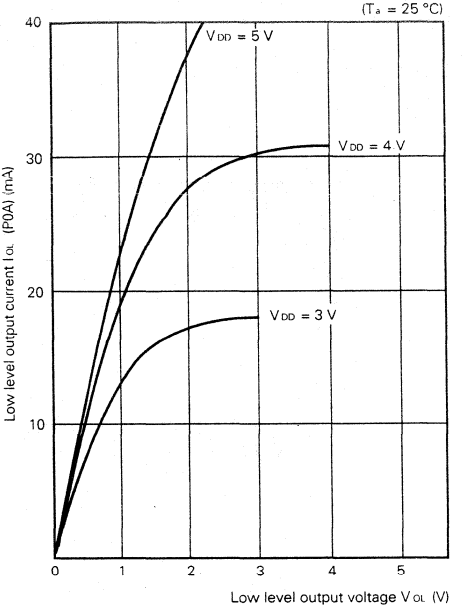
I_{OH2} (P1A) vs $V_{DD} - V_{OH}$



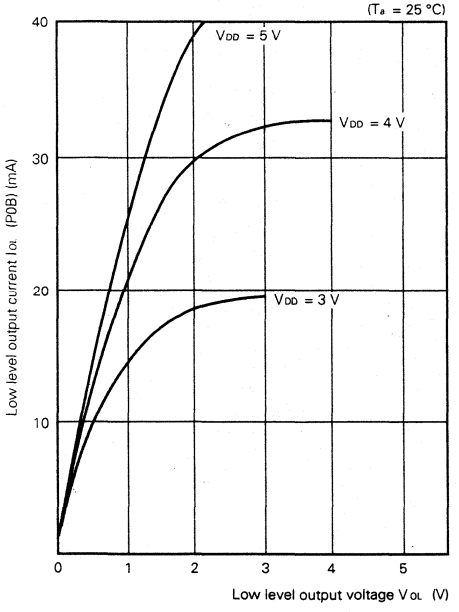
I_{OL} (REM) vs V_{OL}



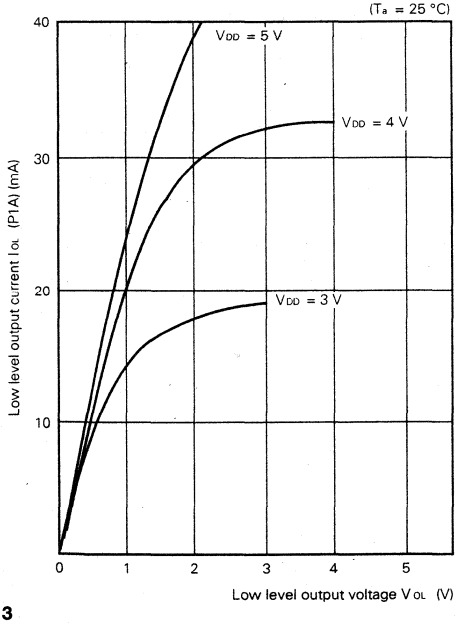
I_{OL} (P0A) vs V_{OL}



I_{OL} (P0B) vs V_{OL}

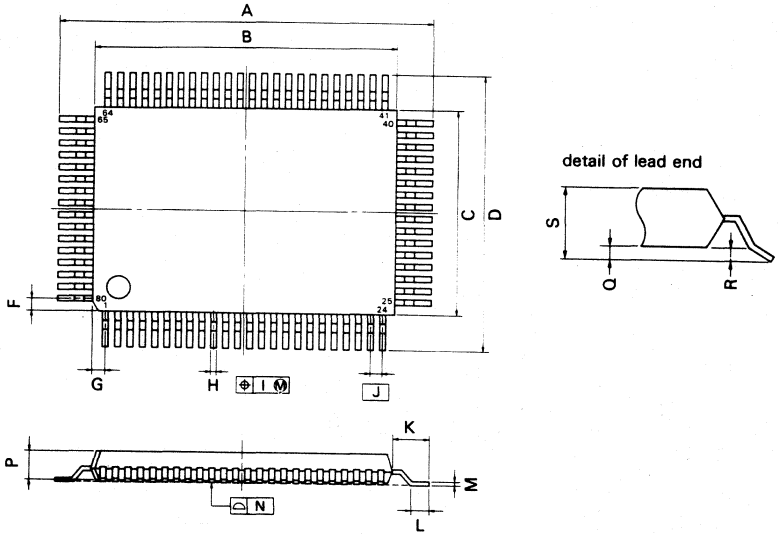


I_{OL} (P1A) vs V_{OL}



25. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×20)

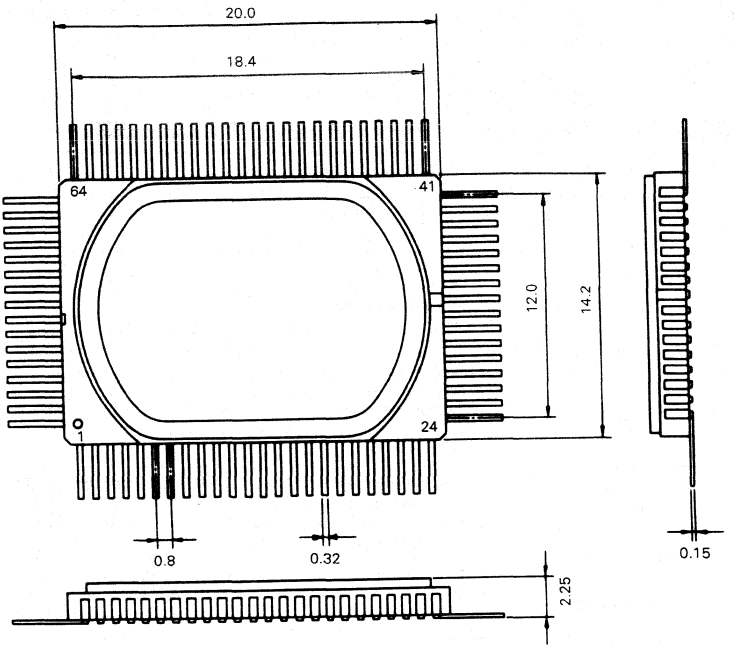


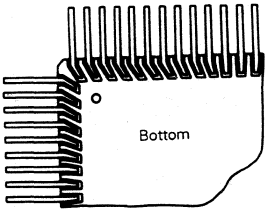
S80GF-80-3B9

NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.008}_{-0.009}$
C	$14^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

ES 80-Pin Ceramic QFP (For Reference) (Unit: mm)





Note 1. Leads on the bottom of the package are guided slantingly.

2. Package length does not include end flash burr.

26. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD17207 by soldering, soldering should be performed under the following recommended contitions.
For other soldering methods, please consult with NEC sales personnel.

Table 16-1 Recommended Soldering Conditions

Product name	Package	Recommended conditions reference code
μPD17207GF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)	• IR-30-162 • VP15-162 • WS60-162 • Pin partial heating

Table 26-2 Soldering Conditions

Recommended conditions reference code	Soldering method	Soldering conditions
IR30-162	Infrared reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of soldering operations; 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
VP15-162	VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of soldering operations; 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
WS60-162	Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max. Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
Pin partial heating	Pin partial heating	Pin temperature: 300 °C max., Timer: 10 seconds max.

* Number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 %RH max.

Note Do not use different soldering methods together (however, pin partial heating can be performed with other soldering methods.)

Remarks For details on recommended soldering conditions for surface mounting, refer to the information document "Surface Mount Device Mounting Manual" (IEI-1207).

APPENDIX A COMPARISON FOR μPD17207 RELATED PRODUCTS

Item \ Part number		μPD17201A	μPD17207	μPD17P207
ROM (bits)		3072 × 16	4096 × 16	
RAM (bits)		336 × 4		
Stack level		5 levels		
A/D converter		• 8-bit resolution × 4 chs • Capable of low-voltage operation: V_{DD} = 2.2 to 5.5 V		
Timer/counter		• 8-bit timer • Clock timer (shared by watch dog timer)		
Serial interface		8-bit, 3-line serial interface: 1ch		
Interrupt	Internal	Vectored interrupt: 1		
	External	Vectored interrupt: 3		
Remote control carrier generator		Provided		
Instruction execution time		3 μs (when 4 MHz ceramic oscillator is used)		
Mask option		Provided		None
V_{PP}, PROM shared pin		None		Provided
Package		80-pin plastic QFP (14 × 20 mm)		

4-BIT SINGLE-CHIP MICROCONTROLLER WITH LCD CONTROLLER/DRIVER AND A/D CONVERTER FOR INFRARED REMOTE CONTROLLER

μPD17P207 is a model of μPD17207 which is equipped with a one-time PROM in place of the μPD17207 internal mask ROM.

Sice the user can write the program to μPD17P207, the microcontroller is suitable for experimental or small-scale production of μPD17207 systems.

It is recommended that you also read the documents related to μPD17207, in addition to this data sheet.

FEATURES

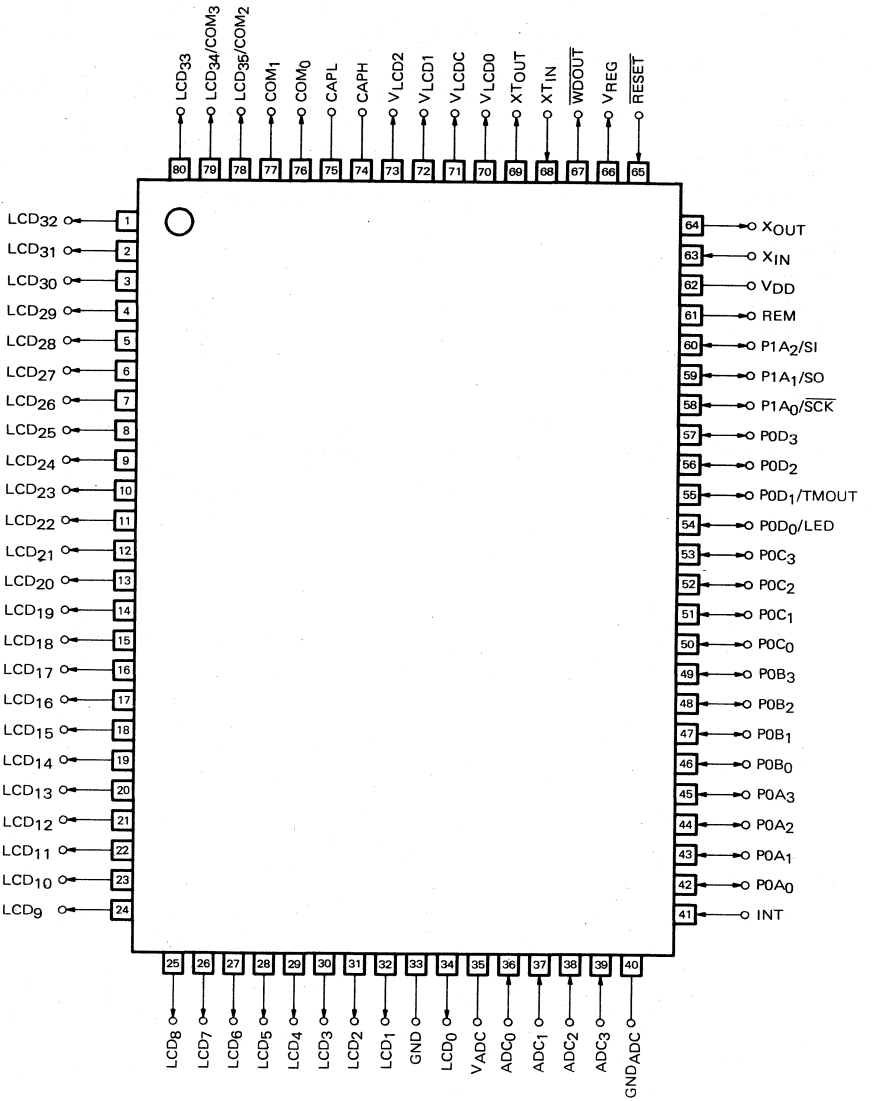
- Compatible with μPD17207
- Internal one-time PROM: 4096 x 16 bits
- Operating voltage range: 2.2 to 5.5 V

ORDERING INFORMATION

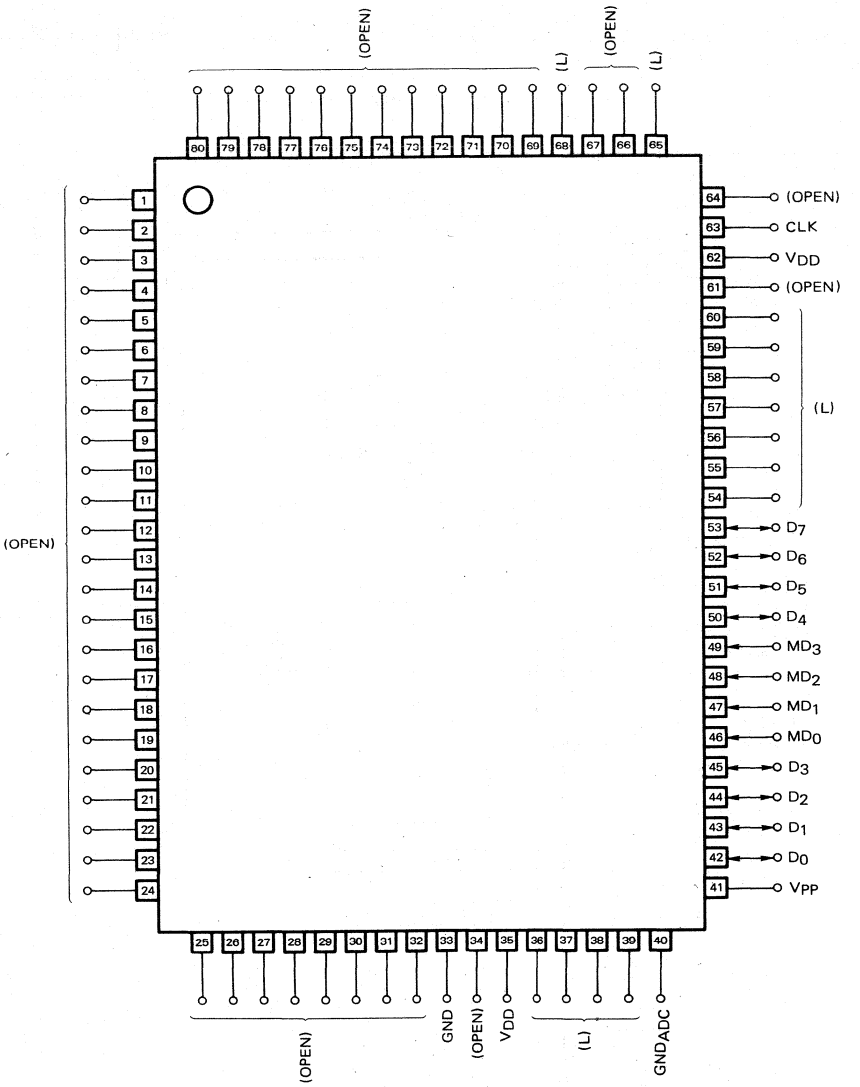
Order Code	Package	Quality Grade
μPD17P207GF-3B9	80-pin-plastic QFP (14 x 20)	Standard

PIN CONFIGURATION (Top View)

(1) Normal operation mode



(2) PROM programming mode

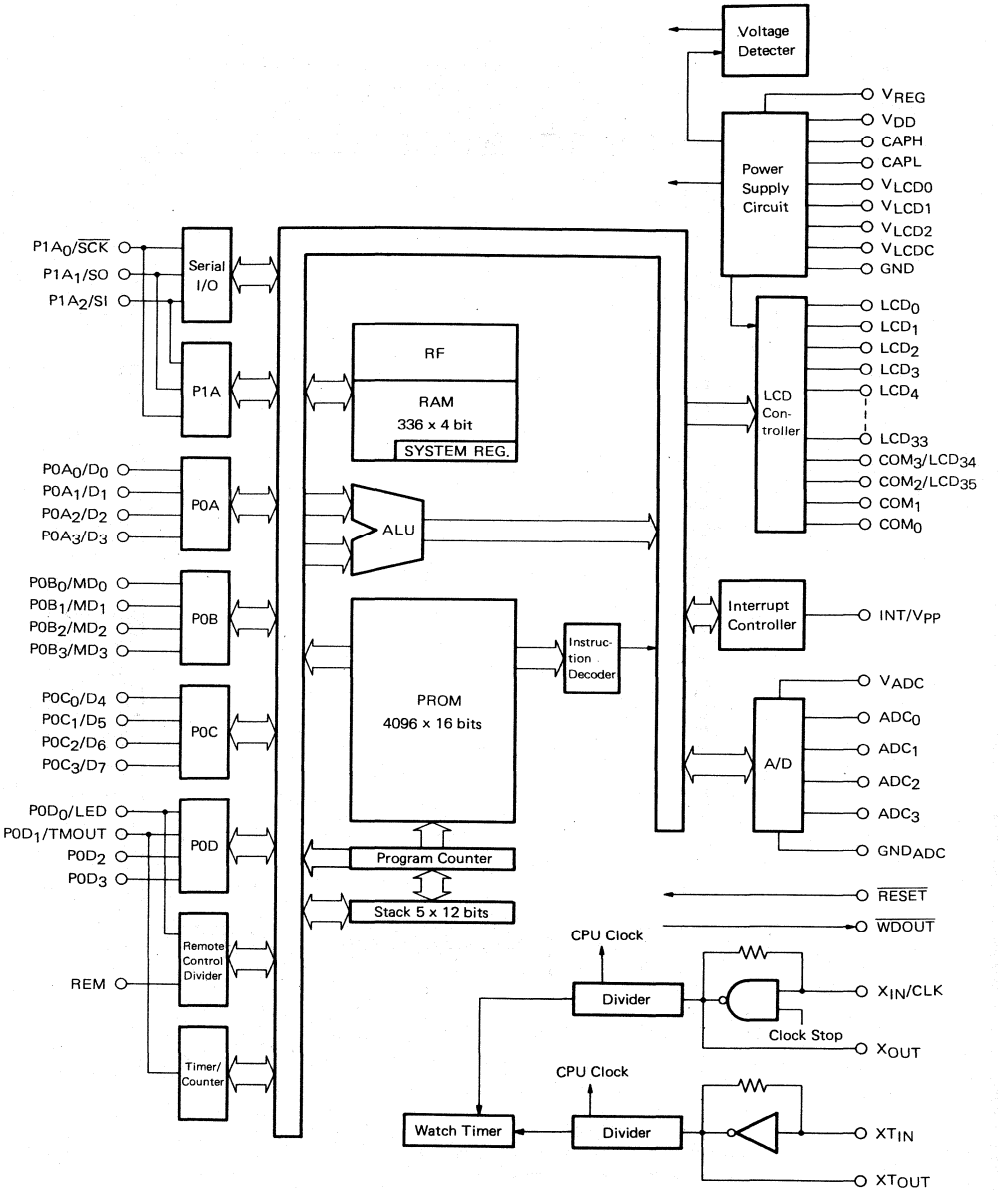


Note : ( ) indicates processing for pins not used in the PROM programming mode.

L : Ground each of these pins through a 470 Ω resistor.

OPEN : Do not connect anything to these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET

76
77
78
79
80
1
⋮
32
34
	COM0
	COM1
	LDC_{35}/COM_2
	LDC_{34}/COM_3
	LDC_{33}
	LDC_{32}
	⋮
	LDC_1
	LDC_0
		Output pins for common and segment signals of LCD driver. The LCDMD3 to LCDMD0 bits on the register file are used to switch the segment signal output to the common signal output or vice versa.
		• COM_0-COM_3
		  • Common signal output of LCD driver
		• LCD_{35}-LCD_0
		  • Segment signal output of LCD driver
			CMOS push-pull	Output ($1/2\ V_{DD}$)

33	GND	Ground	–	–
35	V_{ADC}	Positive power supply of A/D converter. Use $V_{ADC} = V_{DD}$.	–	–
36 ⋮ 39	ADC_0 ⋮ ADC_3	Analog input of 8-bit resolution A/D converter.	–	–
40	GND_{ADC}	A/D converter ground	–	–
41	INT	Inputs an external interrupt request signal. The interrupt request occurs at the rising edge of the input signal.	–	Input
42 ⋮ 45	$P0A_0$ ⋮ $P0A_3$	4-bit I/O port. Input/output can be set in 4-bit units (group I/O). Pull-up resistors are internally connected to these pins.	CMOS push-pull	Input
46 ⋮ 49	$P0B_0$ ⋮ $P0B_3$	4-bit I/O port. Input/output can be set in 4-bit units (group I/O).	N-ch open-drain	Input
50 ⋮ 53	$P0C_0$ ⋮ $P0C_3$	4-bit I/O port. Input/output can be set in 4-bit units (group I/O).	N-ch open-drain	Input

54
55
56
57
	$P0D_0$/LED
	$P0D_1$/TMOUT
	$P0D_2$
	$P0D_3$
		Port 0D, LED output, and 8-bit timer output. The NRZEN bit on the register file is used to switch $P0D_0$ to the LED output or vice versa. The TMOE bit on the register file is used to switch $P0D_1$ to the 8-bit timer output or vice versa.
		• $P0D_0$-$P0D_3$
		  • 4-bit I/O port
		  • Input/output can be set in bit units (bit I/O).
		• LED
		  • Visible LED drive output
		• TMOUT
		  • 8-bit timer output
			CMOS push-pull	Input

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET

58
59
60
	$P1A_0/\overline{SCK}$
	$P1A_1/SO$
	$P1A_2/SI$
		Port 1A and serial interface. The SIOEN bit on the register file is used to switch port 1A to the serial interface or vice versa.
		• $P1A_0$-$P1A_3$
		  • 3-bit I/O port
		  • Input/output can be set in 3-bit units (group I/O).
		• $\overline{SCK}$, SO, SI
		  • $\overline{SCK}$: Serial clock input/output
		  • SO : Serial data output
		  • SI : Serial data input
			CMOS push-pull	Input

61	REM	Output pin for infrared remote controller signal. Drives an infrared LED.	CMOS push-pull	Low-level output
62	V_{DD}	Positive power supply	–	–
63 64	X_{IN} X_{OUT}	Connect a 4 MHz ceramic oscillator or crystal oscillator for main clock oscillation.	–	(Oscillation stop)
65	$\overline{RESET}$	Input pin for system reset	–	Input
66	V_{REG}	Output pin of voltage regulator for subclock oscillation circuit. Connect a 0.1 μF capacitor to this pin.	–	–
67	$\overline{WDOUT}$	Output pin for detecting overrunning. Goes low when a watchdog timer operates or stack overflows.	CMOS push-pull	High-level output
68 69	XT_{IN} XT_{OUT}	Connect a 32 kHz crystal oscillator for subclock oscillation.	–	(Oscillation)
71	V_{LCD0}	Output pin for adjusting LCD drive reference voltage	–	–
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	Reference voltage output pins for LCD drive • V_{VCD0}: Reference voltage output • V_{LCD1}: Doubler output (double voltage) • V_{LCD2}: Tripler output (triple voltage)	–	–
74 75	CAPH CAPL	Connect a capacitor across these pins to raise the LCD drive voltage.	–	–

1.2 PROM PROGRAMMING MODE

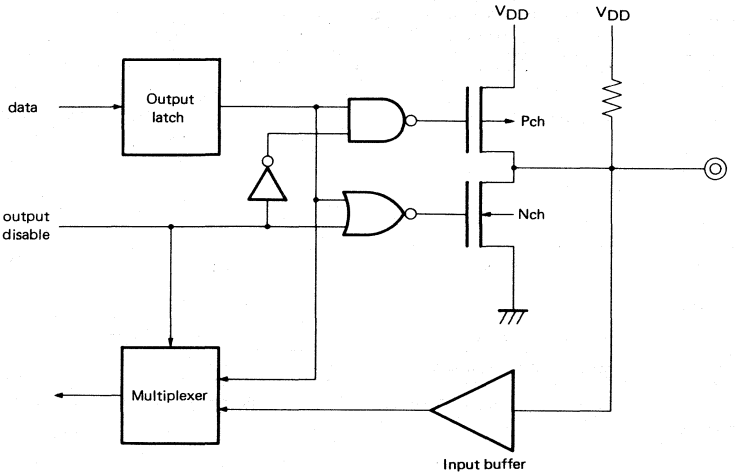
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
33	GND	Ground	–	–
35	VDD	Positive power supply.	–	–
40	GNDADC	A/D converter ground. Make GND_{ADC} equal to GND and do PROM programming.	–	–
41	VPP	Positive power supply for PROM programming. Applies 12.5 V program voltage.	–	–
42 – 45 50 – 53	D0 – D3 D4 – D7	8-bit data input/output pins	CMOS push-pull	Input
46 – 49	MD0 – MD3	Select PROM programming operation mode.	–	Input
62	VDD	Positive power supply	–	–
63	CLK	Inputs the address update clock.	–	Input

Note: The pins other than above cannot be used in PROM programming modes. For processing of the unused pins, see **(2) PROM Programming Mode.**

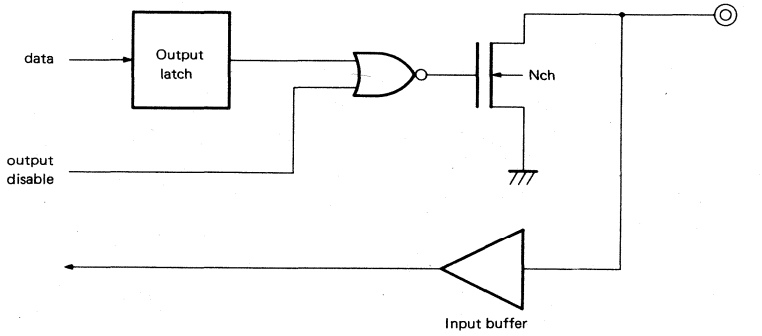
1.3 PIN EQUIVALENT CIRCUITS

The simplified I/O circuits schematic views for μPD17P207 pins are presented below.

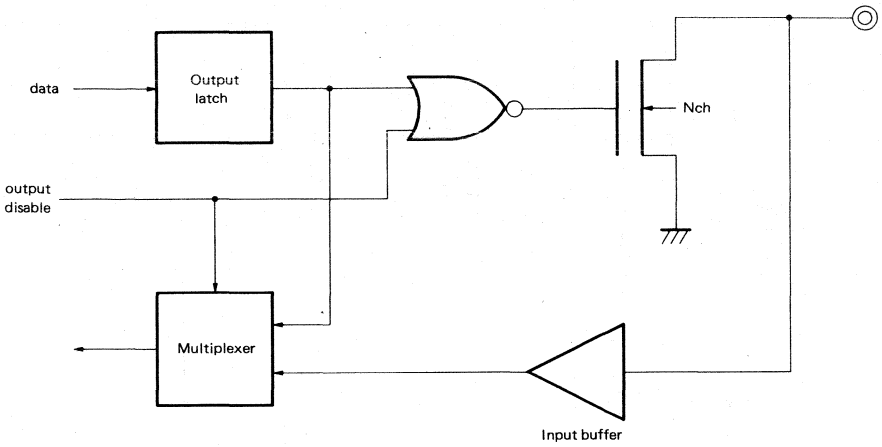
(1) $P0A_0$ to $P0A_3$



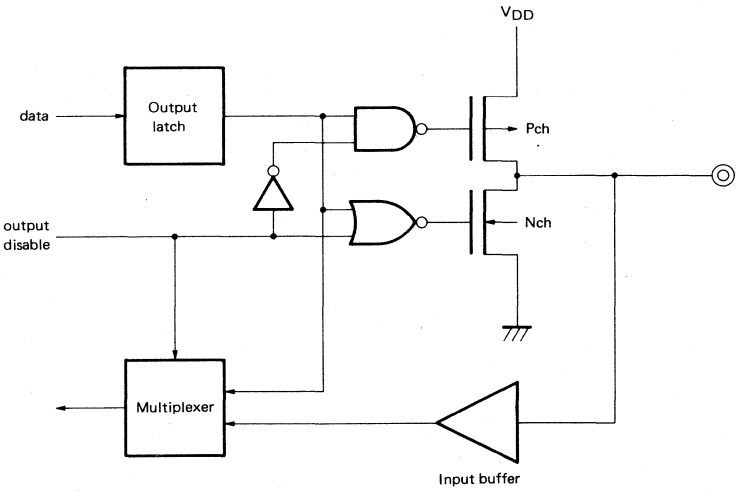
(2) $P0B_0$ to $P0B_3$



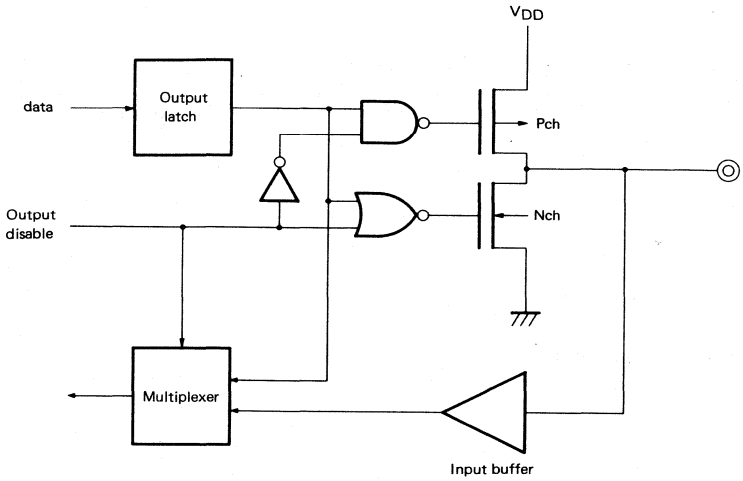
(3) $P0C_0$ to $P0C_3$



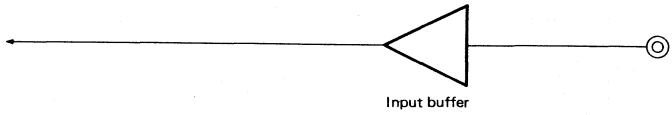
(4) $P0D_0$ to $P0D_3$



(5) $P1A_0$ to $P1A_2$



(6) $\overline{\text{RESET}}$



2. ONE-TIME PROM (PROGRAM MEMORY) WRITING, READING, AND VERIFICATION

Set PROM mode when writing, reading, or verifying PROM. Table 2-1 lists the pins to be used for PROM writing, reading or verification.

In PROM mode, no address input pin is used. Instead, the address is updated by the clock for input from the CLK pin.

Table 2-1 Pins to be Used for PROM Writing, Reading, or Verification

Pin name	Function
V_{PP}	Applies 12.5 V program voltage.
CLK	Inputs address update clock.
MD_0-MD_3	Selects operation mode.
D_0-D_7	Input and output 8-bit data.
V_{DD}	Applies 6 V supply voltage.

2.1 OPERATION MODE FOR WRITING, READING, AND VERIFICATION OF PROGRAM MEMORY

If +6 V is applied to the V_{DD} and +12.5 V to the V_{PP} pin after μPD17P207 has been placed in the reset status for a fixed time, μPD17P207 enters program memory write, read, or verify mode. μPD17P207 is reset when V_{DD} is 5 V and $\overline{RESET}$ goes low.

The MD0 to MD3 pins are used to set the operation modes listed in Table 2-2.

Leave the pins not used for program memory writing, reading, or verification open or ground them through pull-down resistors (470 Ω). (See **(2) PROM Programming Mode.**)

Table 2-2 Operation Modes for Program Memory Write, Read, and Verify

Operation mode selection						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read, verify mode
		H	x	H	H	Program inhibit mode

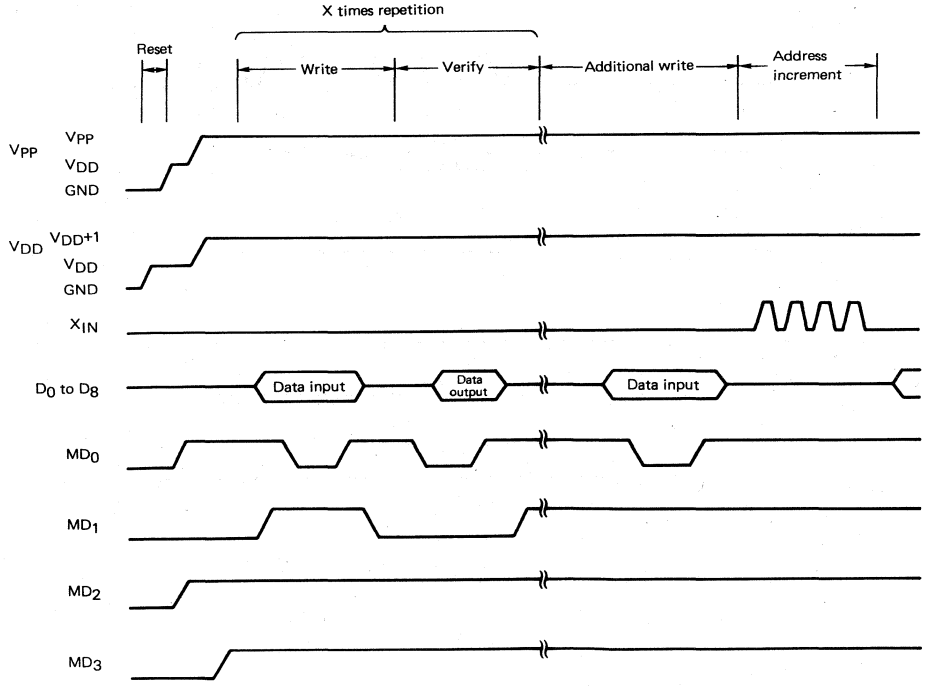
Remarks: x: L or H

2.2 PROGRAM MEMORY WRITING PROCEDURE

Write the program memory by following these steps. The program memory can be written at high speeds.

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (10), if the memory has been written. If it has not been written, repeat (7) through (9).
(10) Additional writing for (the number of times (7) through (9) are repeated: X) x 1 ms
(11) Program inhibit mode
(12) Input a pulse four times to pin CLK, in order to increment the program memory address (by one).
(13) Repeat (7) through (12), until the last address is programmed.
(14) Program memory address 0 clear mode
(15) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(16) Turn power off.

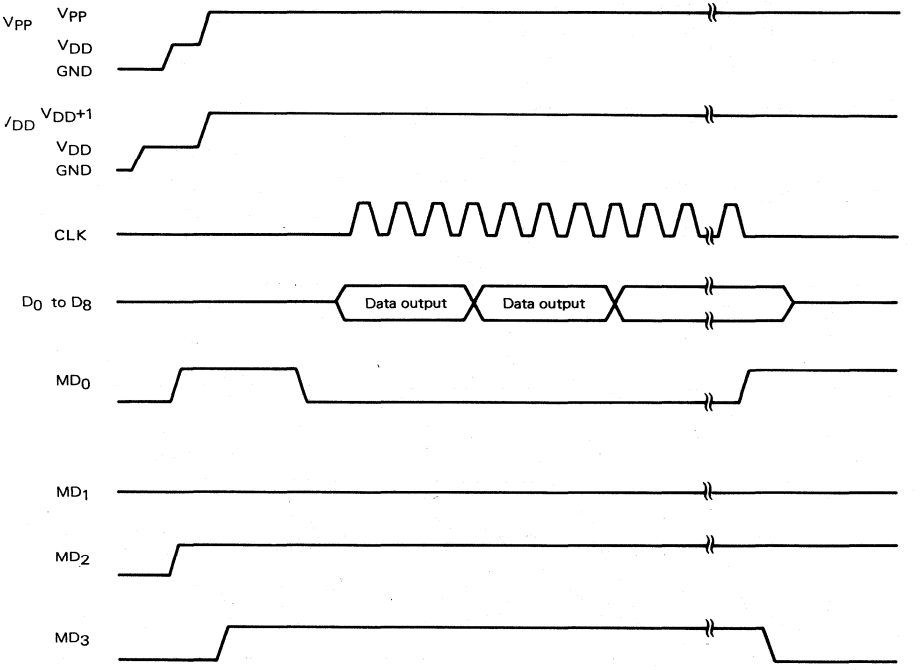
The following figure illustrates steps (2) through (12) above.



2.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Verify mode. The data for each address is output on a one-by-one basis in a cycle during which the clock pulse is input to pin CLK four times.
(8) Program inhibit mode
(9) Program memory address 0 clear mode
(10) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(11) Turn power off.

The following figure illustrates steps (2) through (9) above.



3. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}			−0.3 to +7.0	V
Analog Supply Voltage	AV_{DD}			−0.3 to +7.0	V
Input Voltage	V_I			−0.3 to V_{DD} +0.3	V
Output Voltage	V_O			−0.3 to V_{DD} +0.3	V
High-Level Output Current		REM pin	Peak value	−30	mA
			rms value	−20	mA
		1 pin	Peak value	−7.5	mA
		(excluding REM)	rms value	−5	mA
		All pins	Peak value	−22.5	mA
		(excluding REM)	rms value	−15	mA
High-Level Output Current		1 pin	Peak value	7.5	mA
			rms value	5	mA
		All pins	Peak value	22.5	mA
		(excluding REM)	rms value	15	mA
Operating Temperature	T_{opt}			−20 to +75	°C
Storage Temperature	Tstg			−40 to +125	°C

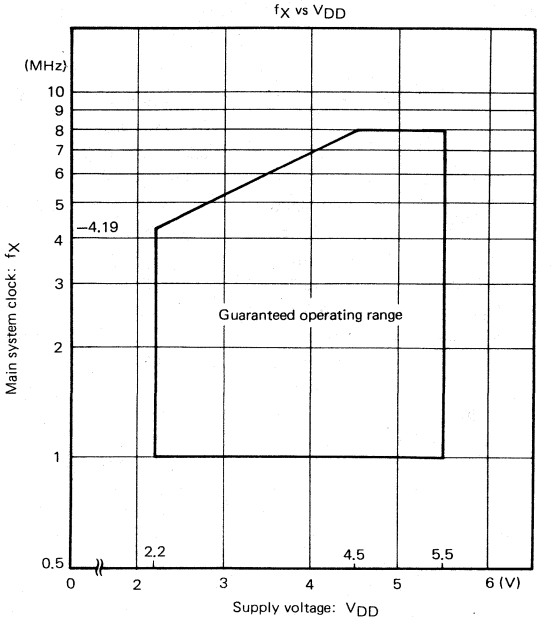
Note: Calculate rms as follows: rms = Peak value x $\sqrt{\text{duty}}$

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	INT, SI, $\overline{\text{RESET}}$ pins

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.4	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+60°C
	V_{DD2}	2.5	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+75°C
	V_{DD3}	4.5	5.0	5.5	V	System clock: f_X = 8 MHz, Ta = -20...+75°C
	V_{DD4}	2.0	3.0	5.5	V	System clock: f_X = 32 kHz, Ta = -20...+75°C
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	


fX vs VDD
(MHz)
10
9
8
7
6
5
4
3
2
1
0.5
Main system clock: fX
4.19
Guaranteed operating range
2.2
4.5
5.5
0
2
3
4
5
6 (V)
Supply voltage: VDD

RECOMMENDED RESONATORS

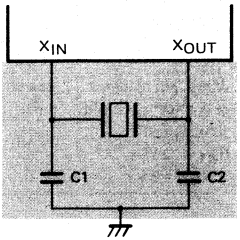
MAIN SYSTEM CLOCK: CERAMIC RESONATOR

Manufacturer	Product name	External capacitance (pF)		Oscillation voltage range (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	unnecessary	unnecessary	2.0	6.0	C-contained type
	CST4.00MGW	unnecessary	unnecessary	2.0	6.0	
	CST4.19MGW	unnecessary	unnecessary	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.00MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

Manufacturer	Frequency (MHz)	Retainer	External capacitance (pF)		Oscillation voltage range (V)		Remarks
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

Oscillator circuit



Note: Keep the oscillator circuit as close to the X_{IN} and X_{OUT} pins as possible. Do not route other signal lines through the shaded portion in the figure.

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARATERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Voltage 1 for detecting Low Voltage	V_{DET1}	1.6	2.0	2.8	V		
Voltage 2 for Detecting High Voltage	V_{DET2}	1.9	2.3	3.4	V		
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$ and INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{RESET}$ and INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{RESET}$ and INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{RESET}$ and INT pins	
High-Level Input Leakage Current	I_{LIH1}			20	μA	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIH2}			3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
Low-Level Input Leakage Current	I_{LIL1}			−20	μA	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIL2}			−3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
High-Level Output Current	I_{OH1}	−7	−15		mA	REM pin	$V_{OH} = V_{DD}-1.2$ V
	I_{OH2}	−0.3	−0.7		mA	*1	$V_{OH} = V_{DD}-0.3$ V
Low-Level Output Current	I_{OL}	0.5	0.9		mA	*2	V_{OL} = 0.3 V
Internal Pull-Up Resistor	R_{POA}	100	200	350	kΩ	$P0A_0$-$P0A_3$ pins	
	R_{RES}	24	47	94	kΩ	$\overline{RESET}$ pin	
A/D Absolute Accuracy				±2	LSB		
A/D Resolution			8		BITS		
A/D Converter Current Dissipation	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comparator mode	
Supply Current	I_{DD1}		0.8	3.5	mA	With X mounted (f_X = 4.19 MHz) and XT not mounted V_{DD} = 3 V	Operation mode
	I_{DD2}		0.23	1.0	mA		HALT mode
	I_{DD3}		2.0	10.0	μA		STOP mode
	I_{DD4}		7.0	25	μA	With X not mounted or in STOP mode and XT mounted (f_{XT} = 32 kHz) V_{DD} = 3 V	Operation mode
	I_{DD5}		3.0	15	μA		HALT mode

*1 $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$ pins

*2 $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P1A_0$-$P1A_2$, REM pins

LCD CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 3.6 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V	External variable resistance (0 to 2.2 MΩ)
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 to C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 to C4 = 0.47 μF
LCD Common Output Current	I_{COM}	30			μA	
LCD Segment Output Current	I_{LCD}	5			μA	

DC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ±10 %)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
VR Output Voltage	V_{REG}	1.42	1.9	2.4	V		
Voltage 1 for Detecting Low Voltage	V_{DET1}	1.6	2.0	2.8	V		
Voltage 2 for Detecting High Voltage	V_{DET2}	1.9	2.3	3.4	V		
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$ and INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Oter than $\overline{RESET}$ and INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{RESET}$ and INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than RESET and INT pins	
High-Level Input Leakage Current	I_{LIH1}			20	μA	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIH2}			3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
Low-Level Input Leakage Current	I_{LIL1}			−20	μA	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
	I_{LIL2}			−3	μA	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins	
High-Level Output Current	I_{OH1}	−7	−15		mA	REM pin	$V_{OH} = V_{DD}-0.6$ V
	I_{OH2}	−0.8	−1.2		mA	*1	$V_{OH} = V_{DD}-0.3$ V
Low-Level Output Current	I_{OL}	1.0	1.5		mA	*2	V_{OL} = 0.3 V
Internal Pull-Up Resistor	R_{POA}	140	200	350	kΩ	$P0A_0$-$P0A_3$ pins	
	R_{RES}	27	47	94	kΩ	$\overline{RESET}$ pin	
A/D Absolute Accuracy				±2	LSB		
A/D Resolution			8		BITS		
A/D Converter Current	I_{REF}		60	120	μA		
Comparator Error			10	20	mV	In comparator mode	
Supply Current	I_{DD1}		1.8	5.0	mA	With X mounted (f_X = 4.19 MHz) and XT not mounted V_{DD} = 3 V	Operation mode
	I_{DD2}		0.6	2.0	mA		HALT mode
	I_{DD3}		2.6	20.0	μA		STOP mode
	I_{DD4}		10.5	40	μA	With X not mounted or in STOP mode and with XT mounted (f_{XT} = 32 kHz) V_{DD} = 5 V	Operating mode
	I_{DD5}		6.0	20	μA		HALT mode

*1 $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$ pins

*2 $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P0A_0$-$P0A_3$, $P1A_0$-$P1A_2$, REM pins

LCD CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ±10 %)

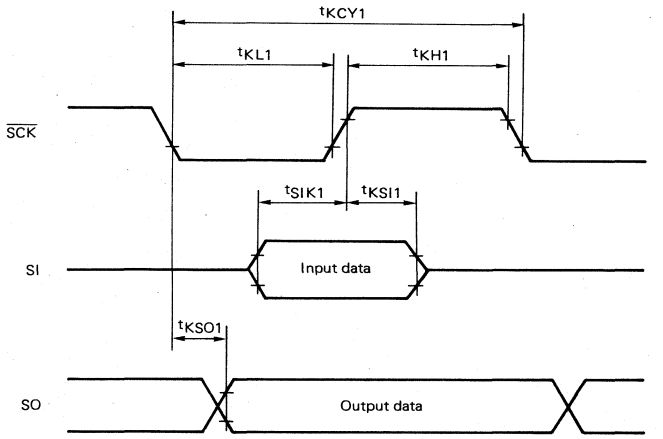
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V	External variable resistance (0 to 2.2 MΩ)
Doubler Output Voltage	V_{LCD1}	1.9	2.0		V_{LCD0}	C1 to C4 = 0.47 μF
Tripler Output Voltage	V_{LCD3}	2.85	3.0		V_{LCD0}	C1 to C4 = 0.47 μF
LCD Common Output Current	I_{COM}	30			μA	
LCD Segment Output Current	I_{LCD}	5			μA	

AC CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
$\overline{SCK}$ Input Cycle Time	t_{KCY}	2.0			μs	V_{DD} = 5 V ± 10 %	Data input
		10.0			μs		Data output
		5.0			μs		Data input
		13.0			μs		Data output
$\overline{SCK}$ Input High-1 Low-Level Width	t_{KH}, t_{KL}	1.0			μs	V_{DD} = 5 V ± 10 %	Data input
		5.0			μs		Data output
		2.5			μs		Data input
		6.5			μs		Data output
SI Setup Time (vs. $\overline{SCK}$ ↑)	t_{SIK}	100			ns		
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KS}	100			ns		
$\overline{SCK}$ ↓ → SO Output Delay Time	t_{KSO}			4.5	μs	C_L = 100 pF	
INT High-Level Width	t_{IOH}			50	μs		
$\overline{RESET}$ Low-Level Width	t_{RSL}			50	μs		

SERIAL TRANSFER TIMING

3-line serial I/O mode:



DC PROGRAMMING CHARACTERISTICS (T_a=25 °C, V_{DD}=6.0±0.25 V, V_{PP}=12.5±0.3 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}-1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Keep V_{PP} to below +13.5 V, including the overshoot.

2: Apply V_{DD} before V_{PP}, and remove V_{DD} after V_{PP}.

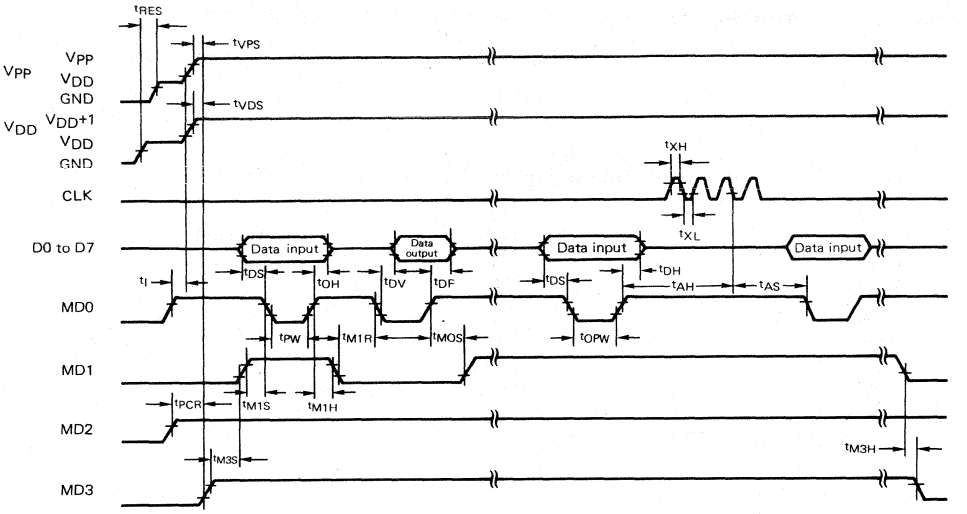
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP}=12.5±0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑→ Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	μs	
V_{PP} Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↓)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High-Low-Level Width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓→ Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

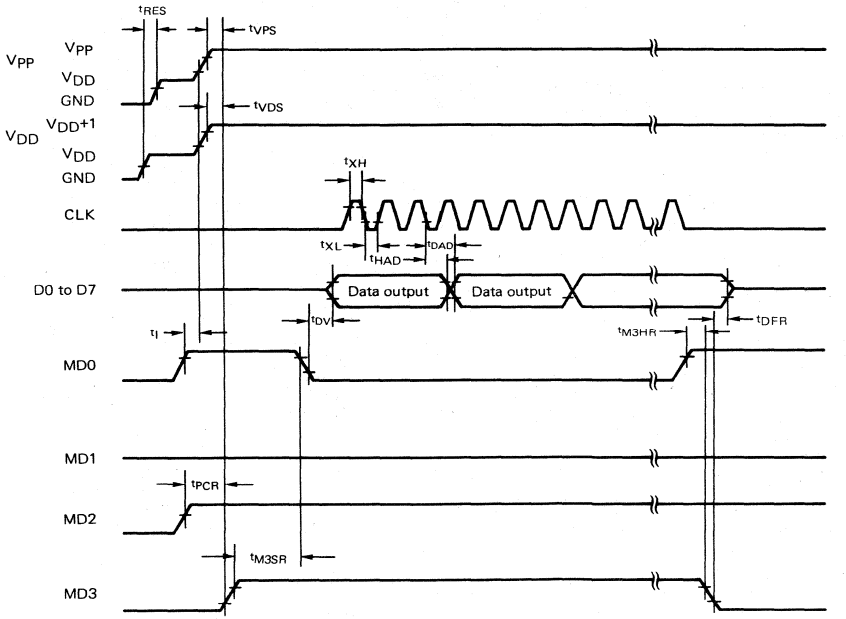
*1: Symbols for corresponding μPD27C256

*2: The internal address signal is incremented by one at the falling edge of the third CLK input and is not connected to a pin.

PROGRAM MEMORY WRITE TIMING

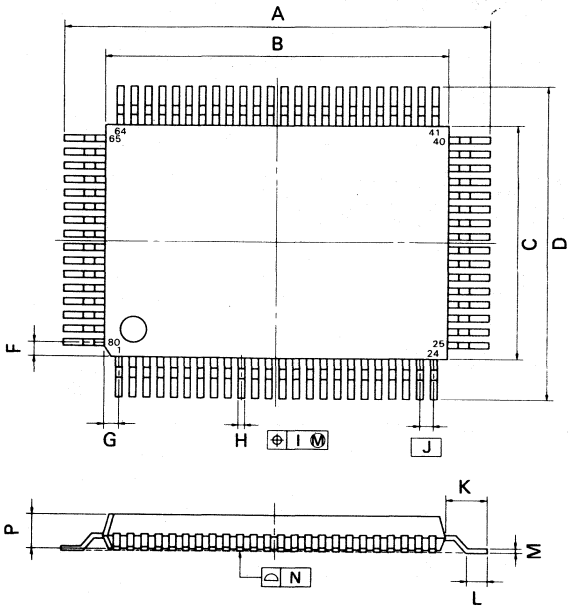


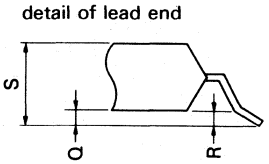
PROGRAM MEMORY READ TIMING



4. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×20)





S80GF-80-3B9

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{+0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{+0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	0.8	0.031
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

4-BIT SINGLE-CHIP MICROCONTROLLER WITH LCD CONTROLLER/DRIVER FOR INFRARED REMOTE CONTROLLER

μPD17202A is a 4-bit single-chip microcontroller containing an LCD controller/driver and an infrared remote controller carrier generator circuit.

This microcontroller employs the 17K architecture and can execute transfer and arithmetic operations with a single 16-bit instruction between data memory addresses and between the data memory and a peripheral circuit.

μPD17202A is housed in a 64-pin plastic QFP.

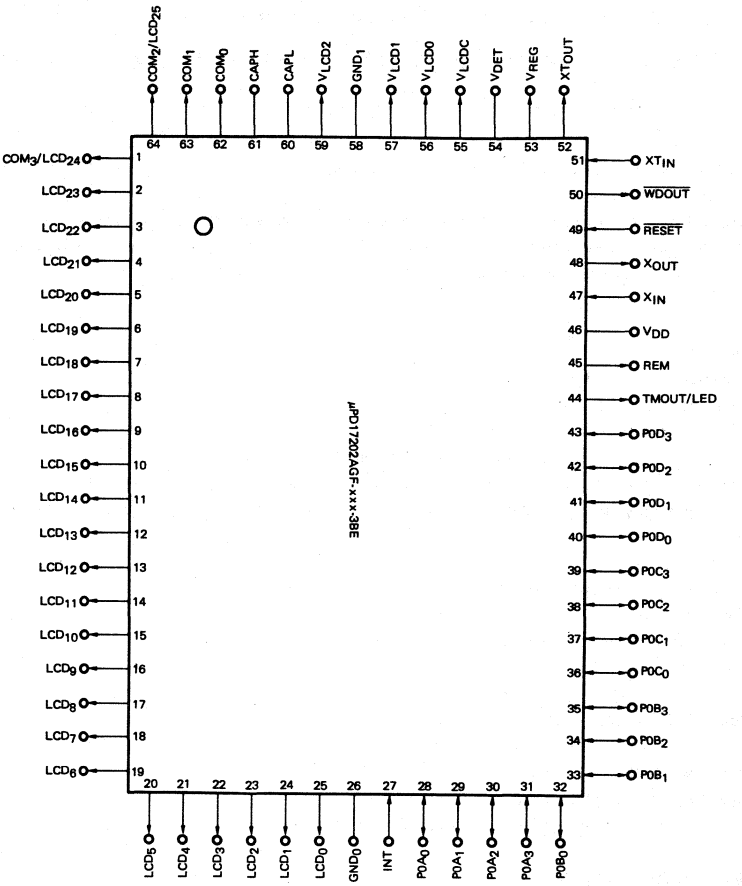
FEATURES

- 17K architecture
- Program memory (ROM): 2048 x 16 bits
- Data memory (RAM): 112 x 4 bits
- Internal infrared remote controller carrier generator
- Internal LCD controller/driver (can display up to 96 segments)
  Common pins: 4, segment pins: 24 (two of the common pins can also be used as segment pins), internal LCD constant voltage supply circuit: LCD drive voltage can be arbitrarily set at 2.4 to 5.4 V by external resistor
- I/O ports: 16
- External interrupt pin: 1
- Stack levels: 5 (two interrupt levels)
- 8-bit timer: 1 channel
- Watch timer: 1 channel (used as watchdog timer or watch timer)
- Standby function: STOP and HALT
  (to reduce current dissipation)
- Instruction execution time: 4 μs
  (with 4 MHz ceramic oscillator)
- Operation clock: 4 MHz or 32 kHz
- Operating voltage range: 2.2 to 5.5 V (with main clock)
  2.0 to 5.5 V (with subclock)

ORDERING INFORMATION

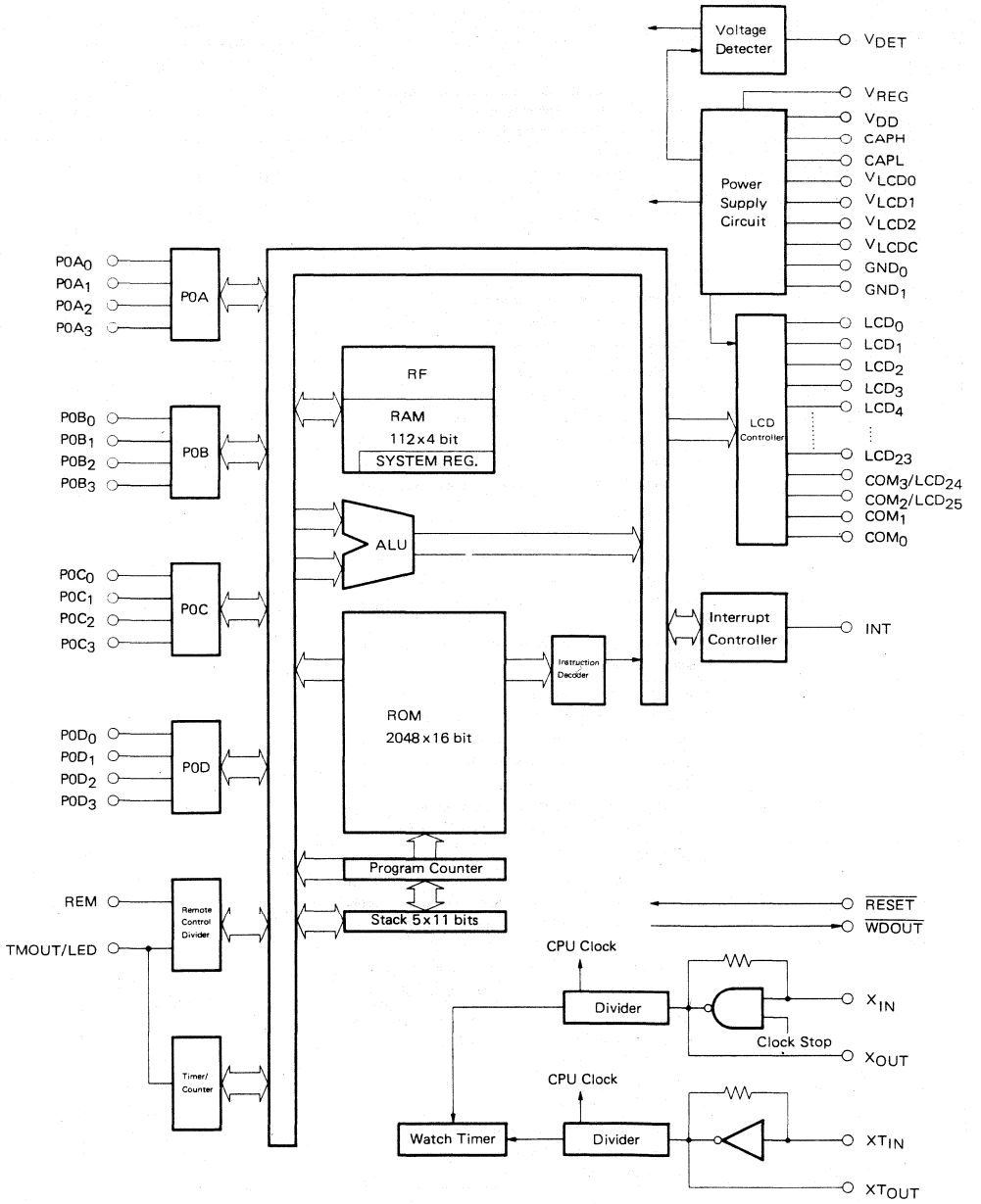
Order Code	Package	Quality Grade
μPD17202AGF-xxx-3BE	64-pin plastic QFP	Standard

PIN CONFIGURATION (Top View)



CAPH, CAPL	: Booster capacitor connection pins
COM_0-COM_3	: LCD common signal output
GND_0-GND_1	: Ground
INT	: External interrupt request signal input
LCD_0-LCK_{25}	: LCD segment signal output
LED	: Remote control transmission indication output
POA_0-POA_3	: Port 0A
POB_0-POB_3	: Port 0B
POC_0-POC_3	: Port 0C
POD_0-POD_3	: Port 0D
REM	: Remote control transmission output
$\overline{RESET}$	: Reset input
TMOUT	: 8-bit timer output
V_{DD}	: Power supply pin
V_{DET}	: Voltage detector detection voltage adjustment
V_{LCDC}	: LCD drive reference voltage adjustment
V_{LCD0}-V_{LCD2}	: LCD drive voltage outputs
V_{REG}	: Voltage regulator output
$\overline{WDOUT}$	: Overhang detecting output
X_{IN}, X_{OUT}	: Main clock oscillator circuit
XT_{IN}, XT_{OUT}	: Subclock oscillator circuit

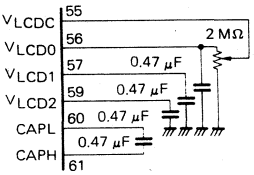
BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN IDENTIFICATION

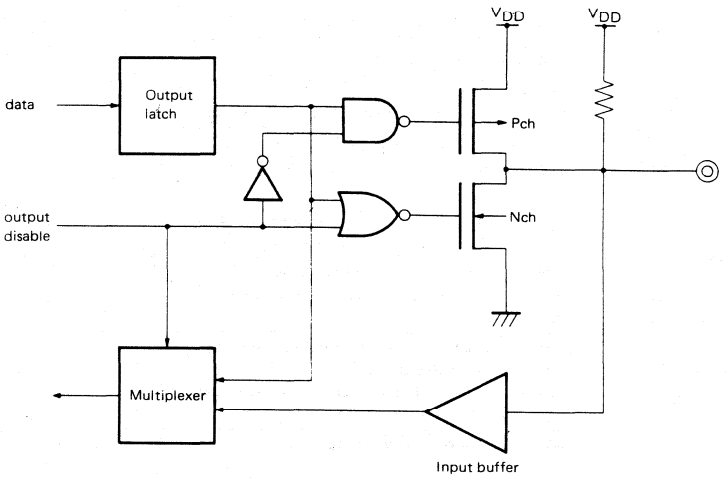
PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
62 63 64 1 2 | 25	COM_0 COM_1 LCD_{25}/COM_2 LCD_{24}/COM_3 LCD_{23} | LCD_0	LCD controller/driver segment signal outputs and LCD controller/driver common signal outputs. • LCD_{25} to LCD_0 LCD controller/driver segment signal outputs • COM_0 to COM_3 LCD controller/driver common signal outputs	CMOS	–
26	GND_0	GND	–	–
27	INT	Inputs external interrupt request signal. Either the rising edge or the falling edge can be specified as the interrupt request effective edge.	–	Input
28 | 31	$P0A_0$ | $P0A_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs with pull-up resistors, and can be used as key return inputs for key matrix. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
32 | 35	$P0B_0$ | $P0B_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs with pull-up resistors, and can be used as key return inputs for key matrix. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
36 | 39	$P0C_0$ | $P0C_3$	4-bit CMOS input/output port. This port can be specified for input/outputs in 4-bit units. In the output mode, these pins become N-ch open-drain outputs, and can be used for key source outputs for key matrix. This port does not enter the standby mode while at least one pin of this port outputs the high-level signal.	N-ch open-drain	Input
40 | 43	$P0D_0$ | $P0D_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain outputs, and can be used for key source outputs for key matrix. This port does not enter the standby mode while at least one pin of this port outputs the high-level signal.	N-ch open-drain	Input
44	TMOUT/LED	This pin outputs NRZ signal (LED), synchronized with infrared remote control signal, and 8-bit timer (TMOUT). • TMOUT · 8-bit timer output • LED · Remote control transmission indication output Goes low when the remote control carrier is output while the NRZ signal (LED) is selected.	CMOS push-pull	High-level output

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
45	REM	Infrared remote control signal output.	CMOS push-pull	**Low-level output**
46	V_{DD}	Positive voltage power supply pin. 2.2 to 5.5 V is applied.	–	–
47 48	X_{IN} X_{OUT}	Main clock oscillation circuit is connected across these pins. Connect a 4 MHz ceramic resonator or crystal resonator across these pins.	–	–
49	$\overline{RESET}$	Reset signal input. Main clock oscillation is stopped during low-level input.	–	Input
50	$\overline{WDOUT}$	Output for detection of a program overhang. This signal goes low when a watchdog timer and a stack overflows are generated.	N-ch open-drain	–
51 52	XT_{IN} XT_{OUT}	Subclock oscillation circuit is connected across these pins. Connect a 32 kHz crystal resonator across these pins.	–	–
53	V_{REG}	Voltage regulator output for subclock generator. An external 0.1 μF capacitor must be connected to this pin.	–	–
54	V_{DET}	A resistor for adjusting the voltage detector detection level is connected to this pin. To adjust the voltage level, a several MΩ variable resistor is connected between this pin and GND.	–	–
55	V_{LCDC}	Adjusts LCD drive reference voltage. **Example:**  		
56 57	V_{LCD0} V_{LCD1}	Outputs a voltage boosted from LCD drive reference voltage. V_{LCD0} voltage becomes the reference voltage. 0.47 μF capacitance should be built up between V_{LCD1} and GND.	–	–
58	GND_1	GND	–	–
59	V_{LCD2}	Outputs a voltage boosted from LCD drive reference voltage. 0.47 μF capacitance should be built up between this pin and GND.	–	–
60 61	CAPL CAPH	Voltage boosting capacitor is connected across these pins. 0.47 μF capacitance should be built up between CAPH and CAPL.		

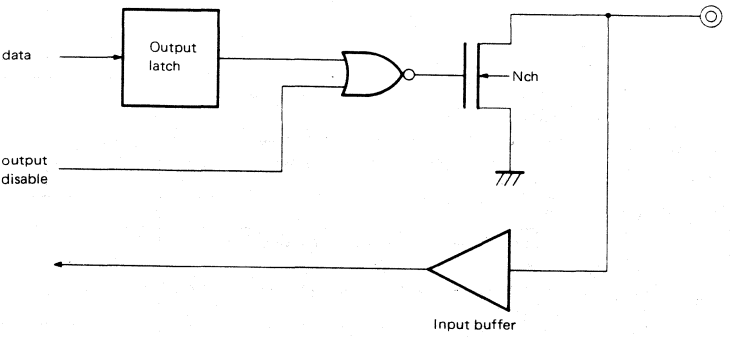
1.2 INPUT/OUTPUT CIRCUITS

The input/output circuit for each μPD17202A's pin is shown below.

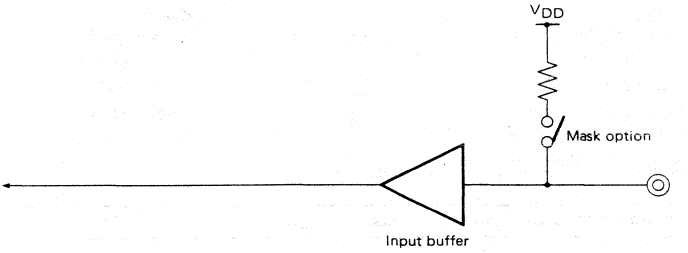
(1) $P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$



(2) $P0C_0$-$P0C_3$, $P0D_0$-$P0D_3$



(3) $\overline{\text{RESET}}$



22. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

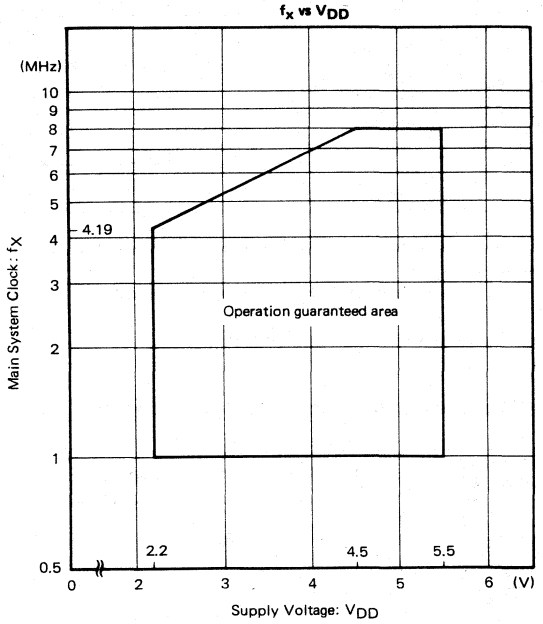
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

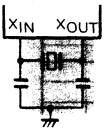
CAHRACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	INT, $\overline{\text{RESET}}$ pins
	C_{PIN}			10	PF	Other than INT, $\overline{\text{RESET}}$ pins

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz
	V_{DD2}	4.5	5.0	5.5	V	System clock: f_X = 8 MHz
	V_{DD3}	2.0	3.0	5.5	V	System clock: f_{XT} = 32 kHz
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = –20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

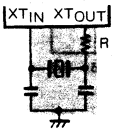
RESONATOR	RECOMMENDED CONSTANTS	ITEM	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Ceramic oscillator **Note 3**		Oscillation frequency (f_X) **Note 1**	1.0	4.0	8.0	MHz	
		Oscillation stabilization time **Note 2**			4	ms	From when V_{DD} reaches the minimum oscillation voltage
Crystal oscillator **Note 3**		Oscillation frequency (f_X) **Note 1**	1.0	4.0	8.0	MHz	
		Oscillation stabilization time **Note 2**			10	ms	V_{DD} = 4.5 to 6.0 V
					30	ms	

Note 1 The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2 The oscillation stabilization time is the time required for stabilizing the oscillation after V_{DD} is applied or the STOP mode is released.

3 The recommended oscillators are shown in the table described later.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = –20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

RESONATOR	RECOMMENDED CONSTANTS	ITEM	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Crystal oscillator		Oscillation frequency (f_{XT})		32.768		kHz	
		Oscillation stabilization time			10	s	

Note: When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the following notations must be read and observed for wiring within the shaded area in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line.**
- **Capacitors used in the oscillators must always be grounded to V_{SS} potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CAHRACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Low Voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V		
High-Level Input Voltage	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$, INT pins	
	V_{IH2}	0.7V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2V_{DD}	V	$\overline{\text{RESET}}$, INT pins	
	V_{IL2}	0		0.3V_{DD}	V	Other than $\overline{\text{RESET}}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT pin	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	$\overline{\text{RESET}}$ pin	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D pin	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT pin	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{\text{RESET}}$ pin	V_{IL} = 0 V w/o pull-up resistor
	I_{IL3}	30	60	120	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A, P0B pins	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	8	15	30	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			0.2	μA	P0C, P0D pins	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	-0.6	-2.0	-4.0	mA	P0A, P0B pins	$V_{OH} = V_{DD} - 0.3$ V
	I_{OH2}	-7.0	-15.0	-25.0	mA	REM pin	$V_{OH} = V_{DD} - 2.0$ V
	I_{OH3}	-0.3	-1.0	-2.0	mA	LED pin	$V_{OH} = V_{DD} - 0.3$ V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B pins	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D pins	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM pin	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED pin	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{\text{WDOUT}}$ pin	V_{OL} = 0.3 V
Supply Current	I_{DD1}	0.2	0.5	1.5	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}		0.5	1.5	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
LCD Output Voltage Adjustable Range	V_{LCD0}	0.6		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9V_{LCD0}	2V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85V_{LCD0}	3V_{LCD0}		V		
Common Output Current	I_{COM}	30			μA	V_{DS} = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	V_{DS} = 0.2 V	

RECOMMENDED OSCILLATORS

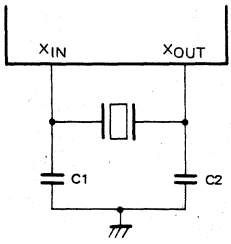
MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
		C1	C2	MIN.	MAX.	
Murata Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW			2.0	6.0	
	CST4.19MGW			2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

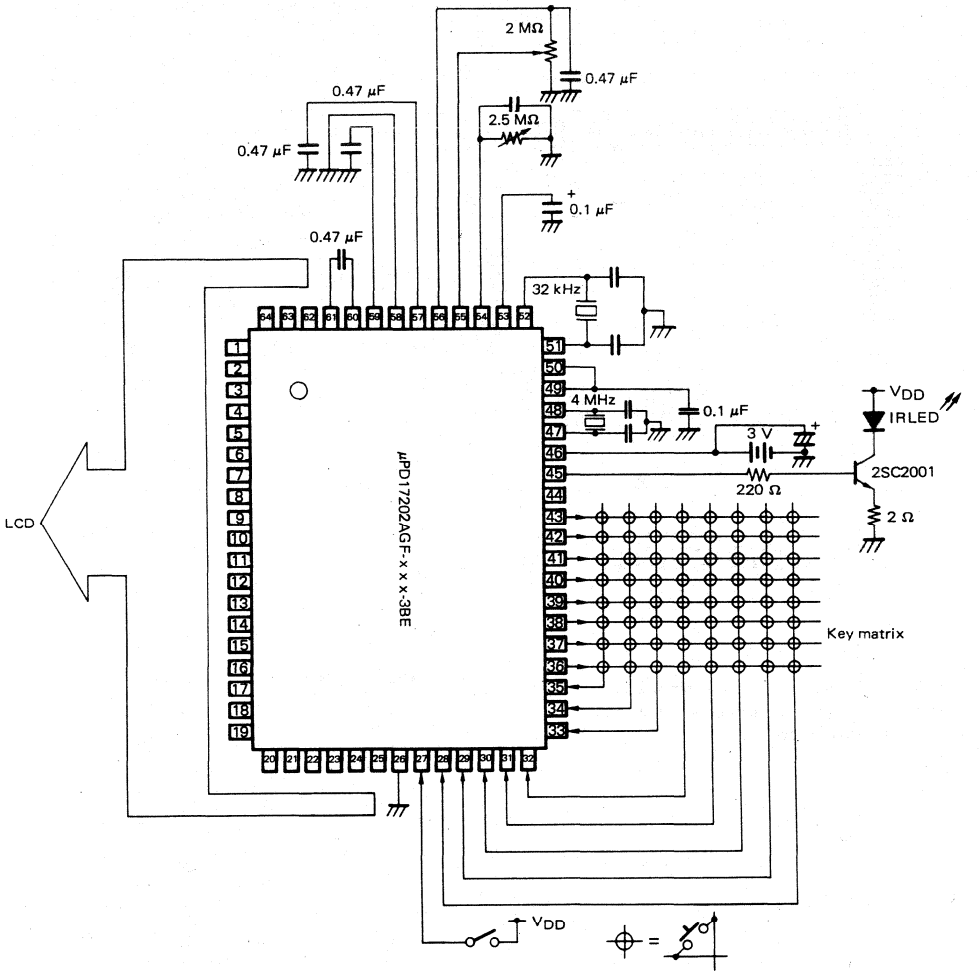
MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

MANUFACTURER	FREQUENCY (MHz)	RETAINER	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

Oscillator circuit



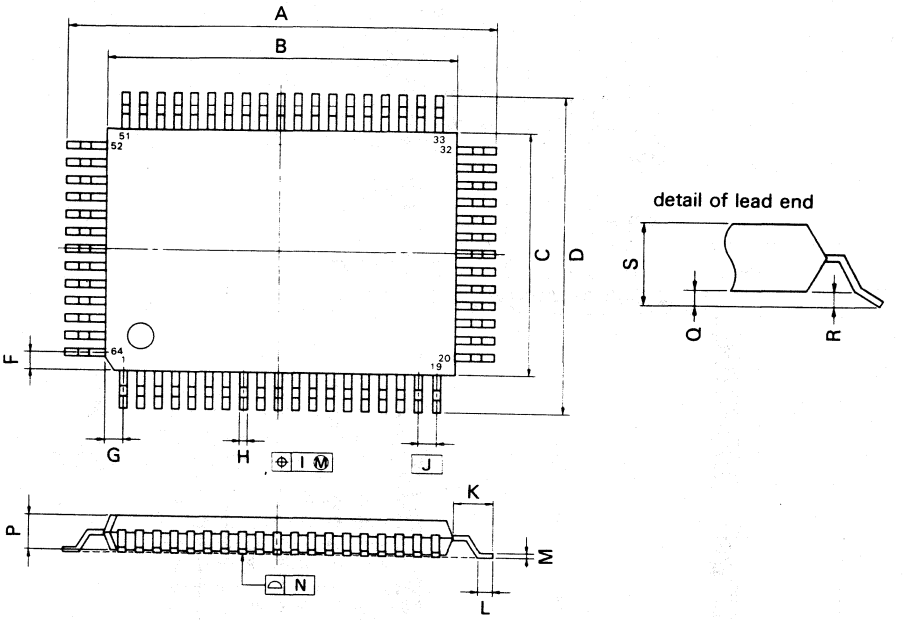
23. APPLICATION CIRCUIT EXAMPLE



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

24. PACKAGE DIMENSION

64 PIN PLASTIC QFP (14×20)



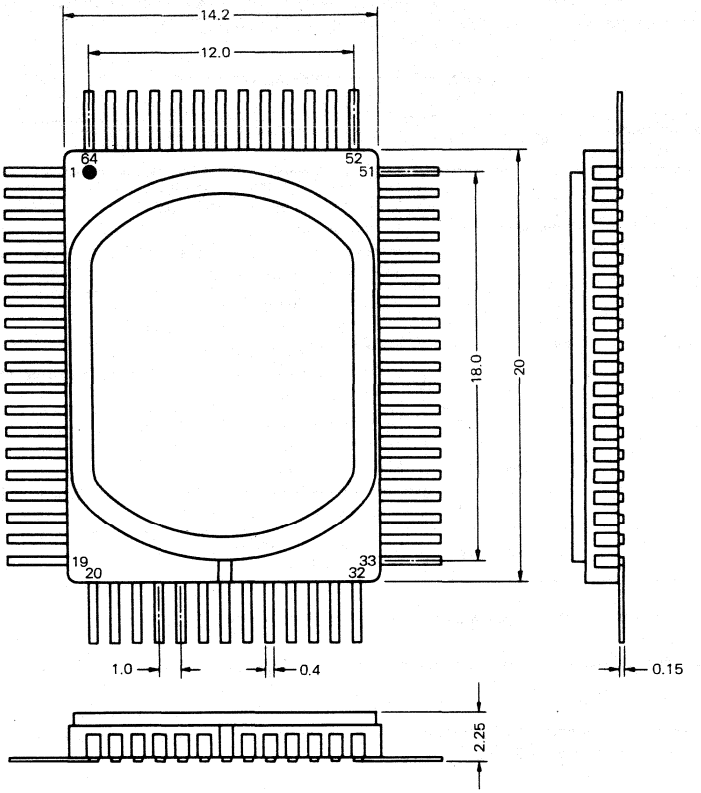
S64GF-100-3B8,3BE

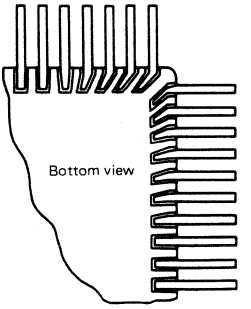
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{-0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{-0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{-0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

64-PIN CERAMIC QFP for ES (Reference) (Unit: mm)





Notes:

1. **The metal cap is connected to pin 26 and is at the ground level.**
2. **The bottom leads are diagonally molded.**
3. **The dimensions of the tip of the lead is not controlled, and therefore may vary.**

25. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD17202A by soldering, soldering should be performed under the following recommended conditions. For other soldering methods, please consult with NEC sales personnel.

Table 25-1 Soldering Conditions

Recommended conditions reference code	Soldering method	Soldering conditions
IR30-162	Infrared reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
VP15-162	VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
WS60-162	Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max., Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
–	Pin partial heating	Pin temperature: 300 °C max., Timer: 10 seconds max.

*: Number of days after unpacking the dry pack. Storage conditions are 25 °C and 65% RH max.

Note: Do not use different soldering methods together (however, pin partial heating can be performed with other soldering methods.)

Remarks: For details on recommended soldering conditions for surface mounting, refer to the information document "Surface Mount Technology Manual" (IEI-1207).

μPD17P202A is a model of μPD17202A which is equipped with a one-time PROM in place of the μPD17202A internal mask ROM.

Since the user can write the program to μPD17P202A, the microcomputer is suitable for experimental or small-scale production of μPD17202A systems.

It is recommended that you also read the documents related to μPD17202A, in addition to this data sheet.

2

FEATURES

- Compatible with μPD17202A
- Internal one-time PROM: 2,048 x 16 bits
- Operating voltage range: 2.2 to 5.5 V

ORDERING INFORMATION

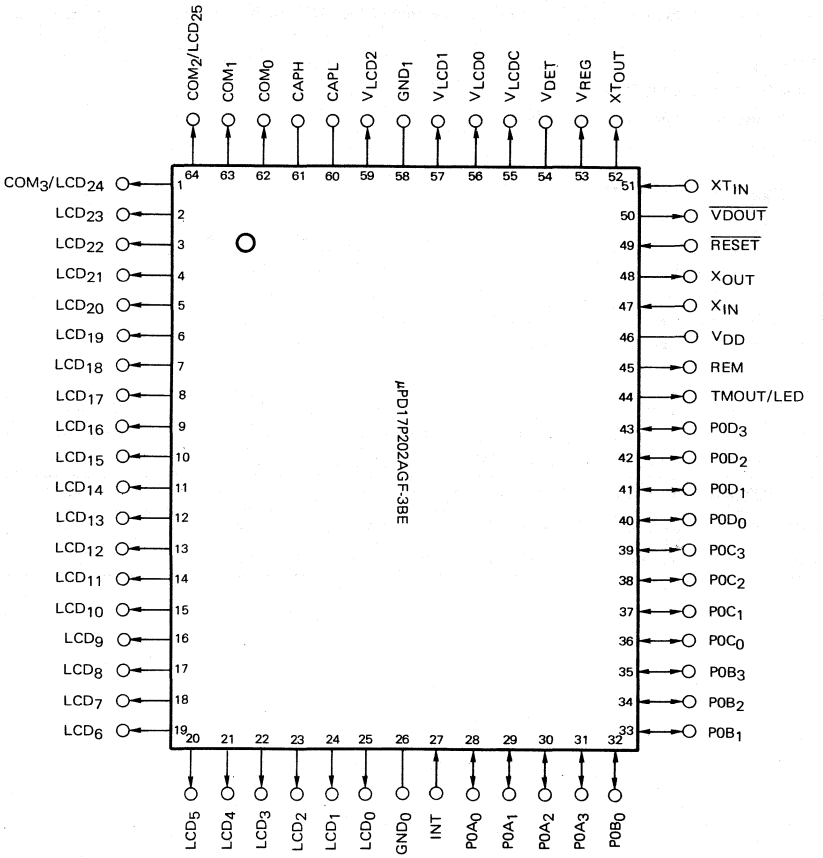
Order Code	Package	Quality Grade
μPD17P202AGF-001-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-002-3BE	64-pin plastic QFP (14 x 20 mm)	Standard
μPD17P202AGF-003-3BE	64-pin plastic QFP (14 x 20 mm)	Standard

Note: Table below indicates differences in these products:

Item / Part number	Pull-up resistor for $\overline{\text{RESET}}$ pin	Pull-up resistors for P0A, P0B pins	Main clock generator used/unused	Subclock generator used/unused
μPD17P202AGF-001-3BE	Provided	Provided	Used	Used
μPD17P202AGF-002-3BE	Not provided	Provided	Used	Unused
μPD17P202AGF-003-3BE	Not provided	Not provided	Unused	Used

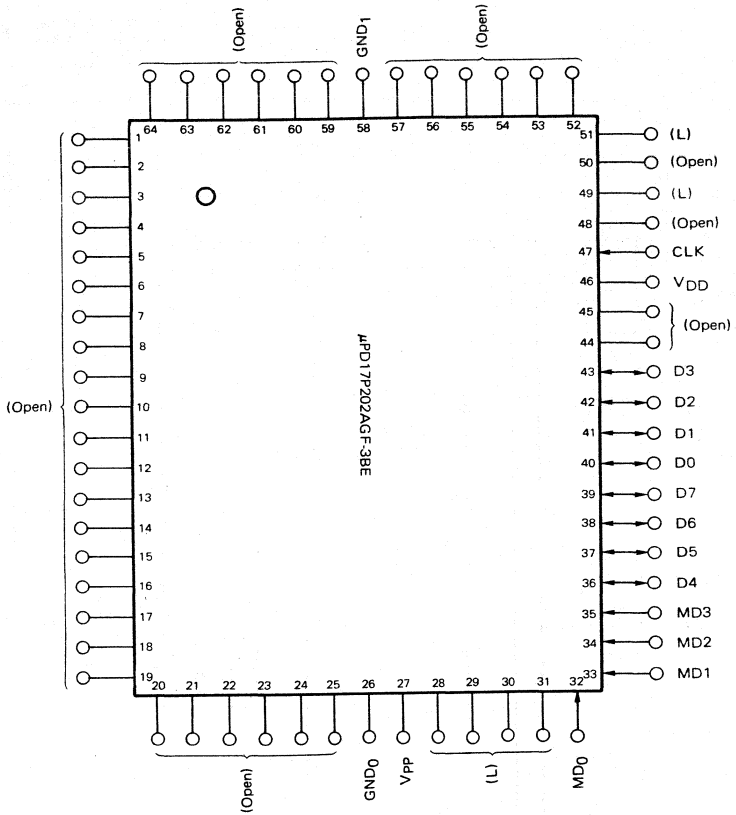
PIN CONFIGURATION (Top View)

(1) Ordinary operation



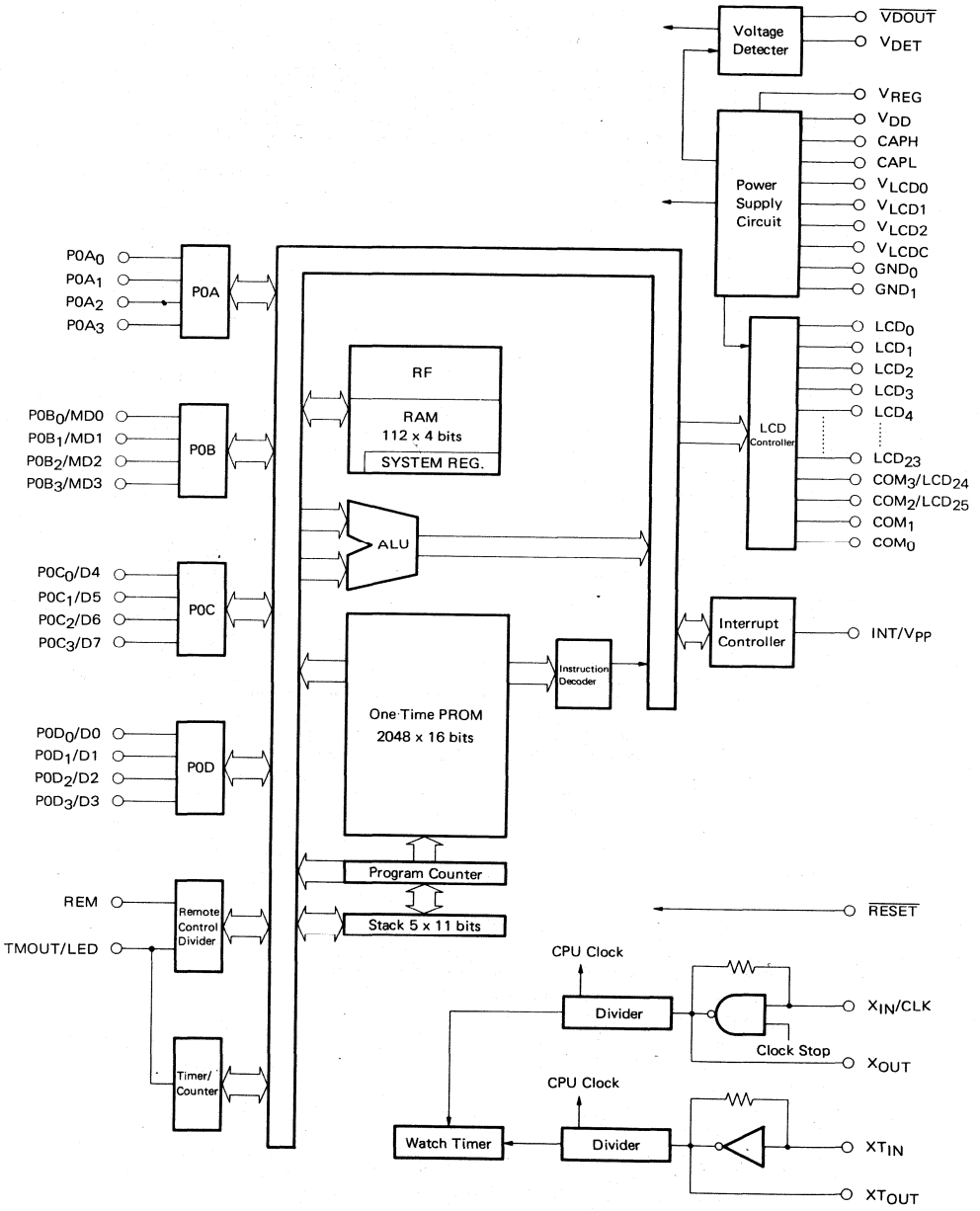
$P0A_0$-$P0A_3$	:	Input/output port
$P0B_0$-$P0B_3$	:	Input/output port
$P0C_0$-$P0C_3$	:	Input/output port
$P0D_0$-$P0D_3$	:	Input/output port
V_{REG}	:	Voltage regulator output
V_{DET}	:	Voltage detector detection voltage adjustment
V_{LCDC}	:	LCD drive reference voltage adjustment
V_{LCD0}-V_{LCD2}	:	LCD drive voltage outputs
LCD_0-LCE_{35}	:	LCD segment signal output
COM_0-COM_3	:	LCD common signal output
TMOUT	:	8-bit timer output
LED	:	Remote control transmission indication output
REM	:	Remote control transmission output
INT	:	External interrupt request signal input
$\overline{RESET}$	:	Reset input
$\overline{VDOUT}$	:	Low voltage detection circuit output
X_{IN}, X_{OUT}	:	Main clock oscillator circuit
XT_{IN}, XT_{OUT}	:	Subclock oscillator circuit
CAPH, CAPL	:	Booster capacitor connection pins
CLK	:	PROM clock input
MD0-MD3	:	PROM mode selection input
D0-D7	:	PROM data input/output
V_{PP}	:	PROM write voltage power supply pin
V_{DD}	:	Power supply pin
GND_0, GND_1	:	GND

(2) PROM programming mode



Note: ( ) indicates processing for pins not used in the PROM programming mode.
L : Ground each of these pins through a 470 Ω resistor.
Open : Do not connect these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 ORDINARY OPERATION MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
62 63 64 1 2 I 25	COM_0 COM_1 LCD_{25}/COM_2 LCD_{24}/COM_3 LCD_{23} I LCD_0	LCD controller/driver segment signal outputs and LCD controller/driver common signal outputs. ● LCD_{25} to LCD_0 ・ LCD controller/driver segment signal outputs ● COM_0 to COM_3 ・ LCD controller/driver common signal outputs	CMOS	–
26	GND_0	GND	–	–
27	INT	Inputs external interrupt request signal. Either the rising edge or the falling edge can be specified as the interrupt request effective edge.	–	Input
28 I 31	$P0A_0$ I $P0A_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note.**	CMOS push-pull	Input
32 I 35	$P0B_0$ I $P0B_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the input mode, these pins become CMOS inputs, and can be used as key return inputs for key matrix. See **Note.**	CMOS push-pull	Input
36 I 39	$P0C_0$ I $P0C_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
40 I 43	$P0D_0$ I $P0D_3$	4-bit CMOS input/output port. This port can be specified for input/output in 4-bit units. In the output mode, these pins become N-ch open-drain output, and can be used for key source output for key matrix.	N-ch open-drain	Input
44	TMOUT/LED	This pin outputs NRZ signal (LED) synchronized with infrared remote control signal and 8-bit timer (TMOUT). ● TMOUT ・ 8-bit timer output ● LED ・ Remote control transmission indication output	CMOS push-pull	High level output

Note: Pull-up resistors are provided only in the μPD17P202A-001 and μPD17P202A-002.

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
45	REM	Infrared remote control signal output.	CMOS push-pull	High level output
46	V_{DD}	Positive voltage power supply pin. 2.2 to 5.5 V is applied in the normal operation mode.	–	–
47 48	X_{IN} X_{OUT}	Main clock oscillation circuit is connected across these pins. Connect a 4 MHz ceramic resonator or crystal resonator across these pins.	–	–
49	$\overline{RESET}$	Reset signal input.	–	Input
50	$\overline{VDOUT}$	Internal low voltage detection circuit output.	CMOS push-pull	–
51 52	XT_{IN} XT_{OUT}	Subclock oscillation circuit is connected across these pins. Connect a 32 kHz crystal resonator across these pins.	–	–
53	V_{REG}	Voltage regulator output for subclock generator.	–	–
54	V_{DET}	A resistor for adjusting the voltage detector detection level is connected to this pin.	–	–
55	V_{LCDC}	Adjusts LCD drive reference voltage.	–	–
56 57	V_{LCD0} V_{LCD1}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
58	GND_1	GND	–	–
59	V_{LCD2}	Outputs a voltage boosted from LCD drive reference voltage.	–	–
60 61	CAPL CAPH	Voltage boosting capacitor is connected across these pins.	–	–

1.2 PROM PROGRAMMING MODE

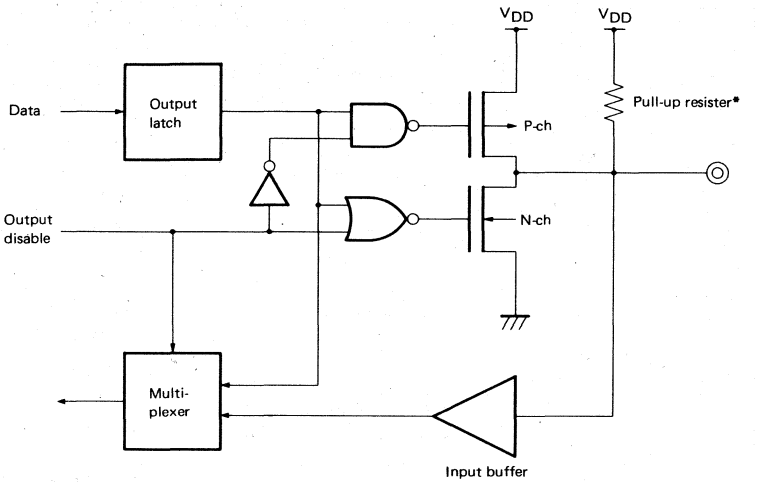
PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	POWER ON RESET
26	GND_0	GND	–	–
27	V_{PP}	Positive power supply pin for PROM programming. 12.5 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
32 I 35	MD3 I MD0	Operation mode selection inputs for PROM programming.	–	Input
36 I 39 40 I 43	D4 I D7 D0 I D3	8-bit data input/output for PROM programming.	CMOS push-pull	Input
46	V_{DD}	Positive power supply pin. 6 V is applied to this pin when programming, reading, or verifying the program memory.	–	–
47	CLK	Clock input for PROM programming.	–	–
48	GND_1	GND	–	–

Remarks: Pins other then listed above are not used in the PROM programming mode. Refer to **"Pin Connection Diagram (2) PROM Programming Mode"** for recommended conditions for unused pins.

1.3 PIN EQUIVALENT CIRCUITS

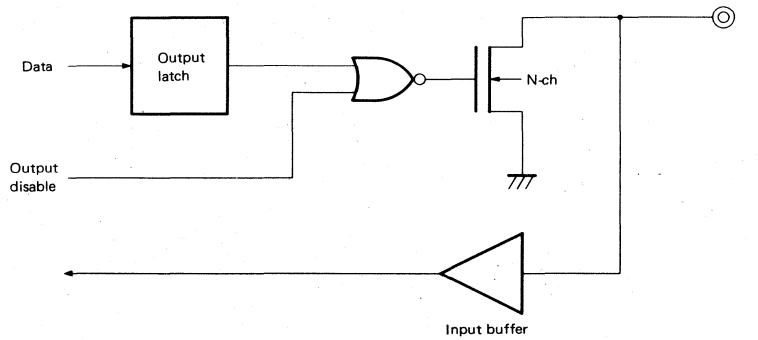
The simplified pin equivalent circuits schematic views for μPD17P202A's pins are presented below.

(1) $P0A_0$ through $P0A_3$, $P0B_0$/MD0 through $P0B_3$/MD3

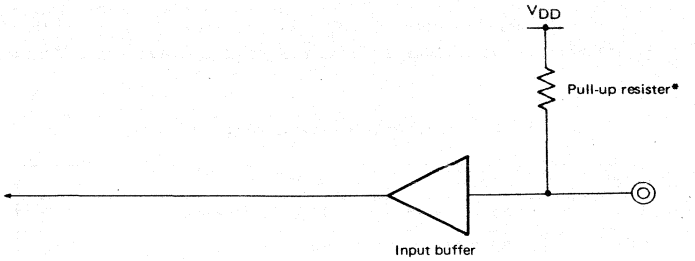


*: Only μPD17P202A-001 and μPD17P202A-002

(2) $P0C_0$/D4 through $P0C_3$/D7, $P0D_0$/D0 through $P0D_3$/D3



(3) $\overline{\text{RESET}}$



*: Only μPD17P202A-001

2. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

When the PROM is to be written, read, or verified, μPD17P201A is set in the PROM mode, and the pins shown in Table 2-1 are used. No address has to be input. Instead, the address is incremented by the clock input from the CLK pin.

Table 2-1 Pins Used to Write/Read/Verify Program Memory

Pin name	Function
V_{PP}	Apply program voltage (12.5 V) to this pin.
CLK	Address incrementing clock input
MD0 to MD3	Operation mode selector
D0 to D7	8-bit data input/output
V_{DD}	Apply operating voltage (6 V) to this pin.

2.1 OPERATION MODES FOR PROGRAM MEMORY WRITE, READ, AND VERIFY

μPD17P202A is set in the program memory write, read, or verify mode, when +6 V is applied to pin V_{DD}, and +12.5 V is applied to pin V_{PP}, after being placed in the reset status (V_{DD} = 5 V, $\overline{RESET}$ = low level) for a certain period of time.

The operation modes, selected by pens MD0 through MD3, are listed in Table 2-2.

Pins not used to write, read, or verify the program memory must be open, or grounded through pull-down resistors (470 Ω).

Table 2-2 Operation Modes for Program Memory Write, Read, and Verify

Operation mode selection						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read, verify mode
		H	x	H	H	Program inhibit mode

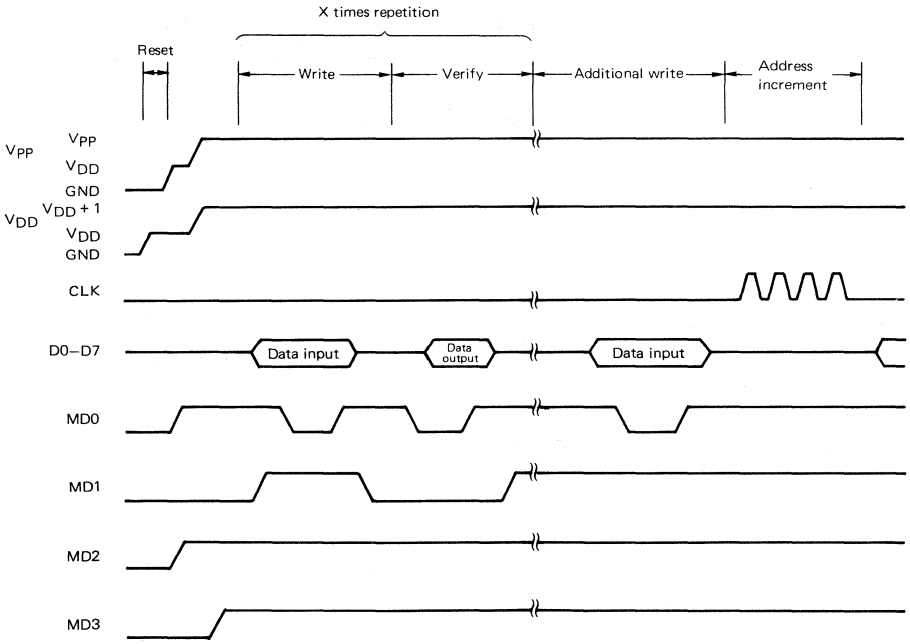
Remarks: x: L or H

2.2 PROGRAM MEMORY WRITING PROCEDURE

Write the program memory by following these steps. The program memory can be written at high speeds.

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Write data in the 1 ms write mode.
(8) Program inhibit mode
(9) Verify mode. Proceed to (10), if the memory has been written. If it has not been written, repeat (7) through (9).
(10) Additional writing for (the number of times (7) through (9) are repeated: X) x 1 ms
(11) Program inhibit mode
(12) Input a pulse four times to pin CLK, in order to increment the program memory address (by one).
(13) Repeat (7) through (12), until the last address is programmed.
(14) Program memory address 0 clear mode
(15) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(16) Turn power off.

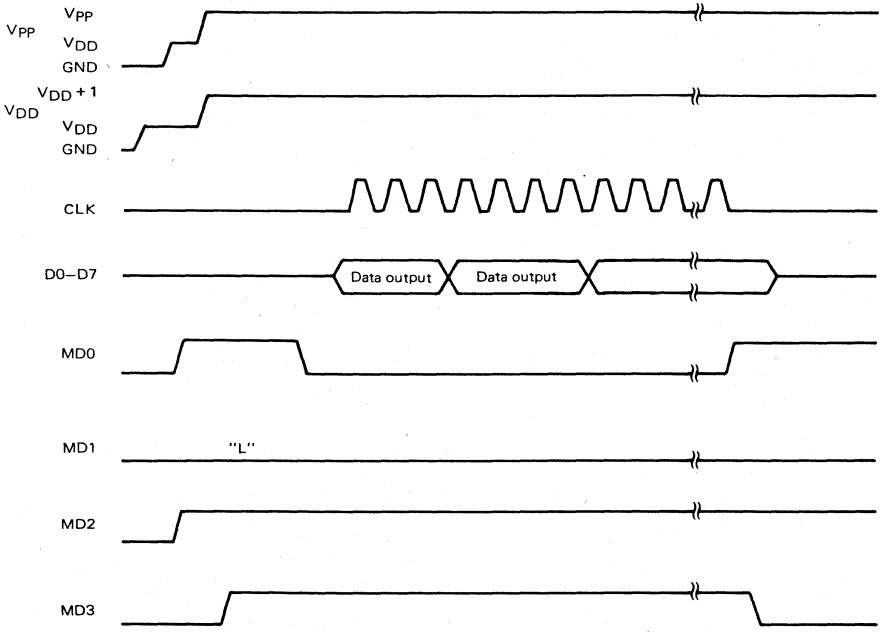
The following figure illustrates steps (2) through (12) above.



2.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins to the ground potential through resistors. Make the pin CLK low.
(2) Apply 5 V to pin V_{DD}. Make pin V_{PP} low.
(3) Wait for 10 μs. Then, apply 5 V to pin V_{PP}.
(4) Set the program memory address 0 clear mode by the mode selector pins.
(5) Apply 6 V to pin V_{DD}, and 12.5 V to pin V_{PP}.
(6) Program inhibit mode
(7) Verify mode. The data for each address is output on a one-by-one basis in a cycle during which the clock pulse is input to pin CLK four times.
(8) Program inhibit mode
(9) Program memory address 0 clear mode
(10) Decrease the voltages on pin V_{DD} and V_{PP} to 5 V.
(11) Turn power off.

The following figure illustrates steps (2) through (9) above.



3. DIFFERENCES BETWEEN μPD17P202A AND μPD17202A

In the μPD17P202A, the internal mask ROM (program memory) for the μPD17202A is replaced by the PROM which can be programmed by the user. Therefore, the program memory and some mask options are the only differences between the μPD17P202A and μPD17202A, so the CPU functions and internal hardware are identical.

The table below summarizes the differences between the μPD17P202A and μPD17202A.

Refer to the μPD17202A data sheet for details on CPU functions and internal hardware.

Item \ Device	μPD17P202A-001	μPD17P202A-002	μPD17P202A-003	μPD17202A
Program memory	• PROM • 0000H-07FFH • 2048 x 16 bits			• Mask ROM • 0000H-07FFH • 2048 x 16 bits
$\overline{\text{RESET}}$ pin pull-up resistor	Provided	None	None	(Mask option)
P0A, P0B pins pull-up resistors		Provided		
Main clock generator provided/not provided				
Subclock generator provided/not provided		None	Provided	
Pin connections	V_{PP} pin, PROM programming pin are provided.			V_{PP} pin, PROM programming pin not provided
Operating voltage range	2.2 to 5.5 V			
Package	64-pin plastic QFP (14 x 20 mm)			

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	Pins INT, $\overline{RESET}$
	C_{PIN}			10	pF	Other than pins INT, $\overline{RESET}$

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	f_X = 4 MHz
	V_{DD2}	3.5	5.0	5.5	V	f_X = 8 MHz
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Low-voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V	VDET pin external resistance = 2 MΩ	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	RESET	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{\text{RESET}}$	V_{IL} = 0 V, w/o pull-up resistor
	I_{IL3}	20	50	100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A, P0B	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
Low-Level Input Current	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	V_{OH} = V_{DD}-0.3 V
	I_{OH2}	−7.0	−15.0	−25.0	mA	REM	V_{OH} = V_{DD}-2 V
	I_{OH3}	−0.3	−1.0	−2.0	mA	LED	V_{OH} = V_{DD}-0.3 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	$\overline{\text{VDOUT}}$	V_{OH} = V_{DD}-0.3 V

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VDOUT}$	V_{OL} = 0.3 V
Common Output Current	I_{COM}	30			μA	Output voltage deviation = 0.2 V	
Segment Output Current	I_{LCD}	5			μA	Output voltage deviation = 0.2 V	
Supply Current	I_{DD1}		0.5	1.5	mA	Oepration mode	Both XT and X oscillate
	I_{DD2}		15	30	μA		Only XT oscillates
	I_{DD3}		0.5	1.5	mA	HALT mode	Both XT and X oscillate
	I_{DD4}		10	15	μA	STOP mode	Only XT oscillates

DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}-0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1: Keep V_{PP} to below +13.5 V, including the overshoot.
2: Apply V_{DD} before V_{PP}, and remove V_{DD} after V_{PP}.

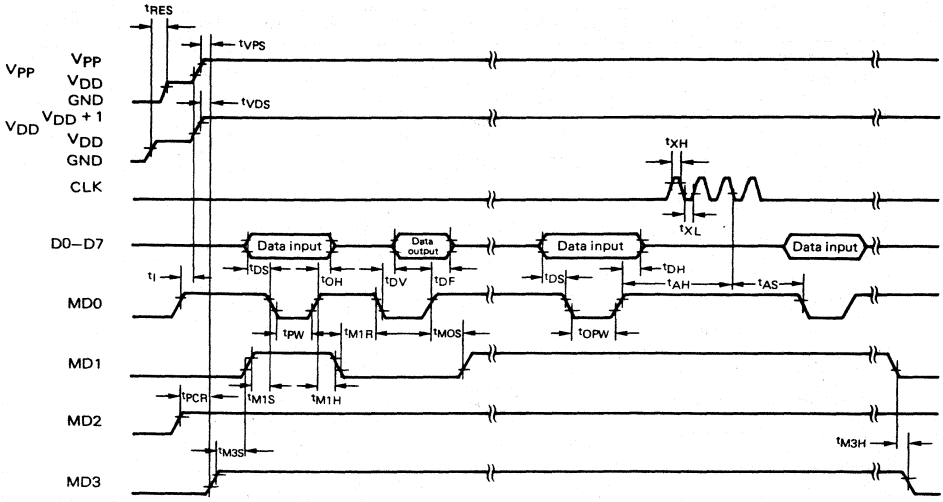
AC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address setup time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address hold time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 setup time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → data output delay time	t_{DV}	t_{DV}			1	μs	MD0=MD1=V_{IL}
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H}+t_{M1R}$ ≧ 50 μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program counter reset time	t_{PCR}	—	10			μs	
CLK input high-, low-level width	t_{XH}, t_{XL}	—	0.125			μs	
CLK Input Frequency	f_X	—			4.19	MHz	
Initial Mode Set Time	t_I	—	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	—	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	—	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	—	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	—	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	—	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

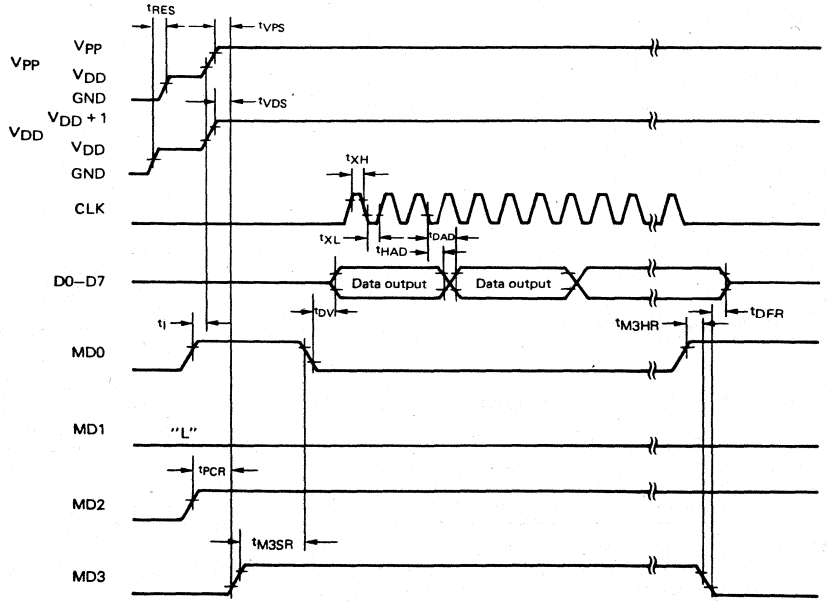
*1: Symbols for corresponding μPD27C256

*2: The internal address is incremented (+1) at the falling edge of third clock periods for the four CLK clock periods, which constitute one cycle. The internal address has no external pin connection.

PROGRAM MEMORY WRITE TIMING

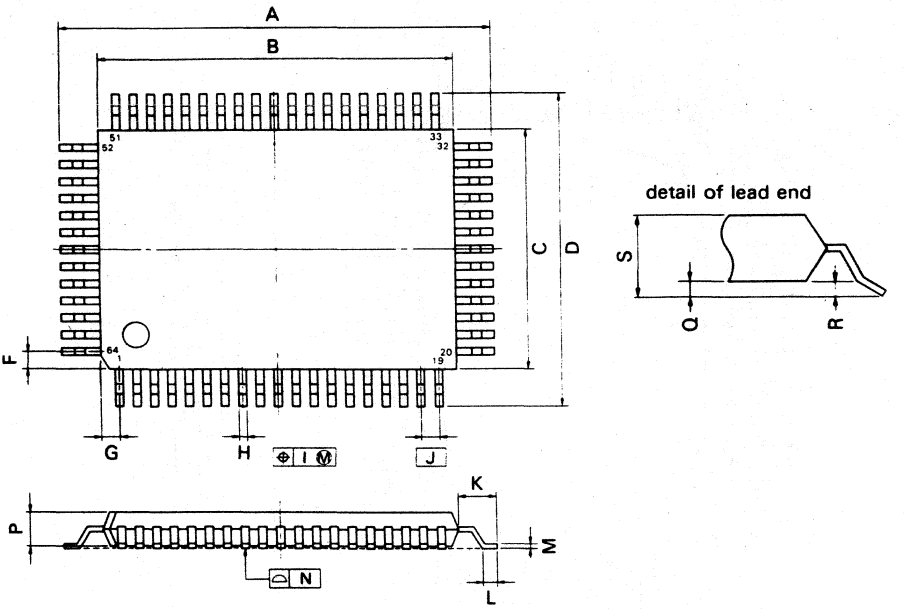


PROGRAM MEMORY READ TIMING



24. PACKAGE DIMENSION

64 PIN PLASTIC QFP (14×20)



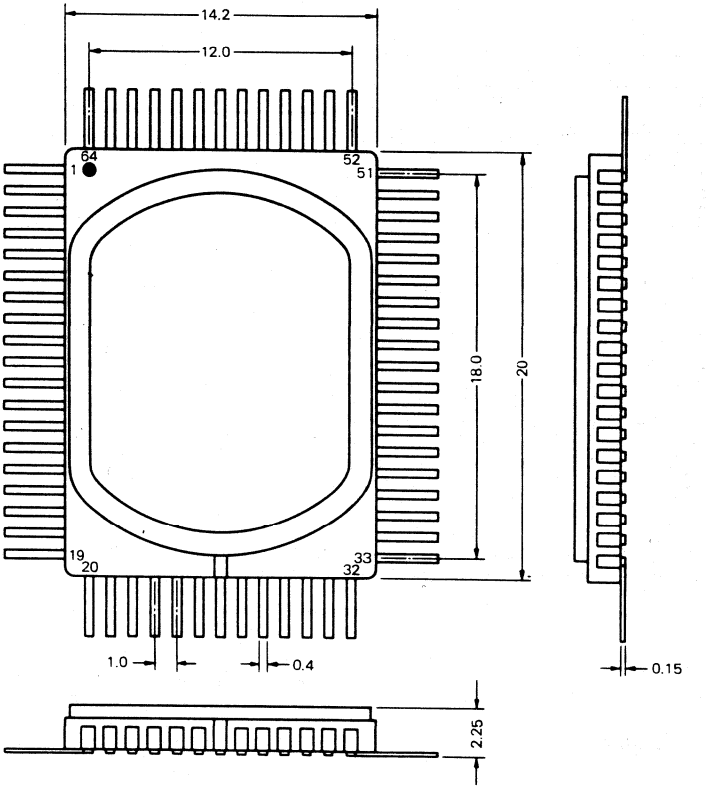
S64GF-100-3B8,3BE

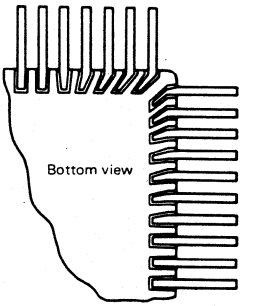
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.2^{\pm 0.4}$	$0.913^{-0.017}_{-0.016}$
B	$20^{\pm 0.2}$	$0.787^{-0.009}_{-0.008}$
C	$14^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{-0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	$0.15^{-0.10}_{-0.05}$	$0.006^{-0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

64-PIN CERAMIC QFP for ES (Reference) (Unit: mm)





Notes:

1. **The metal cap is connected to pin 26 and is at the ground level.**
2. **The bottom leads are diagonally molded.**
3. **The dimensions of the tip of the lead is not controlled, and therefore may vary.**

4-BIT SINGLE-CHIP MICROCONTROLLER WITH 16K-BIT STATIC RAM AND 3-CHANNEL TIMER FOR INFRARED REMOTE CONTROLLER

The μPD17203A is a 4-bit single-chip microcontroller for infrared remote controller. Integrated on the same die are a 16K-bit static RAM (XRAM), a 3-channel timer, a carrier generating circuit for remote controller, an amplifier for the remote control receive signal, and a waveform shaping circuit.

Employing 17K architecture, the μPD17203A can execute transfer or arithmetic operation with a single instruction between data memory addresses and between the data memory and a peripheral circuit.

Each instruction consists of 16 bits (that is, one word). The μPD17203A is housed in a 52-pin plastic QFP.

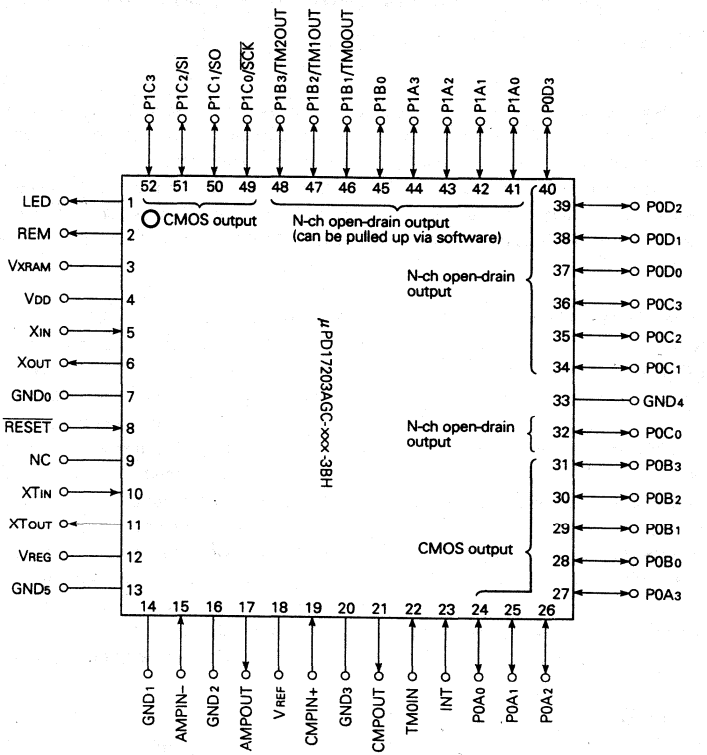
FEATURES

- Program memory (ROM): 4096 × 16 bits
- Data memory (RAM) : 336 × 4 bits
- Static RAM (XRAM) : 4096 × 4 bits
- Carrier generating circuit for infrared remote control
- Internal amplifier for infrared remote control receive signal
- Waveform shaping circuit for infrared remote control receive signal
- Abundant I/O ports (28)
- Three-line serial interface (also used as an I/O port)
- Instruction execution time: 4 μs (4 MHz ceramic oscillator is used)
- Standby function (STOP, HALT)
- Operating voltage range: 2.2 to 5.5 V (at 4 MHz)
  2.0 to 5.5 V (at 32 kHz)
- Operating clock: 4 MHz ceramic/32.768 kHz crystal oscillator
- Stack level : 5 levels (up to 2 levels for multiple interrupts)
- 8-bit timer : One channel (with modulo function)
- 10-bit timer: One channel (with modulo function)
- 16-bit timer: One channel
- Clock timer : One channel (for watchdog timer and clock)

ORDERING INFORMATION

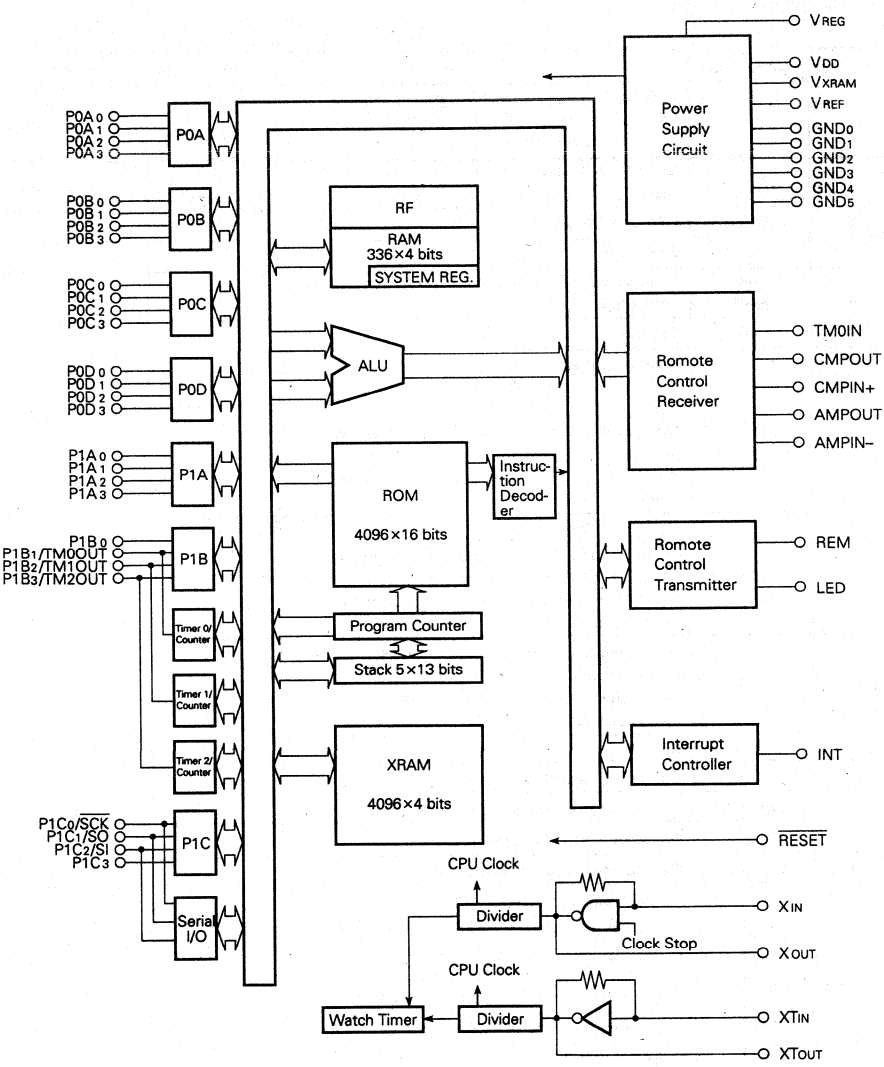
Order Code	Package	Quality Grade
μPD17203AGC-×××-3BH	52-pin plastic QFP (14 × 14 mm)	Standard

PIN CONFIGURATION (Top View)



LED	:	Indication of remote control transmission output
REM	:	Remote control transmission output
X_{IN}, X_{OUT}	:	Main clock oscillation
$\overline{RESET}$	:	Reset input
XT_{IN}, XT_{OUT}	:	Sub-clock oscillation
V_{REC}	:	Voltage regulator output
AMPIN−	:	Operational amplifier input
AMPOUT	:	Operational amplifier output
V_{REF}	:	Reference voltage output
CMPIN+	:	Comparator input
CMPOUT	:	Comparator output
INT	:	External interrupt input
TM0OUT	:	Timer 0 output
TM1OUT	:	Timer 1 output
TM2OUT	:	Timer 2 output
$\overline{SCK}$	:	Serial clock input/output
SO	:	Serial data output
SI	:	Serial data input
$P0A_0$ - $P0A_3$	:	Port 0A
$P0B_0$ - $P0B_3$	:	Port 0B
$P0C_0$ - $P0C_3$	:	Port 0C
$P0D_0$ - $P0D_3$	:	Port 0D
$P1A_0$ - $P1A_3$	:	Port 1A
$P1B_0$ - $P1B_3$	:	Port 1B
$P1C_0$ - $P1C_3$	:	Port 1C
V_{DD}	:	Power supply
V_{XRAM}	:	XRAM power supply
GND	:	Ground
NC	:	Non-connection

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN IDENTIFICATION

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
1	LED	Outputs NRZ signal in synchronization with the infrared remote control signal. Goes low when the remote control carrier is output.	CMOS push-pull	High-level output
2	REM	Outputs an infrared remote control signal (active-high)	CMOS push-pull	Low-level output
3	V_{XRAM}	XRAM power supply	–	–
4	V_{DD}	Positive power supply	–	–
5 6	X_{IN} X_{OUT}	Connect a 4 MHz ceramic oscillator for main clock oscillation.	–	(Oscillation stop)
7	GND_0	Ground.	–	–
8	$\overline{RESET}$	Input pin for system reset. The system is reset when a low-level signal is input. Main clock oscillation is halted during low-level input. A pull-up resistor can be provided by the mask option.	–	–
9	NC	Non-connection	–	–
10 11	XT_{IN} XT_{OUT}	Connect a 32 kHz crystal oscillator for subclock. When an option that does not use the subclock is selected, the divided output of the main clock is used as a timer clock.	–	–
12	V_{REG}	Output pin of voltage regulator for subclock oscillation circuit. To use this pin, an external 0.1 μF capacitor must be connected.	–	–
13	GND_5	Ground.	–	–
14	GND_1	Operational amplifier ground.	–	–
15	AMPIN–	Inverted input of operational amplifier.	–	Input
16	GND_2	Operational amplifier ground.	–	–
17	AMPOUT	Output pin for operational amplifier.	–	Output
18	V_{REF}	Outputs reference voltage. (1/2 V_{DD}). To use this pin, an external 0.1 μF capacitor must be connected.	–	–
19	CMPIN+	Non-inverted input pin for comparator. The comparator output is obtained by CMPOUT.	–	Input
20	GND_3	Operational amplifier ground.	–	–
21	CMPOUT	Output pin for comparator. To use a learning remote controller, CMPOUT and TMOIN must be externally connected.	–	Output

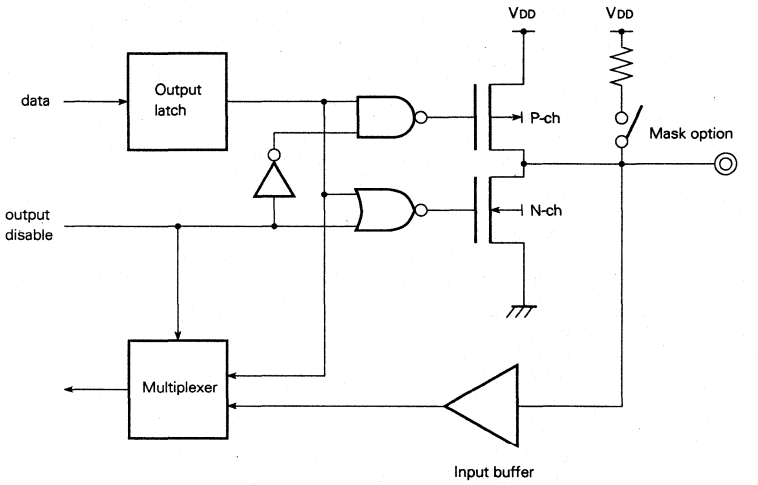
Note GND_1 to GND_3 are operational amplifier grounds.
To stabilize the operation of these amplifiers, they must be made equipotentional.

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
22	TM0IN	Clock input to timer 0. After it has been sampled by the internal clock, the input clock is supplied to timer 0 and, at the same time, to the envelope signal generation circuit. The frequency of the clock input to TM0IN can be measured by operating this timer in conjunction with timer 1.	–	Input
23	INT	Inputs external interrupt signal.	–	Input
24 | 27	P0A0 | P0A3	4-bit I/O port. Input/output can be set in 4-bit units. Pull-up resistors can be connected by mask option. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
28 | 31	P0B0 | P0B3	4-bit I/O port. Input/output can be set in 4-bit units. Pull-up resistors can be connected by mask option. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
32 34 | 36	P0C0 P0C1 | P0C3	4-bit I/O port. Input/output can be set in 4-bit units. The standby mode is released when at least one pin of this port goes high.	N-ch open-drain	Input
33	GND4	Ground.	–	–
37 | 40	P0D0 | P0D3	4-bit I/O port. Input/output can be set in 4-bit units. The standby mode is released when at least one pin of this port goes high.	N-ch open-drain	Input
41 | 44	P1A0 | P1A3	4-bit I/O port. Input/output can be set in bit units. Pull-up resistors can be connected by program.	N-ch open-drain	Input
45 46 47 48	P1B0 P1B1/TM0OUT P1B2/TM1OUT P1B3/TM2OUT	Port 1B and timer output. • P1B0 - P1B3 · 4-bit I/O port · Input/output can be set in bit units. · Pull-up resistors can be connected by the program. • TM0OUT - TM2OUT · Timer outputs	N-ch open-drain	Input (P1B0 - P1B3)
49 50 51 52	P1C0/$\overline{SCK}$ P1C1/SO P1C2/SI P1C3	Port 1C and input/output for serial interface • P1C0 - P1C3 · 4-bit I/O port · Input/output can be set in bit units. • $\overline{SCK}$, SO, SI · $\overline{SCK}$: Serial clock input/output · SO : Serial data output · SI : Serial data input	CMOS push-pull	Input (P1C0 - P1C3)

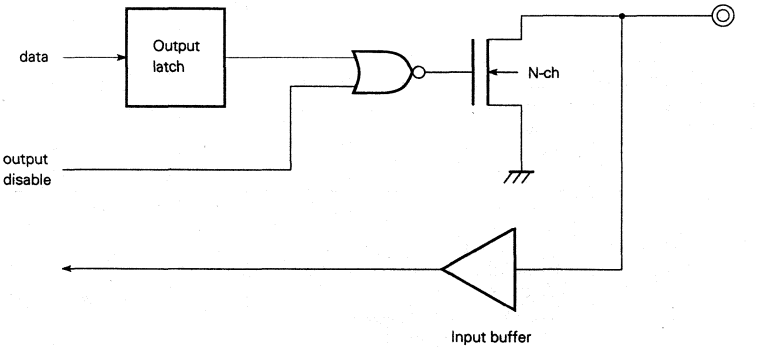
1.2 PIN INPUT/OUTPUT CIRCUITS

This section shows simplified diagrams illustrating the input/output circuits of the μPD17203A pins.

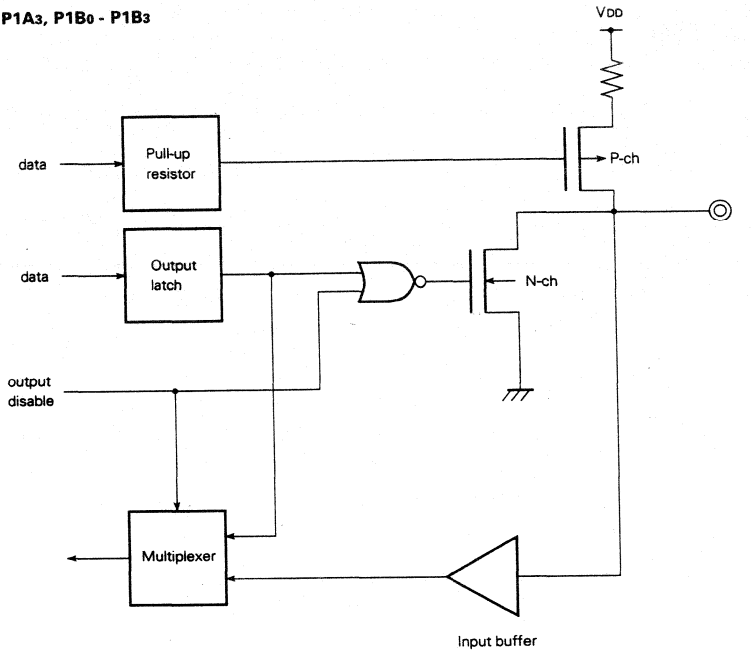
(1) P0A0 - P0A3, P0B0 - P0B3



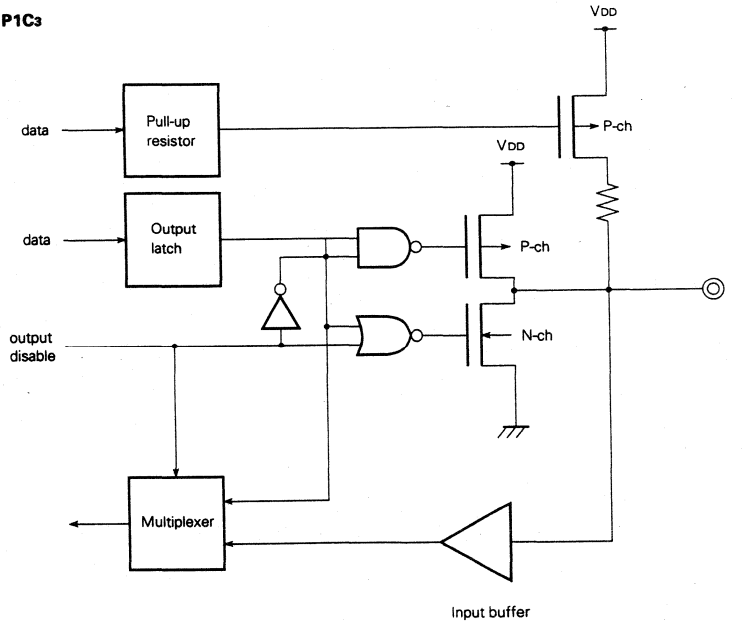
(2) P0C0 - P0C3, P0D0 - P0D3



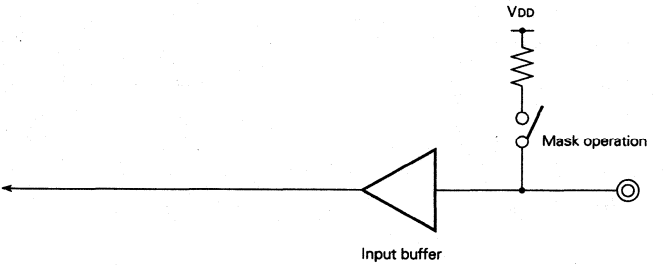
(3) $P1A_0$ - $P1A_3$, $P1B_0$ - $P1B_3$



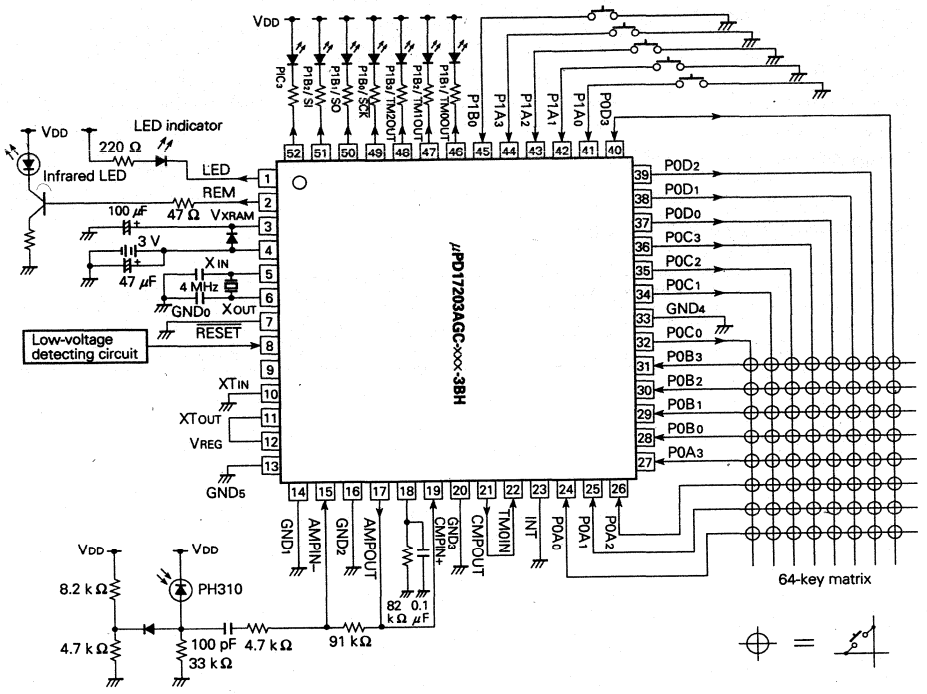
(4) $P1C_0$ - $P1C_3$



(5) $\overline{\text{RESET}}$



20. APPLICATION CIRCUIT EXAMPLE



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

21. ELECTRICAL CHARACTERISTICS

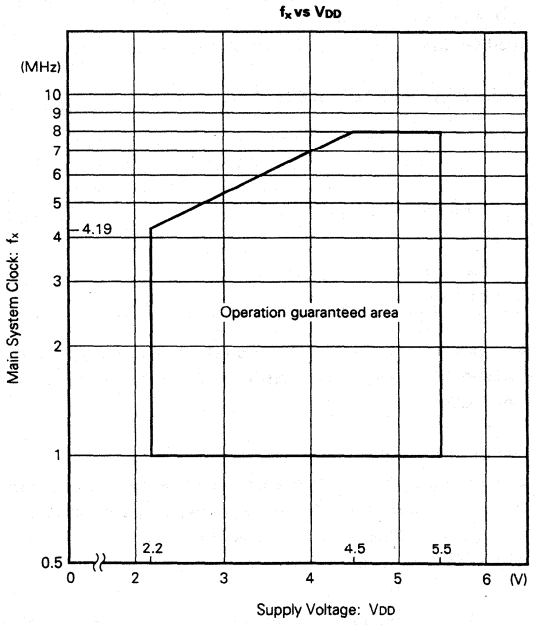
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

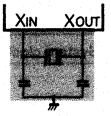
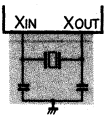
CAPACITANCE (T_a = 25 °C, V_{DD} = 0V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			10	pF	INT and $\overline{\text{RESET}}$ pins
	C_{PIN}			10	pF	Other than INT and $\overline{\text{RESET}}$ pins

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+30°C
	V_{DD2}	2.7	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+55°C
	V_{DD3}	2.9	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+75°C
	V_{DD4}	4.75	5.0	5.5	V	System clock: f_X = 6 MHz, Ta = -20...+50°C
	V_{DD5}	2.0	3.0	5.5	V	System clock: f_X = 32 kHz, Ta = -20...+75°C
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

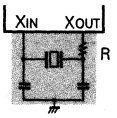
RESONATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic Oscillator **Note 3**		Oscillation frequency (fx) **Note 1**		. 1.0	4.0	8.0	MHz
		Oscillation stabilization time **Note 2**	From when V_{DD} reaches the minimum oscillation voltage			4	ms
Crystal Oscillator **Note 3**		Oscillation frequency (fx) **Note 1**		1.0	4.0	8.0	MHz
		Oscillations stabilization time **Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms

Note 1 The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2 The oscillation stabilization time is the time required for stabilizing the oscillation after V_{DD} is applied or the STOP mode is released.

3 The recommended oscillators are shown in the table described later.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 2.0 to 5.5 V)

RESONATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal Oscillator		Oscillation frequency (fXT)			32.768		kHz
		Oscillation stabilization time				10	s

Note When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the following notations must be read and observed for wiring within the shaded area in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line.**
- **Capacitors used in the oscillators must always be grounded to V_{SS} potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

RECOMMENDED OSCILLATORS

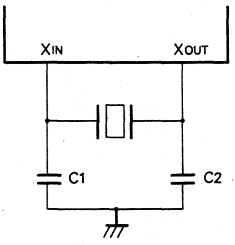
MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR

Manufacturer	Product name	External capacitor (pF)		Oscillation voltage (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW	none	none	2.0	6.0	
	CST4.19MGW	none	none	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

Manufacturer	Frequency (MHz)	Retainer	External capacitor (pF)		Oscillation voltage (V)		Remarks
			C1	C2	MIN.	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

OSCILLATOR CIRCUIT



DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	2.4		3.0	V	$\overline{RESET}$ and INT pins	
	V_{IH2}	2.1		3.0	V	Other than $\overline{RESET}$ and INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.6	V	$\overline{RESET}$ and INT pins	
	V_{IL2}	0		0.9	V	Other than $\overline{RESET}$ and INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	V_{IH} = 3.0 V
	I_{IH2}			0.2	μA	TM0IN	V_{IH} = 3.0 V
	I_{IH3}			0.2	μA	$\overline{RESET}$	V_{IH} = 3.0 V
	I_{IH4}			0.2	μA	P0A - P0D	V_{IH} = 3.0 V
	I_{IH5}			0.2	μA	P1A - P1C	V_{IH} = 3.0 V
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			0.2	μA	$\overline{RESET}$	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL4}	30	60	120	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
	I_{IL5}			0.2	μA	P0A, P0B	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL6}	8	15	30	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
	I_{IL7}			0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL8}			0.2	μA	P1A - P1C	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL9}	30	60	120	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	V_{OH} = 2.7 V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	V_{OH} = 2.7 V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	V_{OH} = 1.0 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	V_{OH} = 2.7 V
	I_{OH5}	−0.3	−1.0	−2.0	mA	CMPOUT	V_{OH} = 2.7 V
Low-level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B, P1C	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D, P1A, P1B	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = -20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz) (contd)

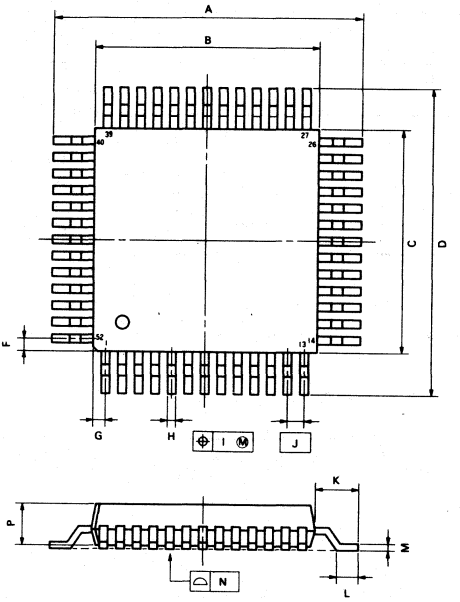
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
V_{REF} Output Voltage	V_{REF}	1.3	1.5	1.7	V	V_{REF} pin external capacity = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	Both XT and X oscillate.
	I_{DD2}		15	30	μA		Only XT oscillates.
	I_{DD3}			2.0	mA	HALT mode	Both XT and X oscillate.
	I_{DD4}		10	15	μA		Only XT oscillates.
XRAM Holding Voltage	V_{XRAM}	1.3	3.0	5.5	V		
XRAM Supply Current	I_{XRAM1}		3.0		μA	Operation mode, V_{XRAM} = 3 V	
	I_{XRAM2}		0.2	1.0	μA	HALT mode, V_{XRAM} = 3 V, T_a = 25 °C	

OPERATIONAL AMPLIFIER/COMPARATOR CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Unity Gain Frequency of Operational Amplifier		0.5	1.0	10	MHz	
Input Offset Voltage of Operational Amplifier			10		mV	
Same Phase Input Voltage Range of Operational Amplifier		0.3		2.7	V	
Output Voltage Range of Operational Amplifier		0.1		2.9	V	
Operational Amplifier Through Rate		1			V/μs	
Input Offset Voltage of Comparator		40	60	80	mV	
Same Phase Input Voltage Range of Comparator		0		3.0	V	
Minimum Output Pulse Width of Comparator		3	4	5	μs	
Comparator Through Rate		10			V/μs	

22. PACKAGE DIMENSIONS

52PIN PLASTIC QFP (□14)



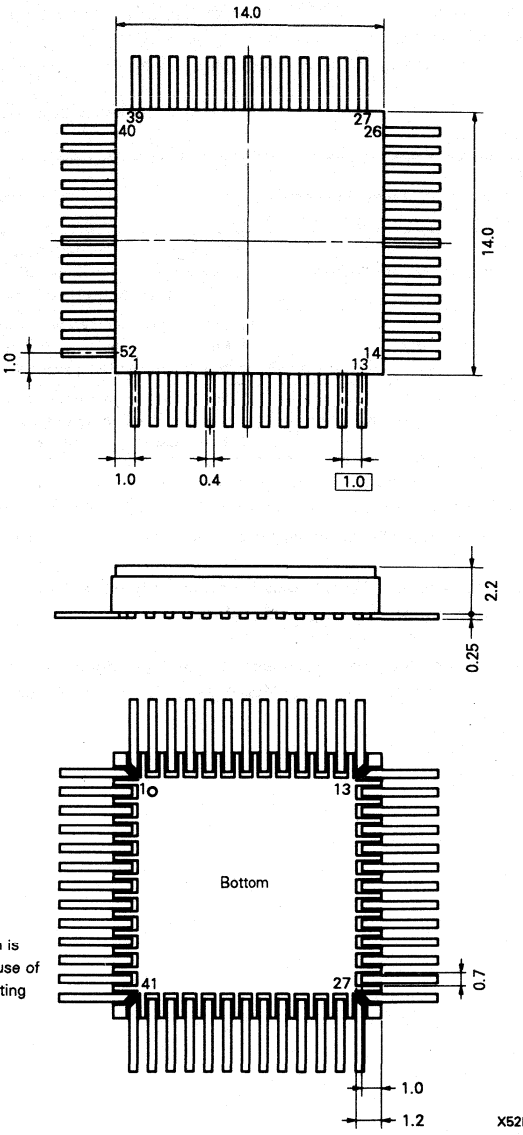
S52GC-100-3BH

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-pin ceramic QFP (14 sq.) (for ES) (unit: mm)



X52B-100B

Note The lead length is not rated because of the lead tip cutting process.

23. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD17203A by soldering, soldering should be performed under the following recommended conditions.

For other soldering methods, please consult with NEC sales personnel.

Table 23-1 Soldering Conditions

Recommended conditions reference code	Soldering method	Soldering conditions
IR30-162	Infrared reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
VP15-162	VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
WS60-162	Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max. Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
Pin partial heating	Pin partial heating	Pin temperature: 300 °C max., Timer: 10 seconds max.

* Number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 % RH max.

Note **Do not use different soldering methods together (however, pin partial heating can be performed with other soldering methods).**

Remarks For detail on recommended soldering conditions for surface mounting, refer to the information document "Surface Mount Device Mounting Manual" (IEI-1207).

APPENDIX A COMPARISON BETWEEN μPD17203A AND μPD17204

Part number	μPD17203A	μPD17204
ROM	4096 × 16 bits	7936 × 16 bits
RAM	336 × 4 bits	
SRAM	4096 × 4 bits	2048 × 4 bits
Instruction execution time	4 μs (when 4 MHz ceramic oscillator is used)	
Stack level	5 levels (up to 2 levels for multiple interrupts)	7 levels (up to 2 levels for multiple interrupts)
Number of I/O ports	28	
Serial interface	8 bits (3-line: 1 channel)	
Interrupt	7 channels	
	External interrupt: 1 channel	
	Internal interrupt: 6 channels	
Timer	4 types	
	8-bit timer	
	10-bit timer	
	16-bit timer	
	Clock timer (also used as a watchdog timer)	
Standby function	STOP mode, HALT mode	
Recommended operating voltage range	V_{DD} = 2.2 to 5.5 V (at 4 MHz), V_{DD} = 2.0 to 5.5 V (at 32 kHz)	
Package	52-pin plastic QFP	

The μPD17P203A is provided with a one-time PROM in the place of the internal ROM in the μPD17203A.

Since a program can be written into the PROM for this microcomputer, it is suitable for experimental production or small-scale production of systems using μPD17203A.

It is recommended that you also read the separately available reference materials on μPD17203A.

FEATRUES

- Internal one-time PROM: 4,096 x 16 bits
- Single power source: 2.2 to 5.5 V

ORDERING INFORMATION

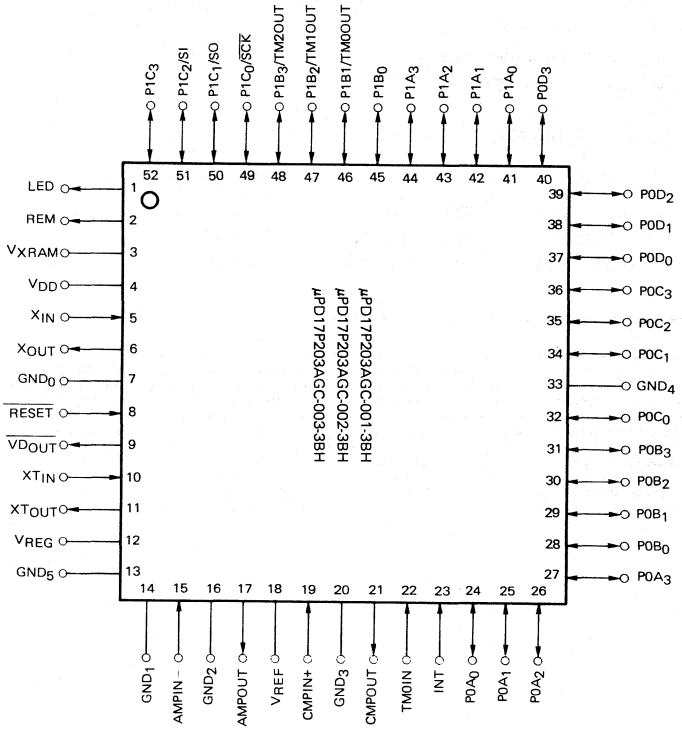
Order Code	Package	Quality Grade
μPD17P203AGC-001-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-002-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-003-3BH	52-pin plastic QFP	Standard

The differences among the above models are as follows:

Item	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
$\overline{\text{RESET}}$ pin pull-up resistor	Provided	Not provided	Not provided	Mask option
P0A and P0B pins pull-up resistor	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option

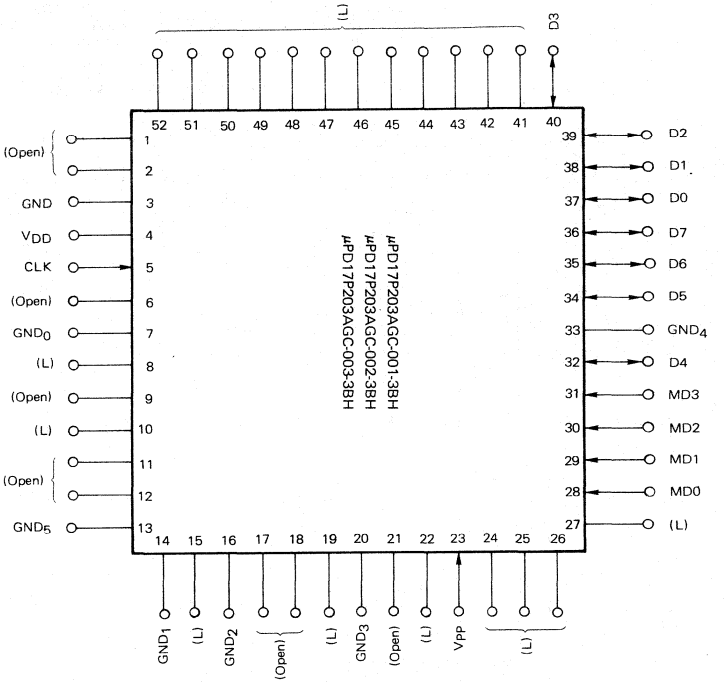
PIN CONFIGURATION (Top View)

(1) For Ordinary Operations



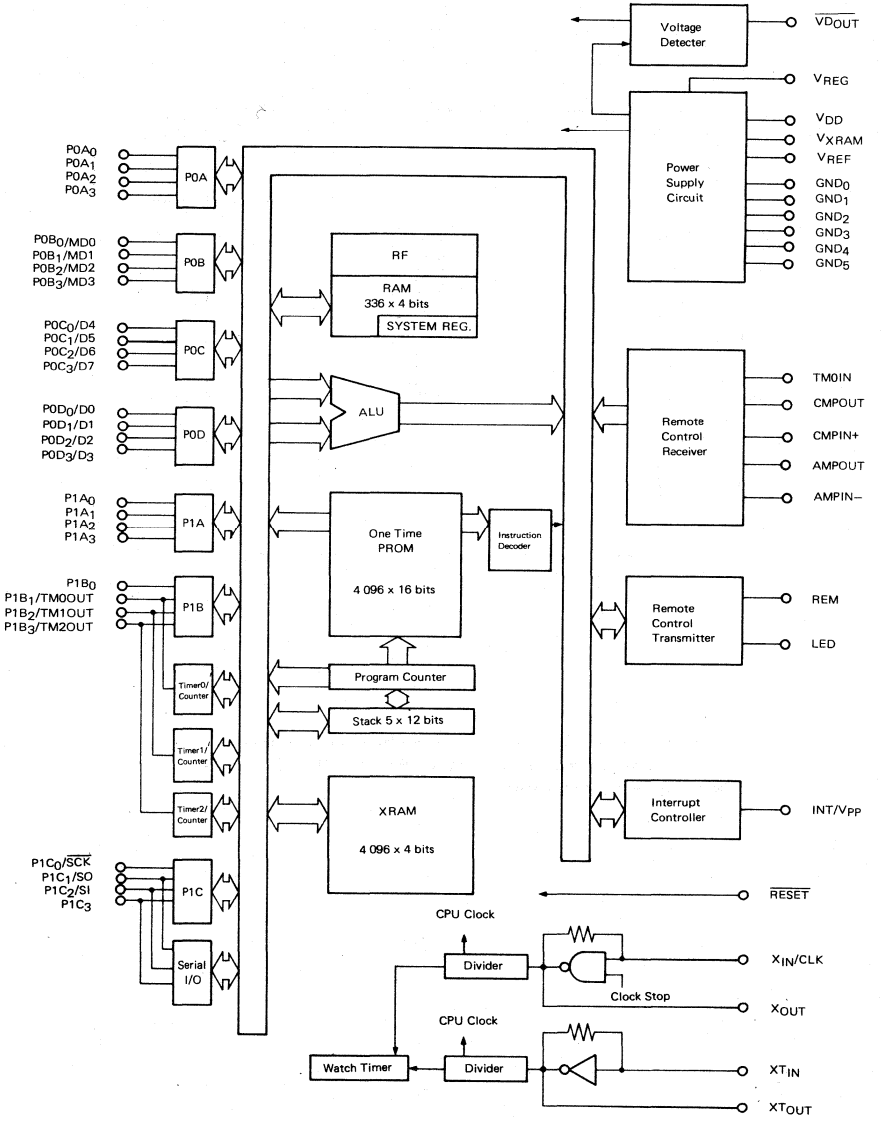
LED	:	Remote controller signal transmission output display
REM	:	Remote controller signal transmission output
X_{IN}, X_{OUT}	:	Main clock oscillator
$\overline{RESET}$	:	Reset input
$\overline{VD_{OUT}}$	:	Low voltage detector output
XT_{IN}, XT_{OUT}	:	Subclock oscillator
V_{REG}	:	Voltage regulator output
AMPIN−	:	Operational amplifier input
AMPOUT	:	Operational amplifier output
V_{REF}	:	Reference voltage output
CMPIN+	:	Comparator input
CMPOUT	:	Comparator output
TM0IN	:	Timer 0 input
INT	:	External interrupt input
TM0OUT	:	Timer 0 output
TM1OUT	:	Timer 1 output
TM2OUT	:	Timer 2 output
$\overline{SCK}$	:	Serial clock input/output
SO	:	Serial data output
SI	:	Serial data input
$P0A_0$–$P0A_3$	:	Port 0A
$P0B_0$–$P0B_3$	:	Port 0B
$P0C_0$–$P0C_3$	:	Port 0C
$P0D_0$–$P0D_3$	:	Port 0D
$P1A_0$–$P1A_3$	:	Port 1A
$P1B_0$–$P1B_3$	:	Port 1B
$P1C_0$–$P1C_3$	:	Port 1C
CLK	:	PROM clock input
MD0–MD3	:	PROM mode selection
D0–D7	:	PROM data input/output
V_{PP}	:	PROM power
V_{DD}	:	Power
V_{XRAM}	:	XRAM power
GND	:	Ground

(2) PROM programming mode



Note: ( ) indicates processing of pins not used in the PROM programming mode.
L : Ground each of these pins through a resistor (470 Ω).
Open : Connect nothing to these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PORT PINS

Symbol	I/O	Shared by: *	Function	At reset
$P0A_0$–$P0A_3$	I/O	–	4-bit I/O port (Port 0A). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0B_0$–$P0B_3$	I/O	(MD0–MD3)	4-bit I/O port (Port 0B). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0C_0$–$P0C_3$	I/O	(D4–D7)	4-bit I/O port (Port 0C). Can be set in input or output mode in 4 bit units. N-ch open-drain in output mode.	Input
$P0D_0$–$P0D_3$	I/O	(D0–D3)	4-bit I/O port (Port 0D). Can be set in input or output mode in units of 4 bits. N-ch open-drain in output mode.	Input
$P1A_0$–$P1A_3$	I/O	–	4-bit I/O port (Port 1A). Can be set in input or output mode in bit units. N-ch open-drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_0$	I/O	–	4-bit I/O port (Port 1B). Can be set in input or output mode in bit units. N-ch open drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_1$–$P1B_3$		TM0OUT–TM2OUT		
$P1C_0$	I/O	$\overline{SCK}$	4-bit I/O port (Port 1C). Can be set in input or output mode in bit units. Pull-up resistor can be connected by program in I/O mode.	Input
$P1C_1$		SO		
$P1C_2$		SI		
$P1C_3$		–		

*( ): Pins shared in PROM programming mode.

1.2 PINS OTHER THAN PORT PINS (IN ORDINARY OPERATION MODE)

Symbol*	I/O	Shared by:	Function	At reset
LED	Output	–	For display of infrared remote controller signal output	Low-level output
REM	Output	–	Infrared remote controller signal output	Low-level output
X_{IN}	Input	–	For main clock oscillator. Connect 4 MHz ceramic oscillator to these pins.	–
X_{OUT}	Output	–		
$\overline{RESET}$	Input	–	RESET signal input	–
$\overline{VDOUT}$	Output	–	Low-voltage detector circuit output	–
XT_{IN}	Input	–	For subclock oscillator	–
XT_{OUT}	Output	–		–
V_{REG}	Output	–	Output from voltage regulator for subclock oscillator	–
AMPIN–	Input	–	Inverted input from internal operational amplifier	–
AMPOUT	Output	–	Internal operational amplifier output	–
V_{REF}	Output	–	Reference voltage output	–
CMPIN+	Input	–	Non-inverted input for comparator	–
CMPOUT	Output	–	Comparator output	–
TM0IN	Input	–	Clock input to timer 0	–
INT	Input	(V_{PP})	External interrupt signal input	–
V_{DD}	–	–	Power	–
V_{XRAM}	–	–	Power to XRAM	–
GND_0–GND_5	–	–	Ground	–

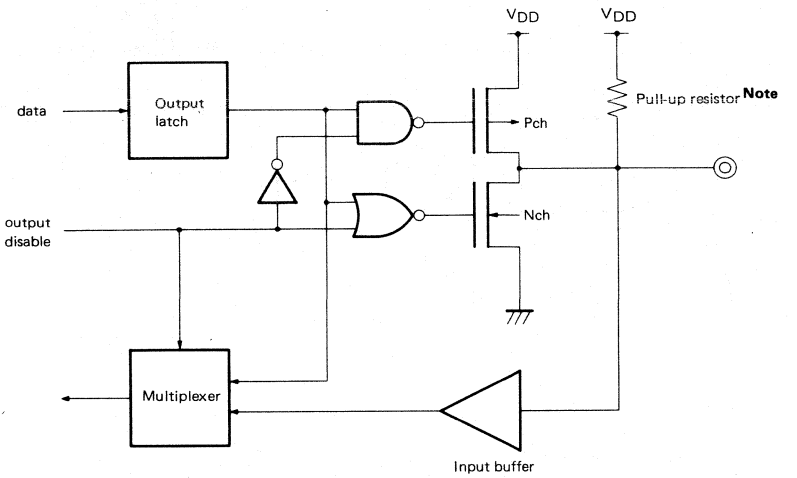
1.3 PINS OTHER THAN PORT PINS (IN PROM PROGRAMMING MODE)

Symbol	I/O	Shared by:	Function	At reset
CLK	Input	X_{IN}	Address updating clock input	–
D0–D3	I/O	$P0D_0$–$P0D_3$	8-bit data input/output	Input
D4–D7		$P0C_0$–$P0C_3$		
MD0–MD3	Input	$P0B_0$–$P0B_3$	Operation mode selection	Input
V_{PP}	–	INT	Applies program voltage (12.5 V). Used as INT pin in ordinary operation mode.	–

1.4 INPUT/OUTPUT CIRCUITS

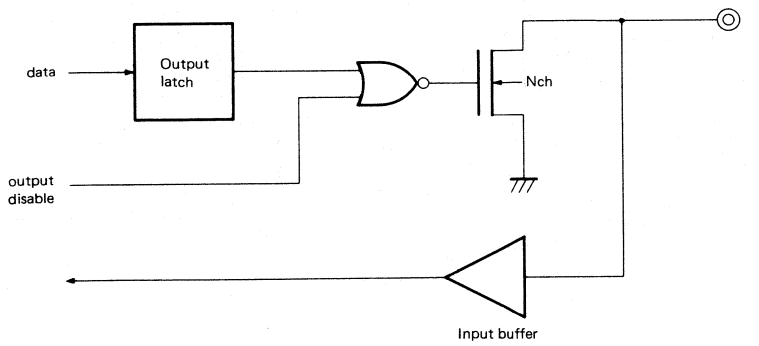
The input/output circuit for each μPD17P203A's pin are shown below.

(1) $P0A_0$–$P0A_3$, $P0B_0$/MD0–$P0B_3$/MD3

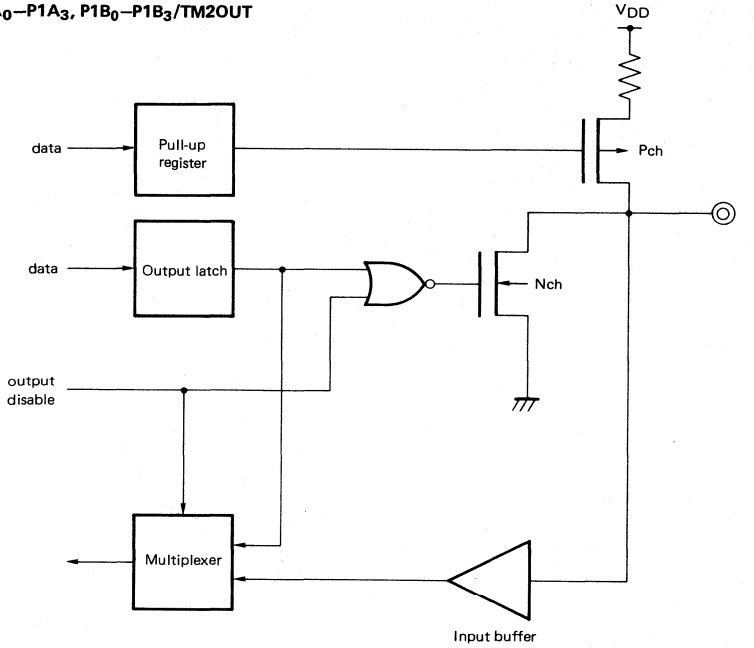


Note: μPD17P203A-001 and -002 only.

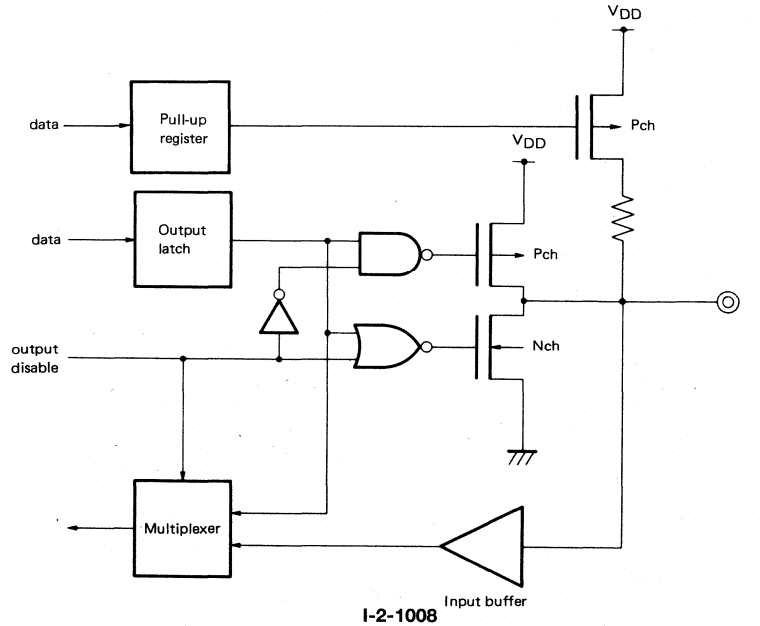
(2) $P0C_0$/D4–$P0C_3$/D7, $P0D_0$/D0–$P0D_3$/D3



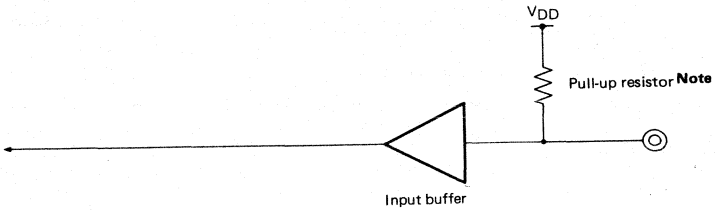
(3) $P1A_0$–$P1A_3$, $P1B_0$–$P1B_3$/TM2OUT



(4) $P1C_0/\overline{SCK}$–$P1C_3$



(3) $\overline{\text{RESET}}$



Note: μPD17P203A-001 only.

2. DIFFERENCES BETWEEN μPD17P203A AND μPD17203A

Since μPD17P203A replaces the internal mask ROM for μPD17203A with a PROM that can be written by the user, the only differences between the two microcomputers are the program memory and mask option. Their CPU functions and internal hardware are essentially the same. The following table lists the differences between μPD17P203A and μPD17203A.

Refer to the μPD17203A Data Sheet for the CPU functions and internal hardware for μPD17P203A.

Item \ Product name	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
Program memory	• PROM • 0000H-0FFFH • 4,096 x 16 bits			• Mask ROM • 0000H-0FFFH • 4,096 x 16 bits
Pull-up resistor for $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	Mask option
Pull-up resistor for P0A and P0B pins	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option
Pin connection	Vpp and PROM programming pins are provided			Vpp and PROM programming pins are not provided
Operating voltage range	2.2 to 5.5 V			
Package	52-pin plastic QFP			

3. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P203A internal program memory is a one-time 4,096 x 16 bit PROM.

The write, read, and verify this one-time PROM, the pins shown in the following table are used. Note that no address input pin is provided. Instead, the address is updated by the clock signal input from the CLK pin.

Pin	Function
V_{PP}	Program voltage application
CLK	Address updating clock input
MD0–MD3	Operation mode selection
D0–D7	8-bit data input/output

3.1 OPERATION MODES WHEN PROGRAM MEMORY IS WRITTEN, READ, OR VERIFIED

μPD17P203A is set in the program memory write, read, and verify mode, when, +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after it has been reset for a certain period of time (V_{DD} = 5 V, $\overline{RESET}$ = 0 V). Once this mode has been set, the following operation modes are available, depending on the setting of the MD0 through MD3 pins. Note that all the unused pins are pulled down with resistors to the ground potential.

Operation mode setting						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read and verify mode
		H	X	H	H	Program inhibit mode

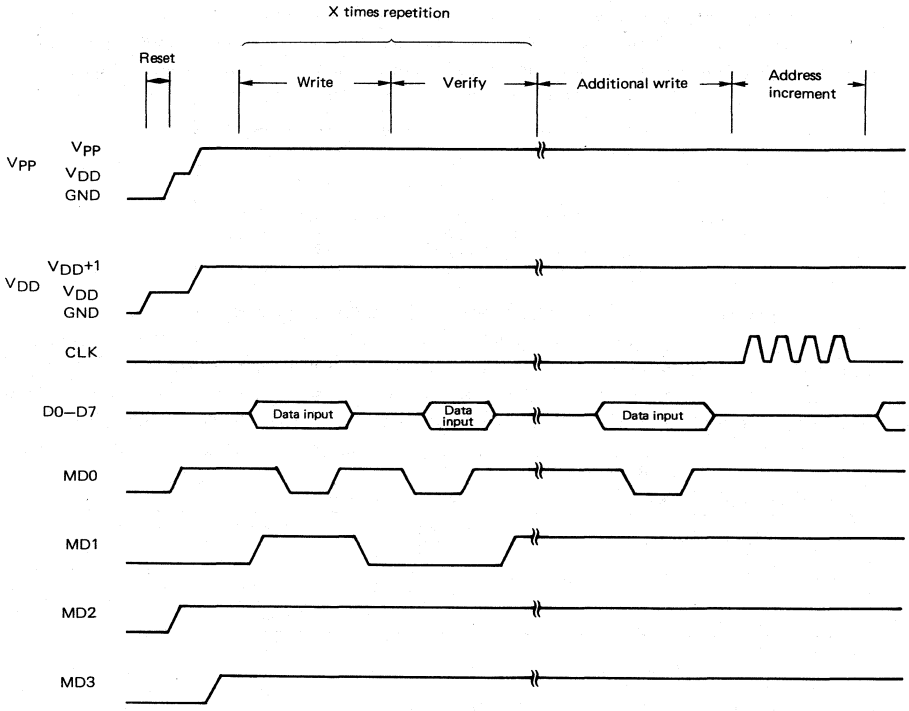
X: L or H

3.2 PROGRAM MEMORY WRITING PROCEDURE

The program memory can be written in the following procedure at high speeds:

(1) Pull down the unused pins with resistors to the ground potential. Make the CLK pin low.
(2) Apply 5 V to the V_{DD} pin. Make the V_{PP} pin low.
(3) Wait for 10 μs. Then apply 5 V to the V_{PP} pin.
(4) Set the program memory address 0 clear mode by using the mode selection pins.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the data has been correctly written, proceed to step (10). If not, repeat (7) through (9).
(10) Additional write for (the number of times (7) through (9) are repeated: X) x 1 ms.
(11) Set the program inhibit mode.
(12) Input a pulse to the CLK pin four times to increment the program memory address by one.
(13) Repeat (7) through (12) until the last address is written.
(14) Set the program memory address 0 clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn off power.

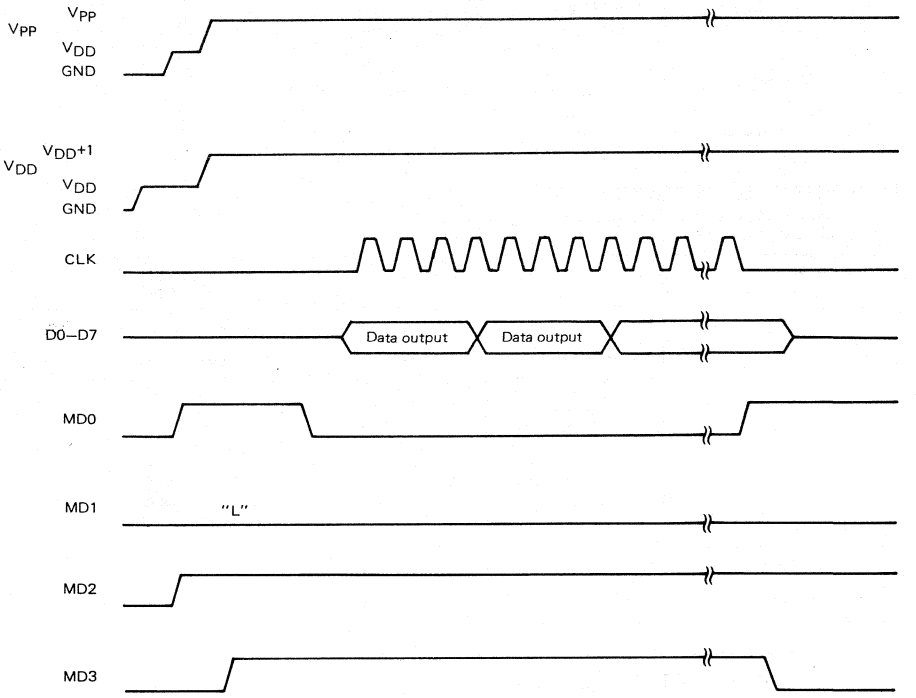
Steps (2) through (12) are illustrated below.



3.3 PROGRAM MEMORY READING PROCEDURE

(1) Pull down the unused pins with resistors to the ground potential. Make the CLK pin low.
(2) Apply 5 V to the V_{DD} pin. Make the V_{PP} pin low.
(3) Wait for 10 μs. Then apply 5 V to the V_{PP} pin.
(4) Set the program memory address 0 clear mode by using the mode selection pins.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Set the verify mode. Input the clock pulse to the CLK pin. Data for one address is output each time the pulse is input four times.
(8) Set the program inhibit mode.
(9) Set the program memory address 0 clear mode.
(10) Apply 5 V to the V_{DD} and V_{PP} pins.
(11) Turn off power.

Steps (2) through (9) are illustrated below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+30°C
	V_{DD2}	2.7	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+55°C
	V_{DD3}	2.9	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+75°C
	V_{DD4}	4.75	5.0	5.5	V	System clock: f_X = 6 MHz, Ta = -20...+50°C
	V_{DD5}	2.0	3.0	5.5	V	System clock: f_X = 32 kHz, Ta = -20...+75°C
XRAM Supply Voltage	V_{XRAM}	1.3		V_{DD}	V	$V_{XRAM} \leq V_{DD}$
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			10	pF	INT, $\overline{\text{RESET}}$ pins
	C_{PIN}			10	pF	Other than INT, $\overline{\text{RESET}}$ pin

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Low Voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V		
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{RESET}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	TM0IN	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	$\overline{RESET}$	$V_{IH} = V_{DD}$
	I_{IH4}			0.2	μA	P0A–P0D	$V_{IH} = V_{DD}$
	I_{IH5}			0.2	μA	P1A–P1C	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			0.2	μA	$\overline{RESET}$	V_{IL} = 0 V w/o pull-up resistor
	I_{IL4}	30	60	120	μA		I_{IL} = 0 V w/pull-up resistor
	I_{IL5}	8	15	30	μA	P0A, P0B	V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL7}			0.2	μA	P1A–P1C	V_{IL} = 0 V w/o pull-up resistor
	I_{IL8}	30	60	120	μA		I_{IL} = 0 V w/pull-up resistor
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	$V_{OH} = V_{DD}$−0.3 V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	$V_{OH} = V_{DD}$−0.3 V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	$V_{OH} = V_{DD}$−2 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	$V_{OH} = V_{DD}$−0.3 V
	I_{OH5}	−0.3	−1.0	−2.0	mA	$\overline{VD_{OUT}}$	$V_{OH} = V_{DD}$−0.3 V
	I_{OH6}	−0.3	−1.0	−2.0	mA	CMPOUT	$V_{OH} = V_{DD}$−0.3 V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VD_{OUT}}$	V_{OL} = 0.3 V
	I_{OL6}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V
V_{REF} Output Voltage	V_{REF}	0.8	1.2	1.6	V	External capacitance for V_{REF} pin = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}			2.0	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
XRAM Hold Voltage	V_{XRAM}	1.3	3.0	5.5	V	Operation mode, V_{XRAM} = 3 V	
XRAM Supply Current	I_{XRAM1}		3.0		μA	HALT mlde, V_{XRAM} = 3 V, T_a = 25 °C	
	I_{XRAM2}		0.2	1.0	μA		

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note: 1. Keep V_{PP} to less than +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP}. Remove V_{DD} after V_{PP}.

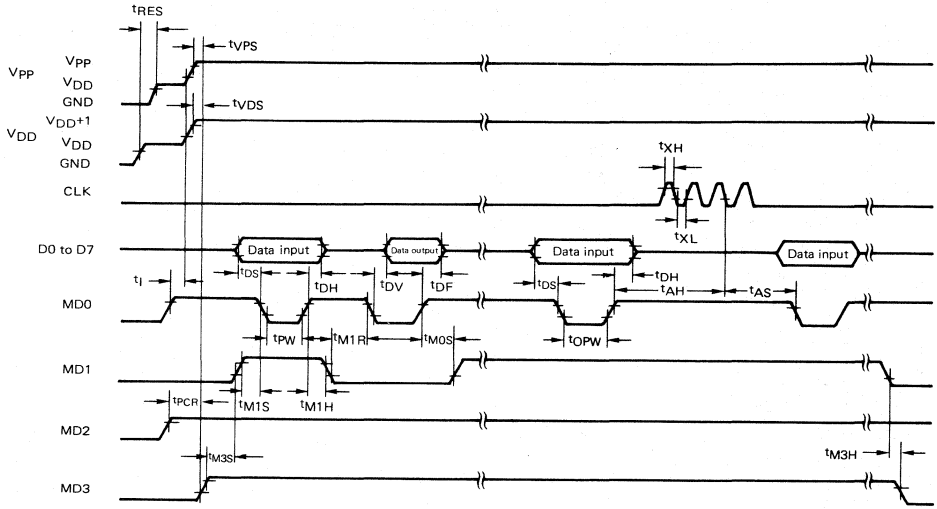
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{MIS}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High, Low Level Widths	t_{XH}, t_{XL}	–	0.063			μs	
CLK Input Frequency	f_X	–			8	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

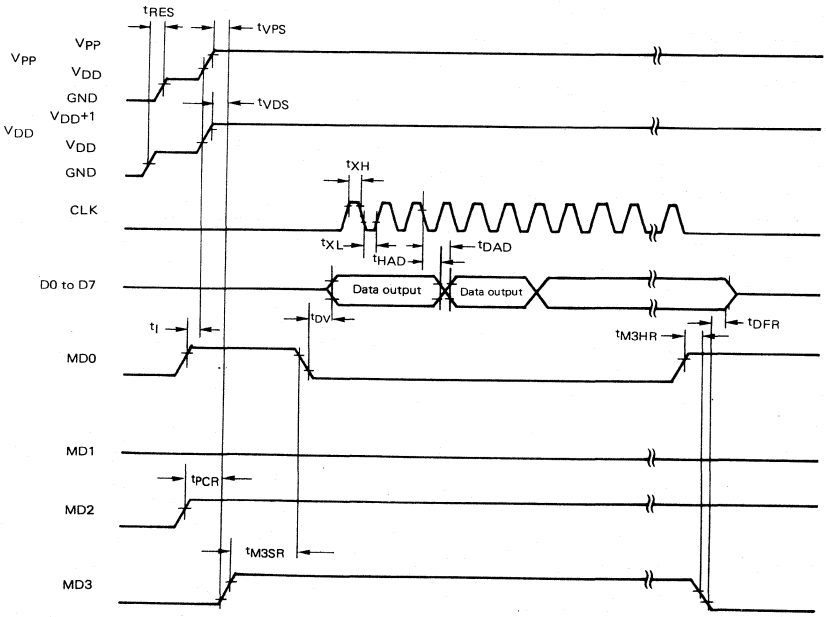
*1. Corresponding symbols of μPD27C256.

*2. The internal address signal is incremented by one at the falling edge of the third CLK input signal and is not connected to a pin.

PROGRAM MEMORY WRITE TIMING

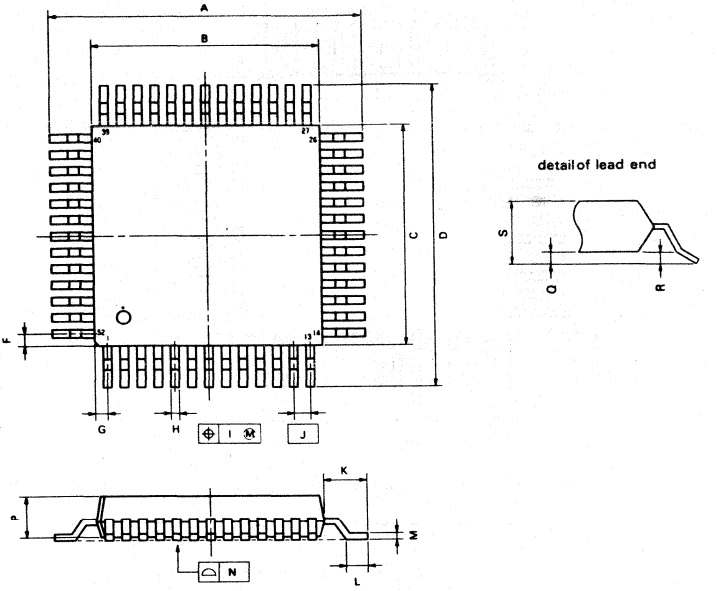


PROGRAM MEMORY READ TIMING



22. PACKAGE DIMENSIONS

52PIN PLASTIC QFP (□14)



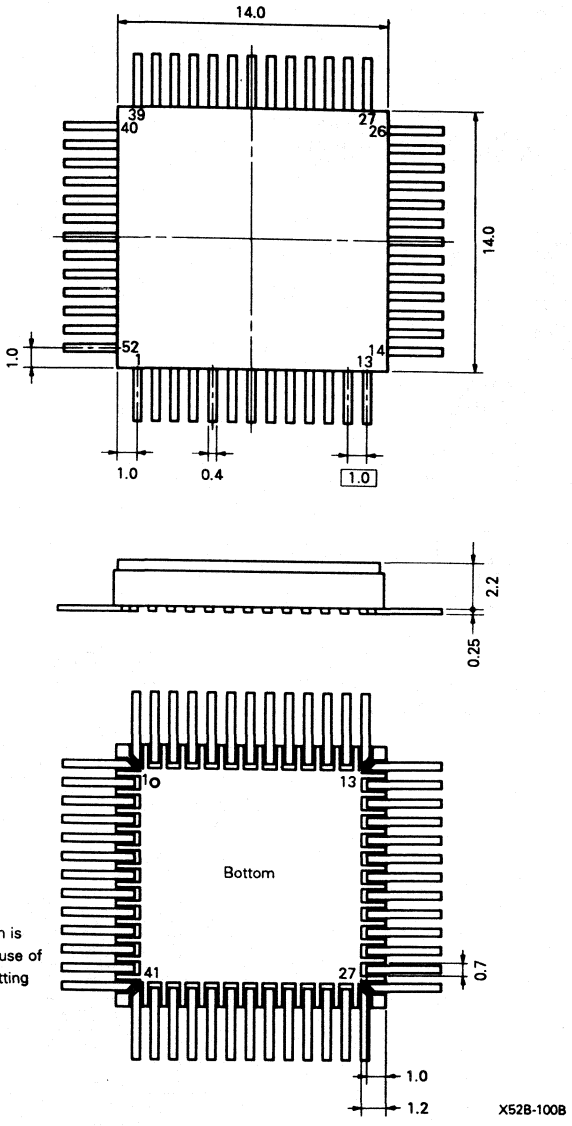
S52GC-100-3BH

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{-0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-pin ceramic QFP (14 sq.) (for ES) (unit: mm)



Note The lead length is not rated because of the lead tip cutting process.

4-BIT SINGLE-CHIP MICROCONTROLLER WITH 8K-BIT STATIC RAM AND 3-CHANNEL TIMER FOR INFRARED REMOTE CONTROLLER

The μPD17204 is a 4-bit single-chip microcontroller for infrared remote controller. Integrated on the same die are an 8K-bit static RAM (XRAM), a 3-channel timer, a carrier generating circuit for remote controller, an amplifier for the remote control receive signal, and a waveform shaping circuit.

Employing 17K architecture, the μPD17204 can execute transfer or arithmetic operation with a single instruction between data memory addresses and between the data memory and a peripheral circuit.

Each instruction consists of 16 bits (that is, one word). The μPD17204 is housed in a 52-pin plastic QFP.

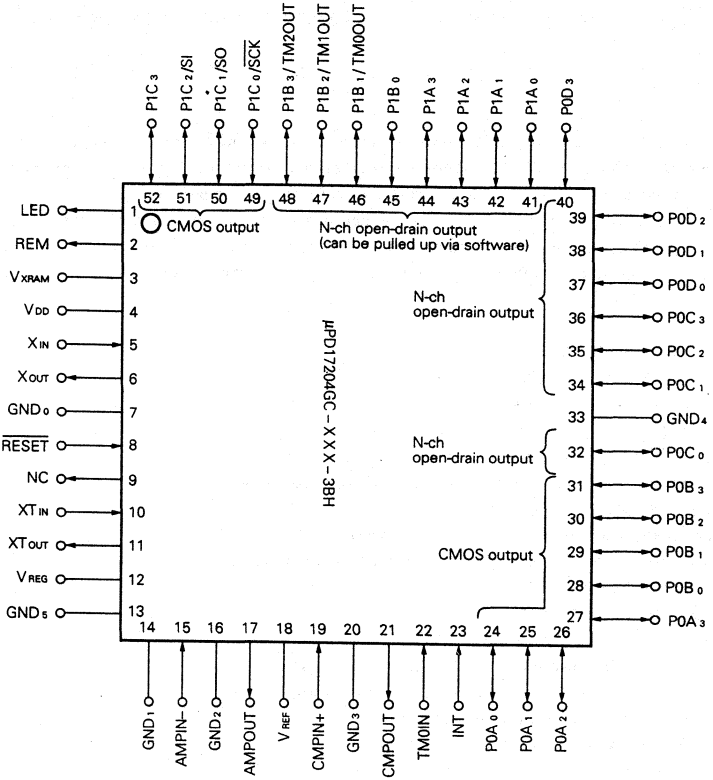
FEATURES

- Program memory (ROM): 7936 × 16 bits
- Data memory (RAM): 336 × 4 bits
- Static RAM (XRAM): 2048 × 4 bits
- Carrier generating circuit for infrared remote control
- Internal amplifier for infrared remote control receive signal
- Waveform shaping circuit for infrared remote control receive signal
- Abundant I/O ports (28)
- Three-line serial interface (also used as an I/O port)
- Instruction execution time: 4 μs (4 MHz ceramic oscillator is used)
- Standby function (STOP, HALT)
- Operating voltage range: 2.2 to 5.5 V (at 4 MHz)
  2.0 to 5.5 V (at 32 kHz)
- Operating clock: 4 MHz ceramic/32.768 kHz crystal oscillator
- Stack level: 7 levels (up to 2 levels for multiple interrupts)
- 8-bit timer: One channel (with modulo function)
- 10-bit timer: One channel (with modulo function)
- 16-bit timer: One channel
- Clock timer: One channel (for watchdog timer and clock)

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17204GC-xxx-3BH	52-pin plastic QFP (14 × 14 mm)	Standard

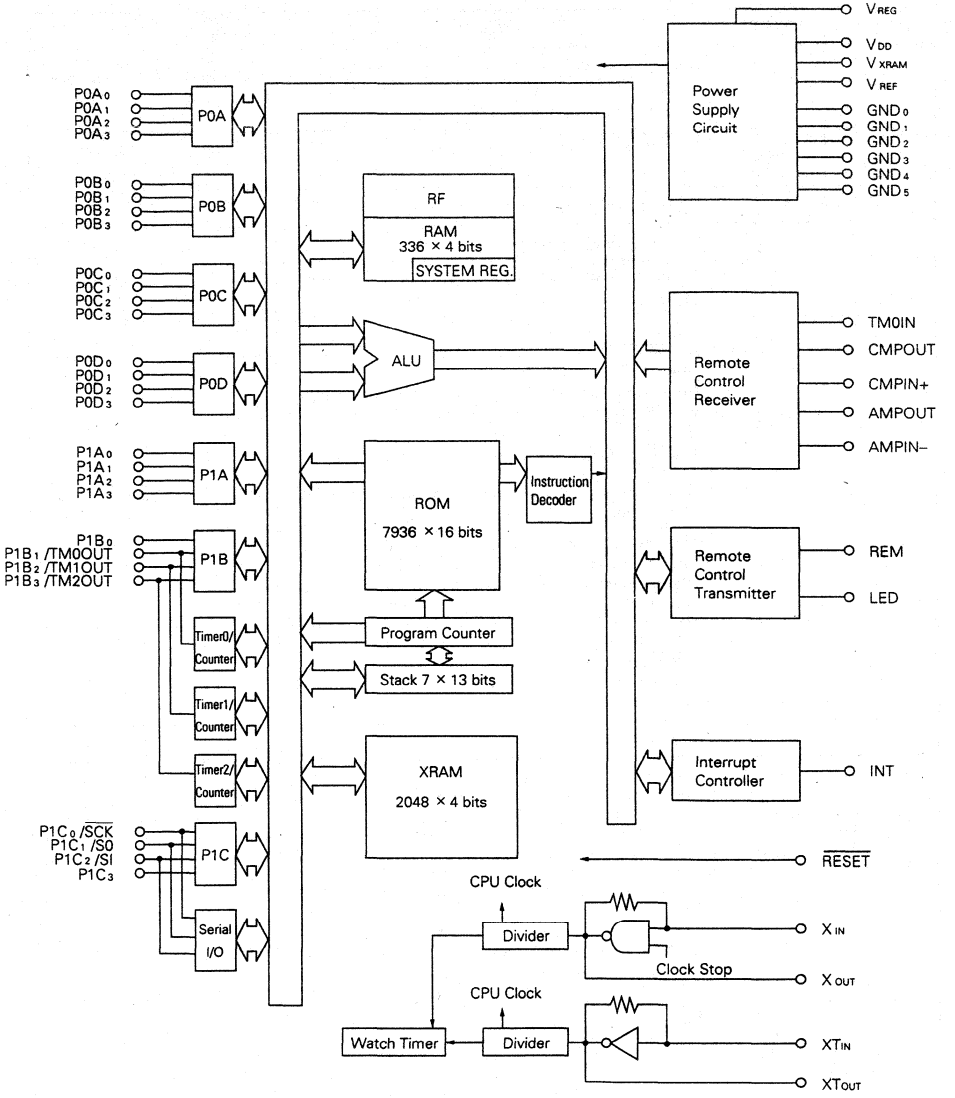
PIN CONFIGURATION (Top View)



LED	:	Indication of remote control transmission output
REM	:	Remote control transmission output
X_{IN}, X_{OUT}	:	Main clock oscillation
$\overline{RESET}$	:	Reset input
XT_{IN}, XT_{OUT}	:	Sub-clock oscillation
V_{REC}	:	Voltage regulator output
AMPIN–	:	Operational amplifier input
AMPOUT	:	Operational amplifier output
V_{REF}	:	Reference voltage output
CMPIN+	:	Comparator input
CMPOUT	:	Comparator output
INT	:	External interrupt input
TM0OUT	:	Timer 0 output
TM1OUT	:	Timer 1 output
TM2OUT	:	Timer 2 output

$\overline{SCK}$	:	Serial clock input/output
SO	:	Serial data output
SI	:	Serial data input
$P0A_0$ to $P0A_3$	:	Port 0A
$P03_0$ to $P0B_3$	:	Port 0B
$P0C_0$ to $P0C_3$	:	Port 0C
$P0D_0$ to $P0D_3$	:	Port 0D
$P1A_0$ to $P1A_3$	:	Port 1A
$P1B_0$ to $P1B_3$	:	Port 1B
$P1C_0$ to $P1C_3$	:	Port 1C
V_{DD}	:	Power supply
V_{XRAM}	:	XRAM power supply
GND	:	Ground
NC	:	Non-connection

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 PIN IDENTIFICATION

PIN No.	SYMBOL	FUNCTION	OUTPUT FORMAT	AT RESET
1	LED	Output NRZ signal in synchronization with the infrared remote control signal. Goes low when the remote control carrier is output.	CMOS push-pull	High-level output
2	REM	Outputs an infrared remote control signal. (active-high)	CMOS push-pull	Low-level output
3	V_{XRAM}	XRAM power supply.	—	—
4	V_{DD}	Positive power supply.	—	—
5 6	X_{IN} X_{OUT}	Connect a 4 MHz ceramic oscillator for main clock oscillation.	—	(Oscillation stop)
7	GND_0	Ground.	—	—
8	$\overline{RESET}$	Input pin for system reset. The system is reset when a low-level signal is input. Main clock oscillation is halted during low-level input. A pull-up resistor can be provided by the mask option.	—	—
9	NC	Non-connection.	—	—
10 11	XT_{IN} XT_{OUT}	Connect a 32 kHz crystal oscillator for subclock. When an option that does not use the subclock is selected, the divided output of the main clock is used as a timer clock.	—	—
12	V_{REG}	Output pin of voltage regulator for subclock oscillation circuit. To use this pin, an external 0.1 μF capacitor must be connected	—	—
13	GND_5	Ground	—	—
14	GND_1	Operational amplifier ground.	—	—
15	AMPIN −	Inverted input of operational amplifier.	—	Input
16	GND_2	Operational amplifier ground.	—	—
17	AMPOUT	Output pin for operational amplifier.	—	Output
18	V_{REF}	Outputs reference voltage. (1/2 V_{DD}). To use this pin, an external 0.1 μF capacitor must be connected.	—	—
19	CMPIN+	Non-inverted input pin for comparator. The comparator output is obtained by CMPOUT.	—	Input
20	GND_3	Operational amplifier ground.	—	—
21	CMPOUT	Output pin for comparator. To use a learning remote controller, CMPOUT and TM0IN must be externally connected.	—	Output

Note GND_1 to GND_3 are operational amplifier grounds.

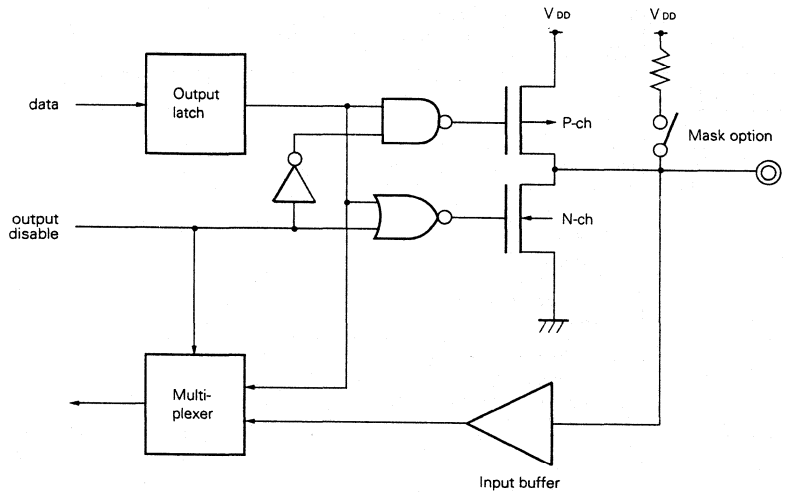
To stabilize the operation of these amplifiers, they must be made equipotential.

PIN No.	SYMBOL	FUNCTION	OUTPUT FORMAT	AT RESET
22	TM0IN	Clock input to timer 0. After it has been sampled by the internal clock, the input clock is supplied to timer 0 and, at the same time, to the envelope signal generation circuit. The frequency of the clock input to TM0IN can be measured by operating this timer in conjunction with timer 1.	—	Input
23	INT	Inputs external internal signal.	—	Input
24 to 27	$P0A_0$ to $P0A_3$	4-bit I/O port. Input/output can be set in 4-bit units. Pull-up resistors can be connected by mask option. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
28 to 31	$P0B_0$ to $P0B_3$	4-bit I/O port. Input/output can be set in 4-bit units. Pull-up resistors can be connected by mask option. The standby mode is released when at least one pin of this port goes low.	CMOS push-pull	Input
32 34 to 36	$P0C_0$ $P0C_1$ to $P0C_3$	4-bit I/O port. Input/output can be set in 4-bit units. The standby modes is released when at least one pin of this port goes high.	N-ch open-drain	Input
33	GND_4	Ground.	—	—
37 to 40	$P0D_0$ to $P0D_3$	4-bit I/O port. Input/output can be set in 4-bit units. The standby modes is released when at least one pin of this port goes high.	N-ch open-drain	Input
41 to 44	$P1A_0$ to $P1A_3$	4-bit I/O port. Input/output can be set in bit units. Pull-up resistors can be connected by program.	N-ch open-drain	Input
45 46 47 48	$P1B_0$ $P1B_1$/ TM0OUT $P1B_2$/ TM1OUT $P1B_3$/ TM2OUT	Port 1B and timer output. ● $P1B_0$ to $P1B_3$ • 4-bit I/O port • Input/output can be set in bit units. • Pull-up resistors can be connected by the program. ● TM0OUT to TM2OUT • Timer outputs	N-ch open-drain	Input ($P1B_0$ to $P1B_3$)
49 50 51 52	$P1C_0$/$\overline{SCK}$ $P1C_1$/SO $P1C_2$ /SI $P1C_3$	Port 1C and input/output for serial interface ● $P1C_0$ to $P1C_3$ • 4-bit I/O port • Input/output can be set in bit units. ● $\overline{SCK}$, SO, SI • $\overline{SCK}$: Serial clock input/output • SO : Serial data output • SI : Serial data input	CMOS push-pull	Input ($P1C_0$ to $P1C_3$)

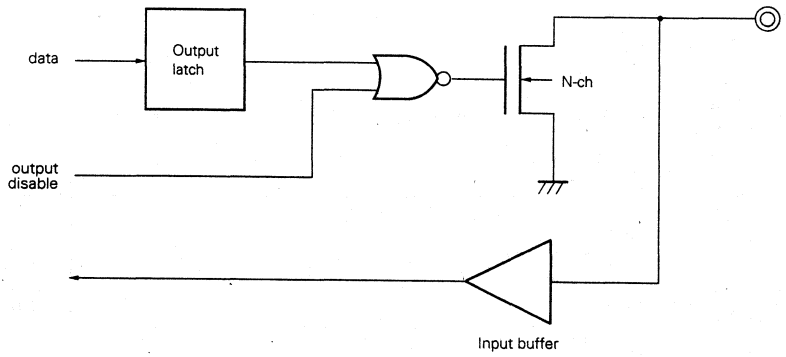
1.2 PIN INPUT/OUTPUT CIRCUITS

This section shows simplified diagrams illustrating the input/output circuits of the μPD17204 pins.

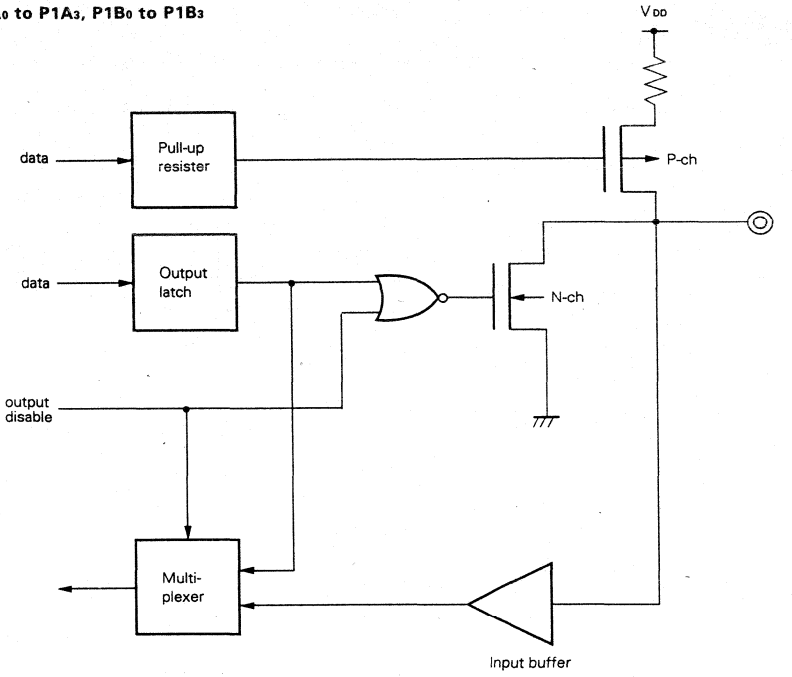
(1) $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$



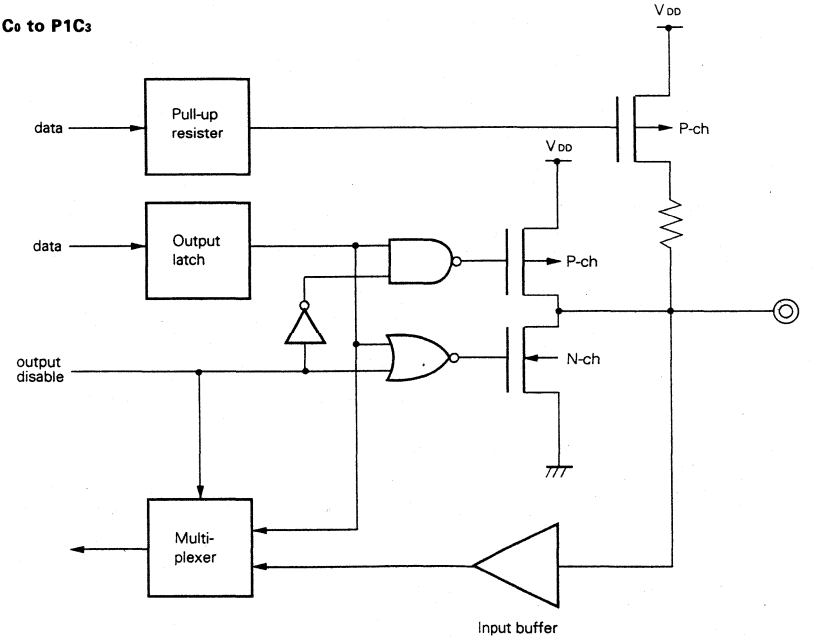
(2) $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$



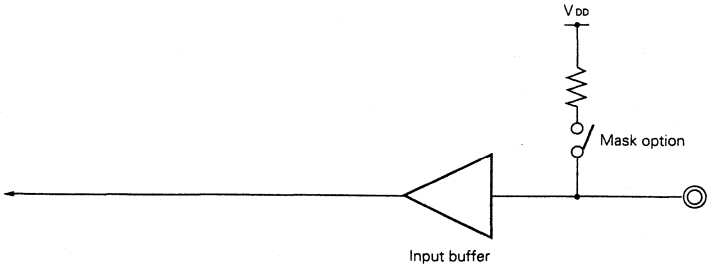
(3) $P1A_0$ to $P1A_3$, $P1B_0$ to $P1B_3$



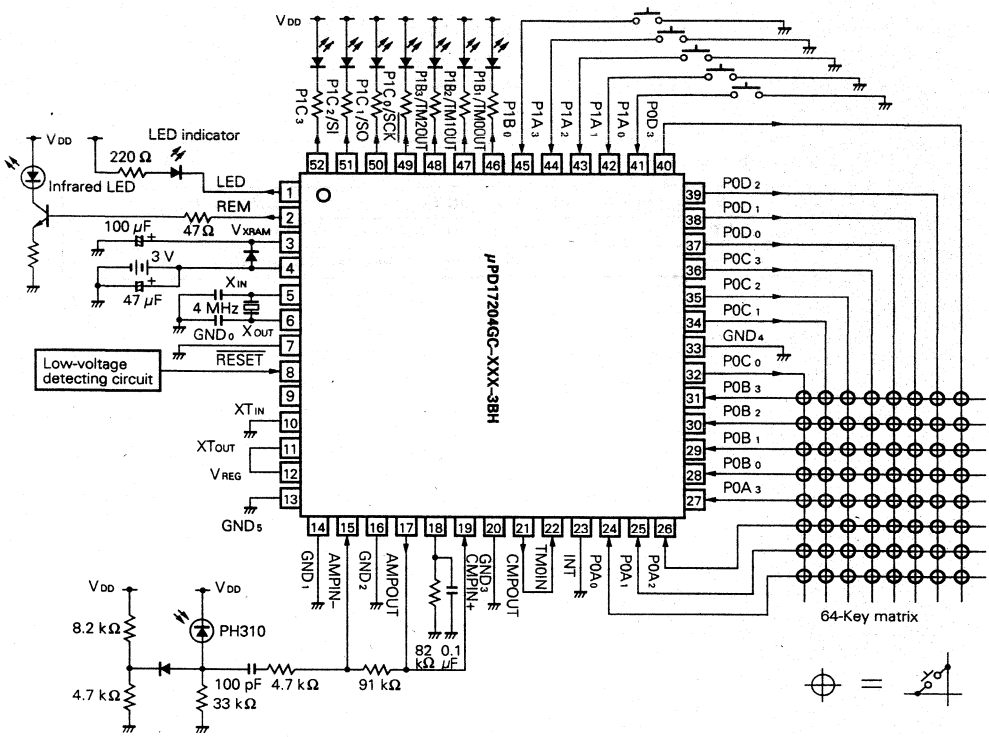
(4) $P1C_0$ to $P1C_3$



(5) $\overline{\text{RESET}}$



20. APPLICATION CIRCUIT EXAMPLE



The application circuit and circuit constants in this material are illustrative. They are not applicable to full production design.

21. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

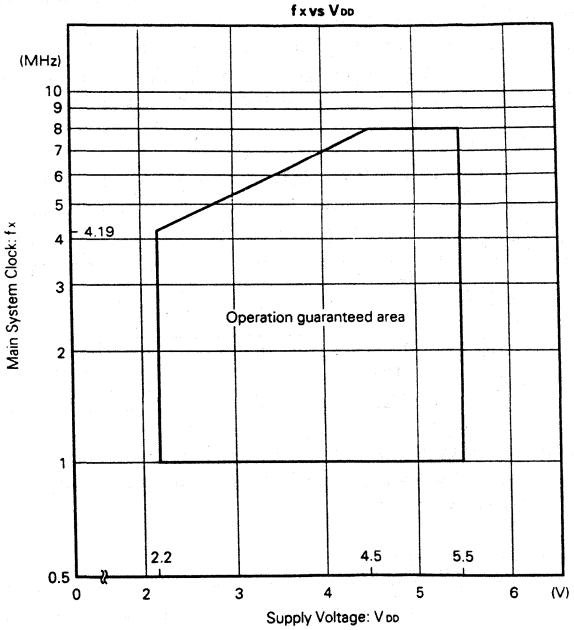
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

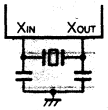
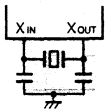
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}			10	pF	INT and $\overline{\text{RESET}}$ pins
	C_{PIN}			10	pF	Other than INT and $\overline{\text{RESET}}$ pins

RECOMMENDED OPERATING RANGES

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+30°C
	V_{DD2}	2.7	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+55°C
	V_{DD3}	2.9	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+75°C
	V_{DD4}	4.75	5.0	5.5	V	System clock: f_X = 6 MHz, Ta = -20...+50°C
	V_{DD5}	2.0	3.0	5.5	V	System clock: f_X = 32 kHz, Ta = -20...+75°C
Main Clock Oscillation Frequency	f_X	1.0	4.19	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	



MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to + 75 °C, V_{DD} = 2.2 to 5.5 V)

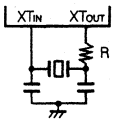
RESONATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic Oscillator Note 3		Oscillation frequency (f_x) Note 1		1.0	4.0	8.0	MHz
		Oscillation stabilization time Note 2	From when V_{DD} reaches the minimum oscillation voltage			4	ms
Crystal Oscillator Note 3		Oscillation frequency (f_x) Note 1		1.0	4.0	8.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms

Note 1 The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2 The oscillation stabilization time is the time required for stabilizing the oscillation after V_{DD} is applied or the STOP mode is released .

3 The recommended oscillators are shown in the table described later.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_a = −20 to + 75 °C, V_{DD} = 2.2 to 5.5 V)

RESONATOR	RECOMMENDED CONSTANTS	ITEM	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal Oscillator		Oscillation frequency (f_{XT})			32.768		kHz
		Oscillation stabilization time				10	s

Note: When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the fol lowing notations must be read and observed for wiring within the shaded area in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line .**
- **Capacitors used in the oscillators must always be grounded to Vss potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

RECOMMENDED OSCILLATORS

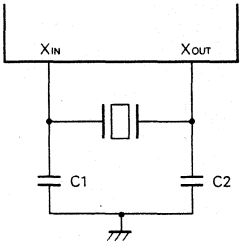
MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
		C1	C2	MIN.	MAX.	
Murata Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	none	none	2.0	6.0	C contained type
	CST4.00MGW	none	none	2.0	6.0	
	CST4.19MGW	none	none	2.0	6.0	
Kyocera	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
Toko	CRHF4.00	18	18	2.0	6.0	
Dai-Shinku	PRS0400BCSAN	39	33	2.0	6.0	

MAIN SYSTEM CLOCK: CRYSTAL OSCILLATOR

MANUFACTURER	FREQUENCY (MHz)	RETAINER	EXTERNAL CAPACITOR (pF)		OSCILLATION VOLTAGE (V)		REMARKS
			C1	C2	MIN	MAX.	
Kinseki	4.0	HC-49U-S	22	22	2.0	6.0	

Oscillator Circuit



DC CHARACTERISTICS (V_{DD} = 3 V, Ta = −20 to +75 °C, f_X = 4 MHz, (f_{XT} = 32 kHz)

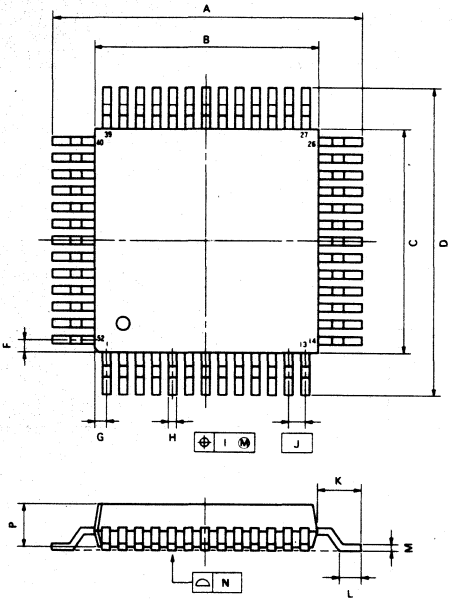
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V_{IH1}	2.4		3.0	V	$\overline{RESET}$ and INT pins	
	V_{IH2}	2.1		3.0	V	Other than $\overline{RESET}$ and INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.6	V	$\overline{RESET}$ and INT pins	
	V_{IL2}	0		0.9	V	Other than $\overline{RESET}$ and INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	V_{IH} = 3.0 V
	I_{IH2}			0.2	μA	TM0IN	V_{IH} = 3.0 V
	I_{IH3}			0.2	μA	$\overline{RESET}$	V_{IH} = 3.0 V
	I_{IH4}			0.2	μA	P0A to P0D	V_{IH} = 3.0 V
	I_{IH5}			0.2	μA	P1A to P1C	V_{IH} = 3.0 V
Low-Level Input current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			0.2	μA	$\overline{RESET}$	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL4}	30	60	120	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
	I_{IL5}			0.2	μA	P0A, P0B	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL6}	8	15	30	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
	I_{IL7}			0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL5}			0.2	μA	P1A-P1C	V_{IL} = 0 V (pull-up resistor is not incorporated)
	I_{IL6}	30	60	120	μA		V_{IL} = 0 V (pull-up resistor is incorporated)
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	V_{OH} = 2.7 V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	V_{OH} = 2.7 V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	V_{OH} = 1.0 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	V_{OH} = 2.7 V
	I_{OH5}	−0.3	−1.0	−2.0	mA	CMPOUT	V_{OH} = 2.7 V
Low-Level Output current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B, P1C	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D, P1A, P1B	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V
Output Voltage	V_{REF}	1.3	1.5	1.7	V	V_{REF} pin external capacity = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	Both XT and X oscillate.
	I_{DD2}		15	30	μA		Only XT oscillates.
	I_{DD3}			2.0	mA	HALT mode	Both XT and X oscillates.
	I_{DD4}		10	15	μA		Only XT oscillates.
XRAM Holding Voltage	V_{XRAM}	1.3	3.0	5.5	V		
XRAM Supply Current	I_{XRAM1}		3.0		μA	Operation mode, V_{XRAM} = 3 V	
	I_{XRAM2}		0.2	1.0	μA	HALT mode, V_{XRAM} = 3 V, Ta = 25 °C	

OPERATIONAL AMPLIFIER/COMPARATOR CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Unity Gain Frequency of Operational Amplifier		0.5	1.0	10	MHz	
Input Offset Voltage of Operational Amplifier			10		mV	
Same Phase Input Voltage Range of Operational Amplifier		0.3		2.7	V	
Output Voltage Range of Operational Amplifier		0.1		2.9	V	
Operational Amplifier Through Rate		1			V/μs	
Input Offset Voltage of Comparator		40	60	80	mV	
Same Phase Input Voltage Range of Comparator		0		3.0	V	
Minimum Output Pulse Width of Comparator		3	4	5	μs	
Comparator Through Rate		10			V/μs	

22. PACKAGE DIMENSIONS

52PIN PLASTIC QFP (□14)



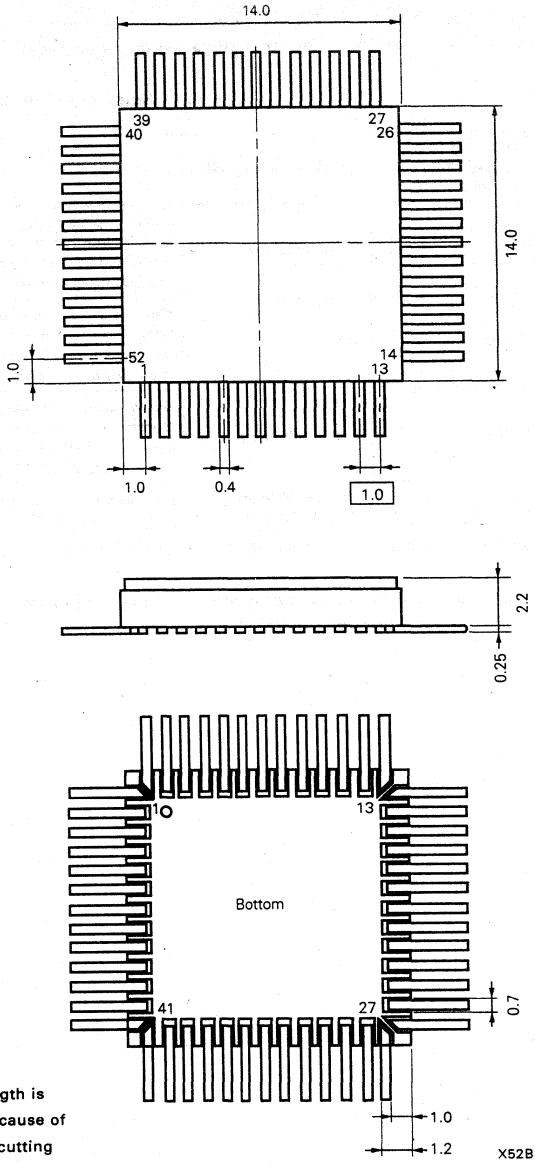
S52GC-100-3BH

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

52-pin ceramic QFP (14 sq.) (for ES) (unit: mm)



Note The lead length is not rated because of the lead tip cutting process

23. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD17204 by soldering, soldering should be performed under the following recommended conditions. For other soldering methods, please consult with NEC sales personnel.

Table 23-1 Soldering Conditions

Recommended conditions reference code	Soldering method	Soldering conditions
IR30-162	Infrared reflow	Package peak temperature: 230 °C, Time: 30 seconds max. (210 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
VP15-162	VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C)
WS60-162	Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max. Number of soldering operations: 1, Maximum number of days*: 2 days (beyond this period, 16 hours of pre-baking is required at 125 °C
Pin partial heating	Pin partial heating	Pin temperature: 300°C max., Timer: 10 seconds max .

*: Number of days after unpacking the dry pack. Storage conditions are 25 °C and 65 % RH max.

Note Do not use different soldering methods together (however, pin partial heating can be performed with other soldering methods).

APPENDIX A COMPARISON BETWEEN μUPD17203A AND μPD17204

Part number	μPD17203A	μPD17204
ROM	4096 × 16 bits	7936 × 16 bits
RAM	336 × 4 bits	
SRAM	4096 × 4 bits	2048 × 4 bits
Instruction execution time	4 μs (when 4 MHz ceramic oscillator is used)	
Stack level	5 levels (up to 2 levels for multiple interrupts)	7 levels (up to 2 levels for multiple interrupts)
Number of I/O ports	28	
Serial interface	8 bits (3-line: 1 channel)	
Interrupt	7 channels	
	External interrupt: 1 channel	
	Internal interrupt: 6 channels	
Timer	4 types	
	8-bit timer	
	10-bit timer	
	16-bit timer	
	Clock timer (also used as a watchdog timer)	
Standby function	STOP mode, HALT mode	
Recommended operating voltage range	V_{DD} = 2.2 to 5.5 V (at 4 MHz) V_{DD} = 2.0 to 5.5 V (at 32 kHz)	
Package	52-pin plastic QFP	

4-BIT SINGLE-CHIP MICROCONTROLLER WITH 8K-BIT STATIC RAM AND 3-CHANNEL TIMER FOR INFRATED REMOTE CONTROLLER

μPD17P204 is a variation of μPD17204 and is equipped with a one-time PROM instead of an internal mask ROM.

μPD17P204 is suitable for preproduction or small-scale production when developing a μPD17204 system because program can be written by the user.

When reading this document, also refer to the μPD17204 Data Sheet.

FEATURES

- Internal one-time PROM: 7936 × 16 bits
- Supply voltage: 2.2 to 5.5 V

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P204GC-001-3BH	52-pin plastic QFP	Standard
μPD17P204GC-002-3BH	52-pin plastic QFP	Standard
μPD17P204GC-003-3BH	52-pin plastic QFP	Standard

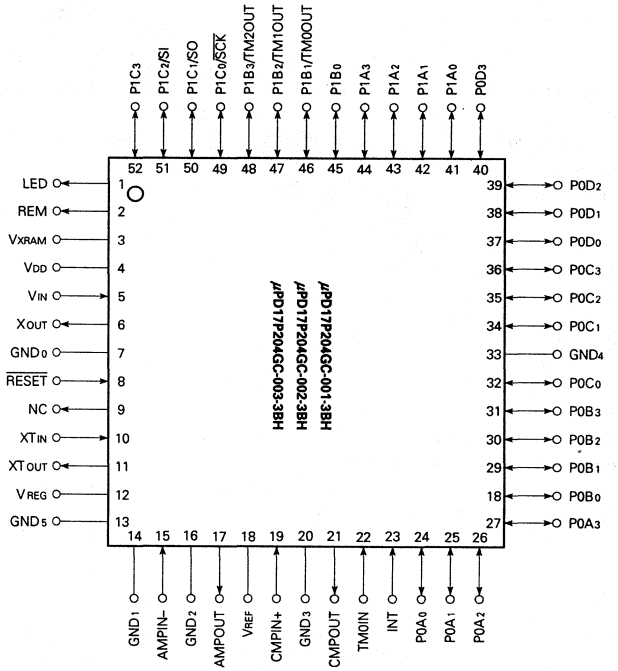
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The features of each product is shown in the following table:

Item	μPD17P204-001	μPD17P204-002	μPD17P204-003	μPD17204
Pull-up resistor of $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	On request (mask option)
Pull-up resistor of P0A and P0B pins		Provided		
Main clock oscillator circuit				
Subclock oscillator circuit		Not provided	Provided	

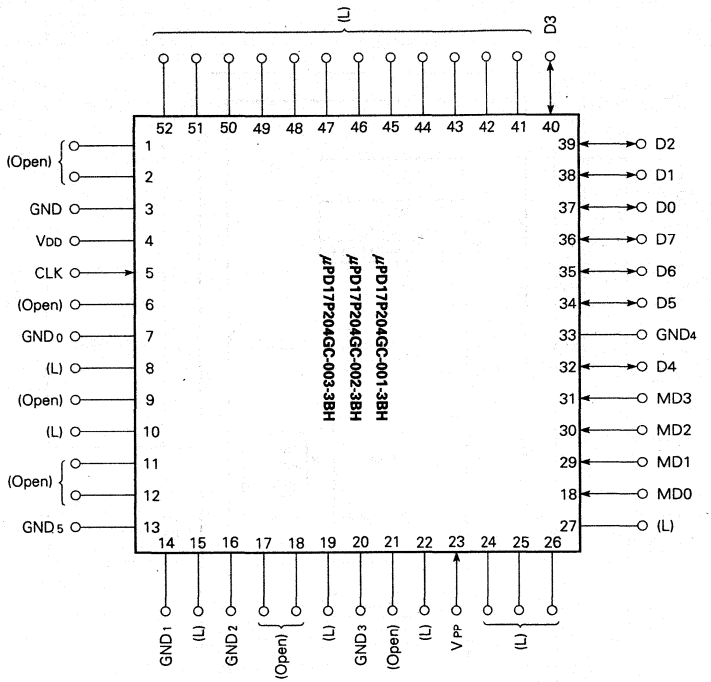
PIN CONFIGURATION (Top View)

(1) Normal operation mode



LED	: Remote control transmission output indication pin	$\overline{SCK}$	: Serial clock input/output pin
REM	: Remote control transmission output	SO	: Serial data output pin
XIN, XOUT	: Main clock resonator connection pins	SI	: Serial data input pin
$\overline{RESET}$	: Reset input pin	P0A0 - P0A3	: Port 0A
NC	: Non-connection pin	P0B0 - P0B3	: Port 0B
VTIN, XTOUT	: Subclock resonator connection pins	P0C0 - P0C3	: Port 0C
VREG	: Voltage regulator output pin	P0D0 - P0D3	: Port 0D
AMPIN–	: Operational amplifier input pin	P1A0 - P1A3	: Port 1A
AMPOUT	: Operational amplifier output pin	P1B0 - P1B3	: Port 1B
VREF	: Reference voltage output pin	P1C0 - P1C3	: Port 1C
CMPIN+	: Comparator input pin	CLK	: PROM clock input pin
CMPOUT	: Comparator output pin	MD0 - MD3	: PROM mode selection pin
TM0IN	: Timer 0 input pin	D0 - D7	: PROM data input/output pin
INT	: External interrupt input pin	VPP	: PROM power supply pin
TM0OUT	: Timer 0 output pin	VDD	: Power supply pin
TM1OUT	: Timer 1 output pin	VXRAM	: XRAM power supply pin
TM2OUT	: Timer 2 output pin	GND:	: Ground

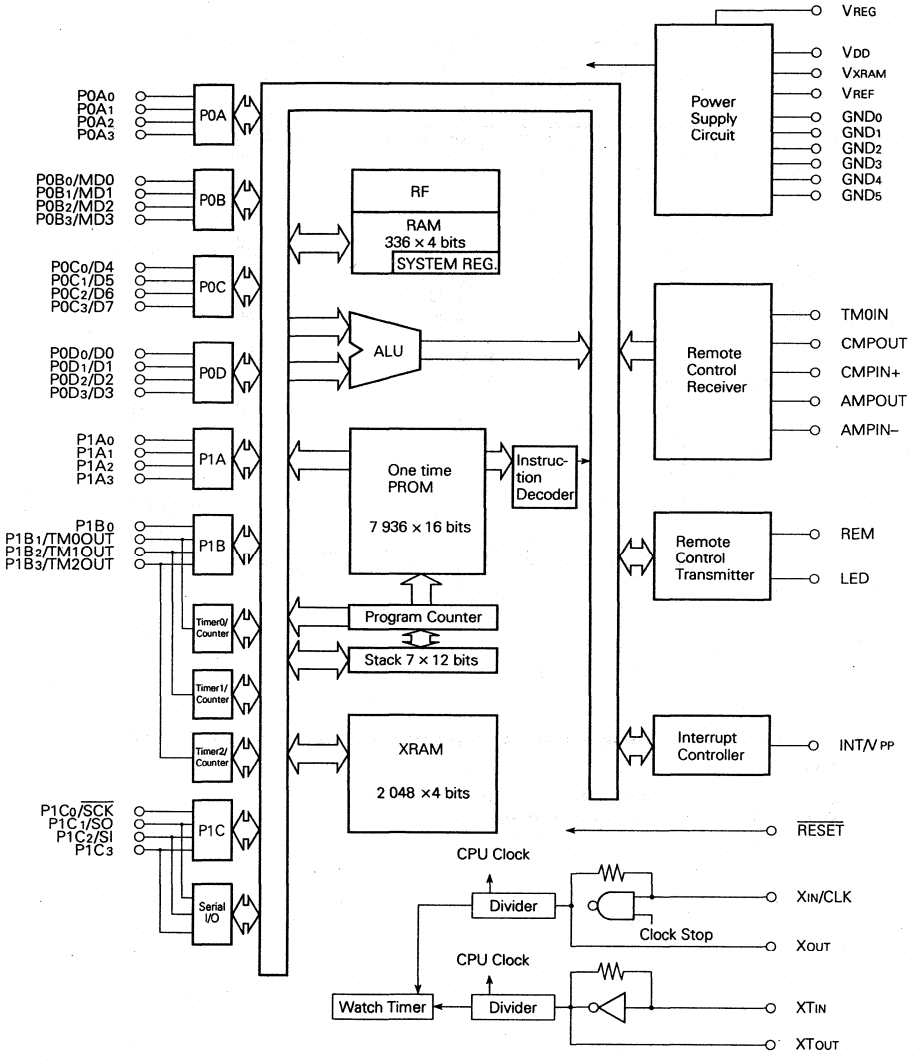
(2) PROM programming mode



Note **Those enclosed in parentheses indicate the processing of the pins not used in PROM programming mode.**

L : Ground these pins through a resistor (470 Ω).
Open : Do not connect anything to these pins.

BLOCK DIAGRAM



1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
0	LED	Outputs NRZ signal in synchronization with infrared remote controller signal. Remains low while remote control carrier is output.	CMOS push-pull	High-level output
2	REM	Outputs active-high infrared remote control signal.	CMOS push-pull	Low-level output
3	V_{XRAM}	Supplies power to XRAM.	—	—
4	V_{DD}	Positive power	—	—
5 6	X_{IN} X_{OUT}	Connect 4 MHz ceramic oscillator for main clock oscillation	—	(Oscillation stop)
7	GND_0	Ground	—	—
8	$\overline{RESET}$	Inputs low-active system reset signal. While this pin remains low level, oscillation of main clock stops. Pull-up resistor can also be connected by mask option.	—	—
9	NC	No connection	—	—
10 11	XT_{IN} XT_{OUT}	Connect 32 kHz crystal oscillator across these pins. When option not using subclock is selected, main clock is divided and is supplied to watch timer.	—	—
12	V_{REG}	Outputs signal from voltage regulator for subclock oscillator circuit. Connect external 0.1 μF capacitor.	—	—
13	GND_5	Ground	—	—
14	GND_1	Ground for operation amplifier	—	—
15	AMPIN–	Inverted input of operational amplifier	—	Input
16	GND_2	Ground of operational amplifier	—	—
17	AMPOUT	Output of operational amplifier	—	Output
18	V_{REF}	Outputs reference voltage of 1/2V_{DD}. Connect external 0.1 μF capacitor.	—	—
19	CMPIN+	Non-inverted input of comparator. Output of this comparator can be obtained from CMPOUT.	—	Input
20	GND_3	Ground of operational amplifier	—	—
21	CMPOUT	Comparator output. Externally connect CMPOUT and TM0IN when using micro-controller as teaching remote controller	—	Output

Remarks GND_1 - GND_3 are the ground pins of the operational amplifier. Keep all these pins at the same potential to stabilize the operation of the operational amplifier.

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
22	TM0IN	Clock input to timer 0. Input clock is sampled by internal clock and then input to envelope signal generator circuit, as well as to timer 0. By using timer 0 with timer 1, frequency of clock input to this pin can be measured.	—	Input
23	INT	External interrupt signal input pin	—	Input
24 to 27	$P0A_0$ to $P0A_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units. Pull-up resistor can be connected by mask option. When one or more of these pins goes low in standby mode, standby mode is released.	CMOS push-pull	Input
28 to 31	$P0B_0$ to $P0B_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units. Pull-up resistor can be connected by mask option. When one or more of these pins goes low in standby mode, standby mode is released.	CMOS push-pull	Input
32 34 to 36	$P0C_0$ $P0C_1$ to $P0C_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units. When one or more of these pins goes low in standby mode, standby mode is released.	N-ch open drain	Input
33	GND_4	Ground	—	—
37 to 40	$P0D_0$ to $P0D_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units. When one or more of these pins goes low in standby mode, standby mode is released.	N-ch open drain	Input
41 to 44	$P1A_0$ to $P1A_3$	Constitute 4-bit I/O port, which can be set in input or output mode in bitwise. Pull-up registor can be connected through program.	N-ch open drain	Input
45 46 47 48	$P1B_0$ $P1B_1$/TM0OUT $P1B_2$/TM1OUT $P1B_3$/TM2OUT	Port 1B or timer output • $P1B_0$ - $P1B_3$ · 4-bit I/O port · Can be set in input/output mode in bitwise · Pull-up resistor can be connected through program • TM0OUT - TM2OUT · Timer output	N-ch open drain	Input ($P1B_0$ - $P1B_3$)
49 50 51 52	$P1C_0$/$\overline{SCK}$ $P1C_1$/SO $P1C_2$/SI $P1C_3$	Port 1C or serial interface I/O • $P1C_0$ - $P1C_3$ · 4-bit I/O port · Can be set in input/output mode in bitwise • $\overline{SCK}$, SO, SI · $\overline{SCK}$: serial clock I/O · SO : serial clock data output · SI : serial clock data input	CMOS push-pull	Input ($P1C_0$ - $P1C_3$)

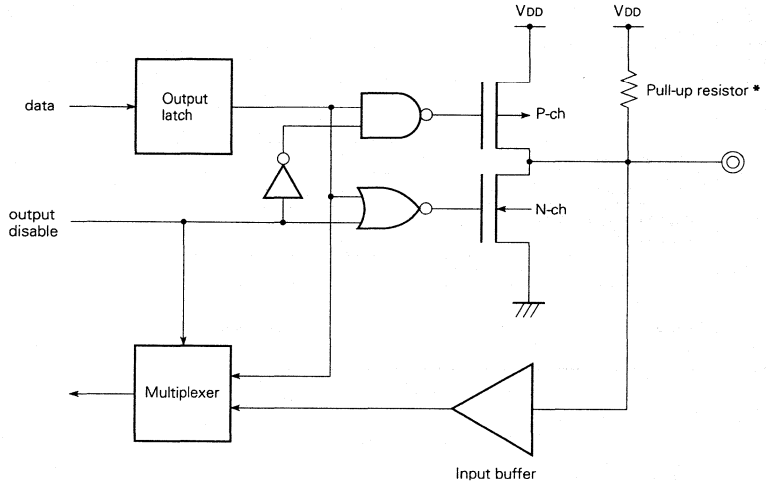
1.2 PROM PROGRAMMING MODE

PIN No.	SYMBOL	FUNCTION	OUTPUT TYPE	AT RESET
3 7 13 14 16 20 33	GND GND_0 GND_5 GND_1 GND_2 GND_3 GND_4	Ground	—	—
4	V_{DD}	Positive power	—	—
5	CLK	Address updating clock input	—	Input
23	V_{PP}	Supplies program voltage. Apply 12.5 V to this pin.	—	—
28 to 31	MD0 - MD3	Selects PROM programming mode		Input
32 34 to 36	D4 - D7	8-bit data I/O	CMOS push-pull	Input
37 to 40	D0 - D3			

1.3 PIN EQUIVALENT CIRCUITS

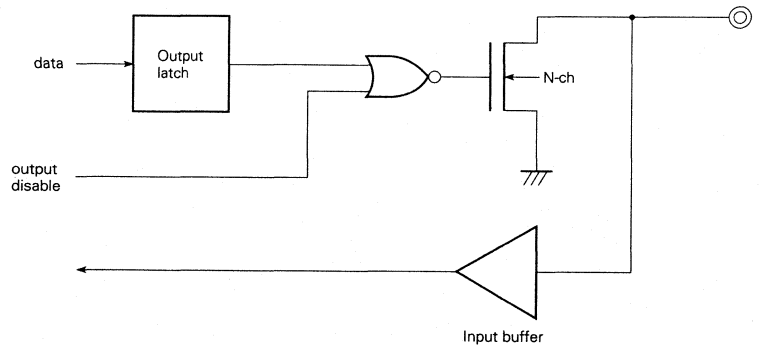
This section shows the equivalent circuits of the μPD17P204 pins in simplified schematic diagrams.

(1) $P0A_0$ - $P0A_3$, $P0B_0$/MD0 - $P0B_3$/MD3

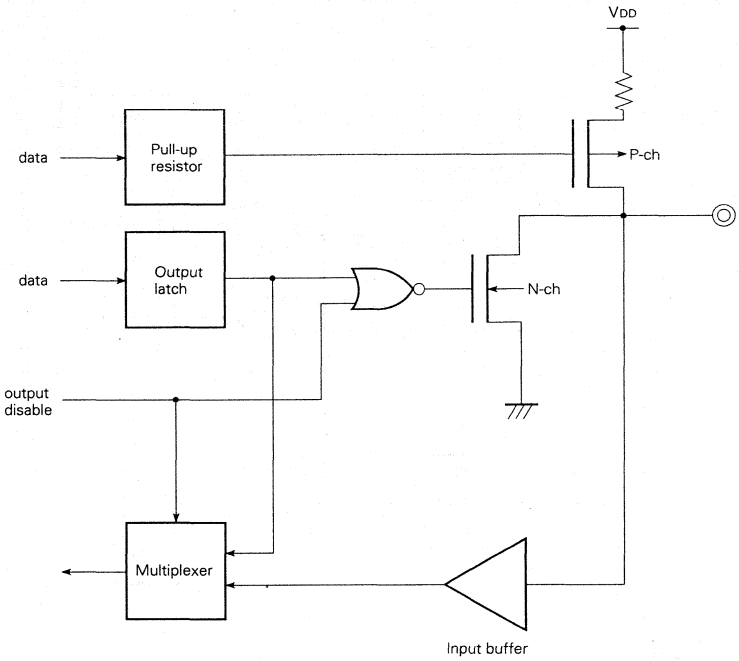


* μPD17P204-001, - 002 only

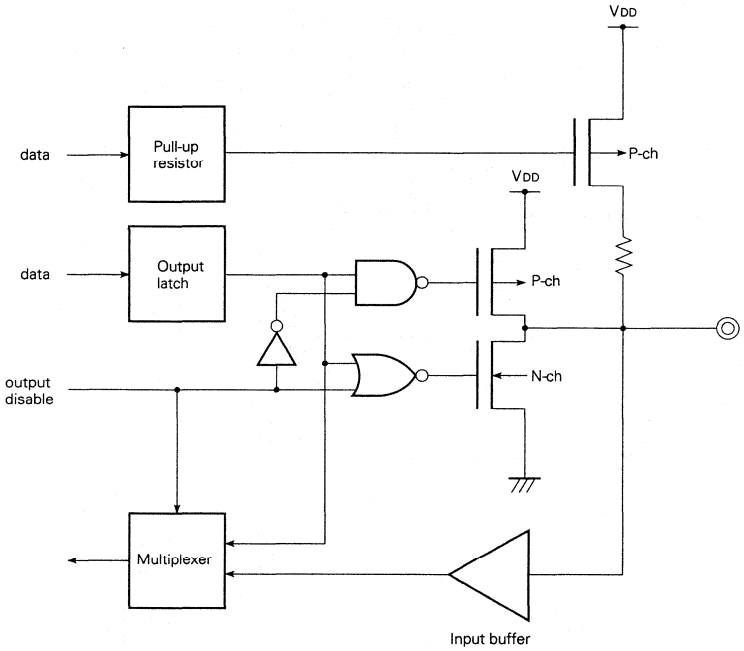
(2) $P0C_0$/D4 - $P0C_3$/D7, $P0D_0$/D0 - $P0D_3$/D3



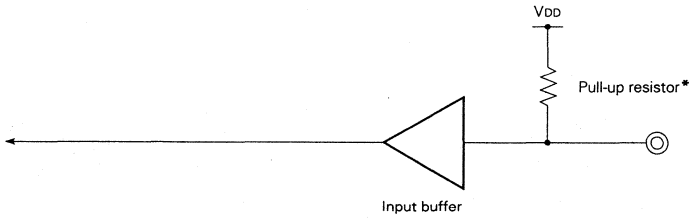
(3) $P1A_0$ - $P1A_3$, $P1B_0$ - P_1B_3/TM2OUT



(4) P1C0/$\overline{SCK}$ - P1C3



(5) $\overline{RESET}$



* μPD17P204-001 only

2. DIFFERENCES BETWEEN μPD17P204 AND μPD17204

The μPD17P204 and μPD17204 are identical in the CPU functions and internal hardware peripherals in that the μPD17P204 is provided with a PROM, which can be written by the user, in the place of the mask ROM of the μPD17204. The only differences between the two microcontrollers are therefore the program memory and mask option.

For the CPU functions and internal hardware peripherals of the μPD17P204, therefore, refer to the Data Sheet of the μPD17204.

Item \ Product	μPD17P204-001	μPD17P204-002	μPD17P204-003	μPD17204
Program memory	· PROM · 0000H - 1EFFH · 2048 × 16 bits			· Mask ROM · 0000H - 1EFFH · 2048 × 16 bits
Pull-up resistor of $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	On request (mask option)
Pull-up resistor of P0A and P0B pins		Provided		
Main clock oscillator circuit				
Subclock oscillator circuit		Not provided	Provided	
Pin configuration	V_{PP} and PROM program pins provided			V_{PP} and PROM program pins not provided
Operating voltage range	V_{DD} = 2.2 to 5.5 V(at 4 MHz), V_{DD} = 2.0 to 5.5 V (at 32 kHz)			
Package	52-pin plastic QFP			

3 ONE-TIME PROM (PROGRAM MEMORY) WRITING, READING, AND VERIFICATION

μPD17P204 provides the program memory of 7936 × 16 bits one-time PROM.

The following table lists the pins to be used for this PROM writing, reading or verification.

In PROM mode, no address input pin is used. Instead, the address is updated by the clock for input from the CLK pin.

Pin name	Function
V_{PP}	Applies program voltage.
CLK	Inputs address update clock.
MD0 - MD3	Selects operation mode.
D0 - D7	Input and output 8-bit data.

3.1 OPERATION MODE FOR WRITING, READING, AND VERIFICATION OF PROGRAM MEMORY

If +6 V is applied to the V_{DD} and +12.5 V to the V_{PP} pin after μPD17P204 has been placed in the reset status for a fixed time (V_{DD} = 5 V, $\overline{RESET}$ = 0 V), μPD17P204 enters program memory write, read, or verify mode.

The MD0 to MD3 pins are used to set the operation modes listed in the following table.

Leave the pins not used for program memory writing, reading, or verification open or ground through pull-down resistors.

Operating mode specification						Operating mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	x	H	H	Program inhibit mode

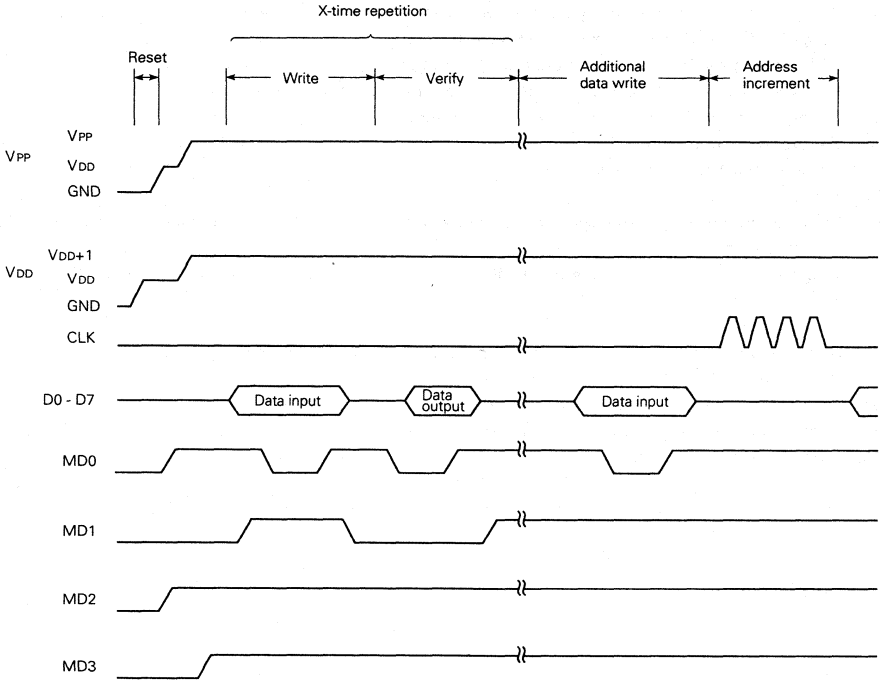
Note x: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 microseconds, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Write data in 1-millisecond write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (X) in steps (7) to (9)) times 1 milliseconds.
(11) Set program inhibit mode.
(12) Supply a pulse to the CLK pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power supply.

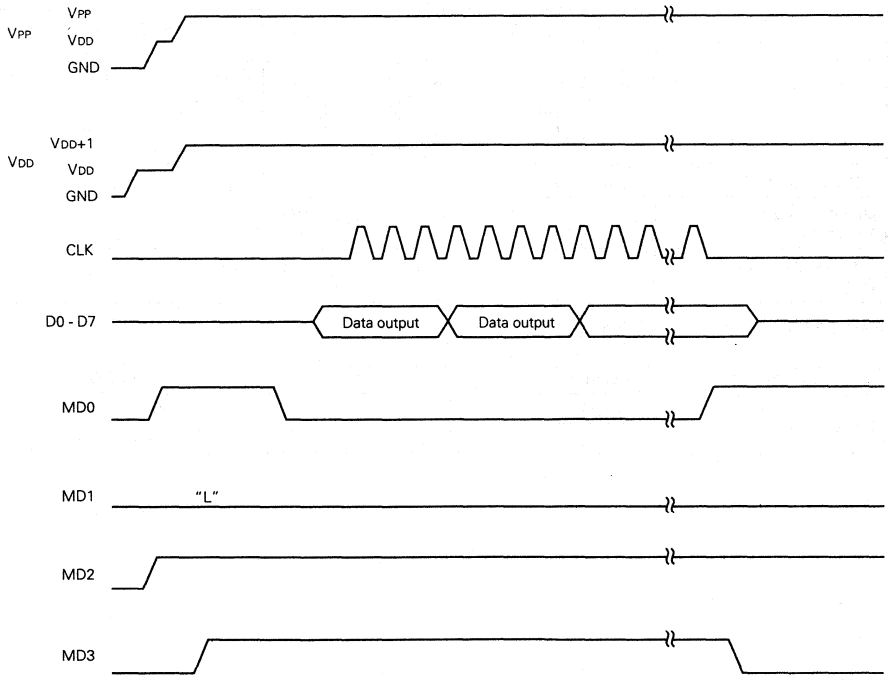
Steps (2) to (12) are illustrated below.



3.3 PROGRAM MEMORY READ PROCEDURE

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 microseconds, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the CLK pin four times.
(8) Set program inhibit mode.
(9) Set program memory address 0 clear mode.
(10) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.2	3.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+30°C
	V_{DD2}	2.7	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+55°C
	V_{DD3}	2.9	5.0	5.5	V	System clock: f_X = 4 MHz, Ta = -20...+75°C
	V_{DD4}	4.75	5.0	5.5	V	System clock: f_X = 6 MHz, Ta = -20...+50°C
	V_{DD5}	2.0	3.0	5.5	V	System clock: f_X = 32 kHz, Ta = -20...+75°C
XRAM Supply Voltage	V_{XRAM}	1.3		V_{DD}	V	$V_{XRAM} \leq V_{DD}$
Main Clock Oscillation Frequency	f_X	2.0	4.0	8.0	MHz	
Subclock Oscillation Frequency	f_{XT}		32.768		kHz	

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			10	pF	INT, $\overline{RESET}$ pins
	C_{PIN}			10	pF	Other than INT, $\overline{RESET}$ pins

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$, INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$, INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	TM0IN	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	$\overline{\text{RESET}}$	$V_{IH} = V_{DD}$
	I_{IH4}			0.2	μA	P0A - P0D	$V_{IH} = V_{DD}$
	I_{IH5}			0.2	μA	P1A - P1C	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			0.2	μA	$\overline{\text{RESET}}$	V_{IL} = 0 V, w/o pull-pn resistors
	I_{IL4}	30	60	120	μA		I_{IL} = 0 V, w/pull-up resistors
	I_{IL5}	8	15	30	μA	P0A, P0B	V_{IL} = 0 V, w/pull-up resistors
	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL7}			0.2	μA	P1A - P1C	V_{IL} = 0 V, w/o pull-up resistors
	I_{IL8}	30	60	120	μA		I_{IL} = 0 V, w/pull-up resistors
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	$V_{OH} = V_{DD}$ − 0.3 V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	$V_{OH} = V_{DD}$ − 0.3 V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	$V_{OH} = V_{DD}$ − 2 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	$V_{OH} = V_{DD}$ − 0.3 V
	I_{OH5}	−0.3	−1.0	−2.0	mA	CMPOUT	$V_{OH} = V_{DD}$ − 0.3 V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V
V_{REF} Output Voltage	V_{REF}	0.8	1.2	1.6	V	V_{REF} pin external capacitance = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	Generates both XT and X
	I_{DD2}		15	30	μA		Generates XT only
	I_{DD3}			2.0	mA	HALT mode	Generates both XT and X
	I_{DD4}		10	15	μA		Generates XT only
XRAM Holding Voltage	V_{XRAM}	1.3	3.0	5.5	V		
XRAM Supply Current	I_{XRAM1}		3.0		μA	Operation mode, V_{XRAM} = 3 V	
	I_{XRAM2}		0.2	1.0	μA	HALT mode, V_{XRAM} = 3 V, Ta = 25 °C	

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD} – 0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD} – 1.0			V	I_{OH} = –1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes 1. V_{PP} must not exceed +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP} and disconnect it after V_{PP}.

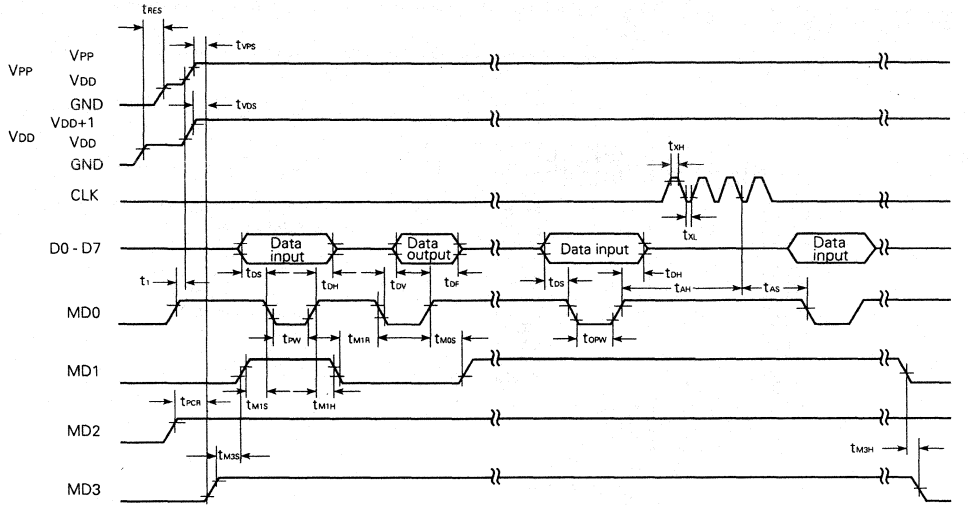
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time *2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	t_{M1H} + t_{M1R} ≧ 50 μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	—	10			μs	
CLK Input High-/Low-Level Width	t_{XH}, t_{XL}	—	0.063			μs	
CLK Input Frequency	f_X	—			8	MHz	
Initial Mode Set Time	t_I	—	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	—	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	—	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	—	2			μs	When data is read from program memory
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When data is read from program memory
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	When data is read from program memory
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	—	2			μs	When data is read from program memory
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	—	2			μs	When data is read from program memory
Reset Setup Time	t_{RES}		10			μs	

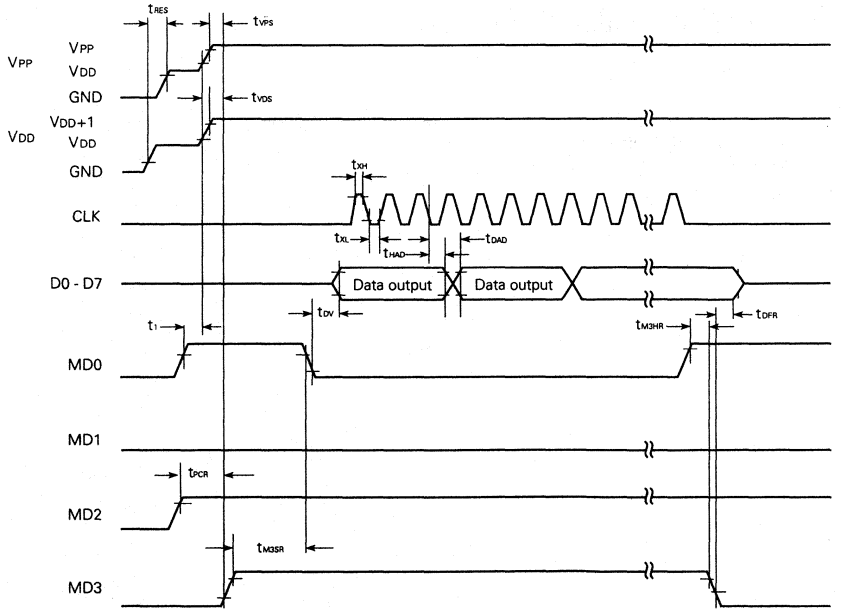
***1** These symbols are the corresponding μPD27C256 symbols.

***2** The internal address is incremented by 1 at the third falling edge of CLK (with four clocks constituting as one cycle). The internal address is not connected to any pin.

PROGRAM MEMORY WRITE TIMING

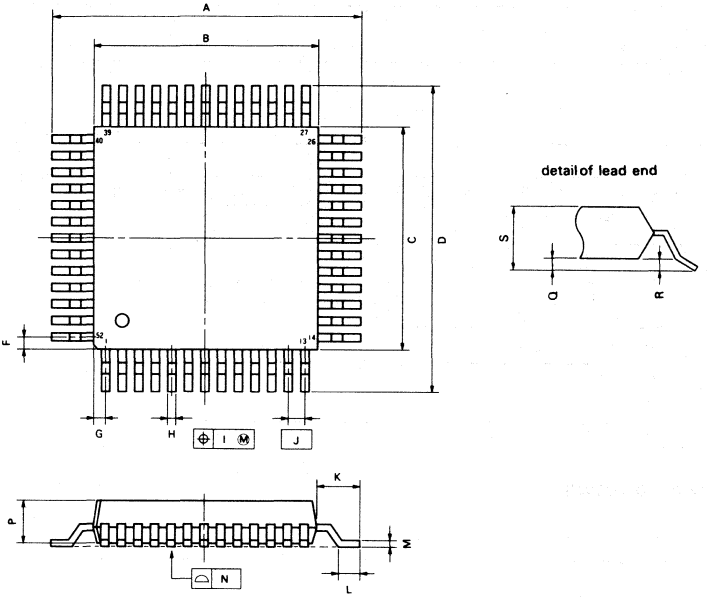


PROGRAM MEMORY READ TIMING



5. PACKAGE DIMENSION

52PIN PLASTIC QFP (□14)



S52GC-100-3BH

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

4-BIT SINGLE-CHIP MICROCONTROLLER FOR INFRARED REMOTE CONTROLLER

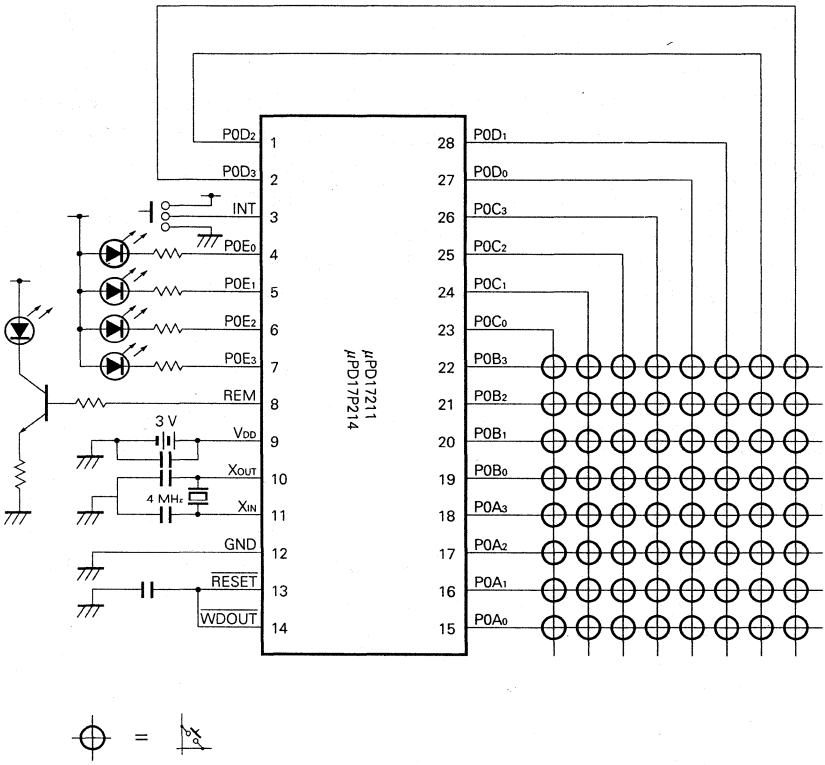
The μPD17211 is a 4-bit single-chip microcontroller for infrared remote controller. Its CPU employs the 17K architecture, and can directly manipulate the data memory, accomplish various arithmetic operations, and control hardware peripherals with single instruction. All instructions are 16-bit, 1-word instructions.

The μPD17P214 has a one-time PROM, instead of the internal mask ROM for the μPD17211, and an expanded internal memory. This one-time PROM model is suitable for evaluating the μPD17211 program and for small-scale production of the application system.

APPLICATIONS

- For infrared remote controller
- Prememory remote controller for various AV systems, such as TVs, VCRs, and audio equipment

APPLICATION EXAMPLE



FEATURES (Merit)

- Internal carrier generator for infrared remote controller
  - ⇨ Carrier frequency variable from 7.8 kHz to 1 MHz through program (with 4 MHz oscillator)

- Many I/O ports
  - ⇨ Can configure a 64-key key matrix

- Entire program memory area can be referenced through table
  - ⇨ Several remote controller formats can be programmed

- Wide oscillation frequency range
  - ⇨ 4 MHz ceramic oscillator or 455 kHz ceramic oscillator can be connected

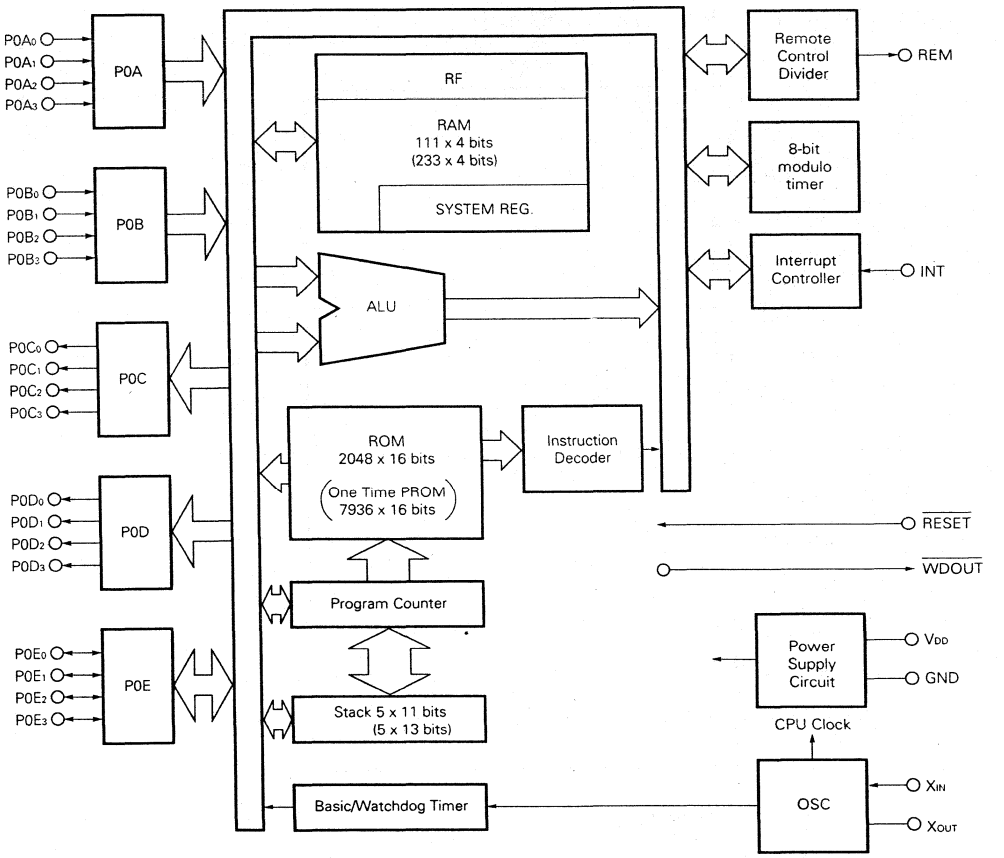
- Watchdog output pin

FUNCTIONAL OVERVIEW

❑ Functions

Product name	μPD17211	μPD17P214
ROM capacity	2048 x 16 bits (mask ROM)	7936 x 16 bits (one-time PROM)
RAM capacity	111 x 4 bits	223 x 4 bits
Instruction execution speed	4 μs (w/4 MHz ceramic oscillator normal mode) 17.6 μs (w/455 kHz ceramic oscillator high speed mode)	
Stack level	5 levels	
Number of I/O ports	Input ports: 9	
	Output ports (N-ch open-drain output): 8	
	I/O ports (CMOS push-pull output): 4	
Interrupt	3 channels { External interrupt: 1 channel Internal interrupt: 2 channels	
Timer	2 channels { 8-bit modulo timer: 1 channel Basic/watchdog timer: 1 channel	
Standby function	STOP mode/HALT mode	
Recommended operating voltage range	2.2 to 5.5 V	

BLOCK DIAGRAM

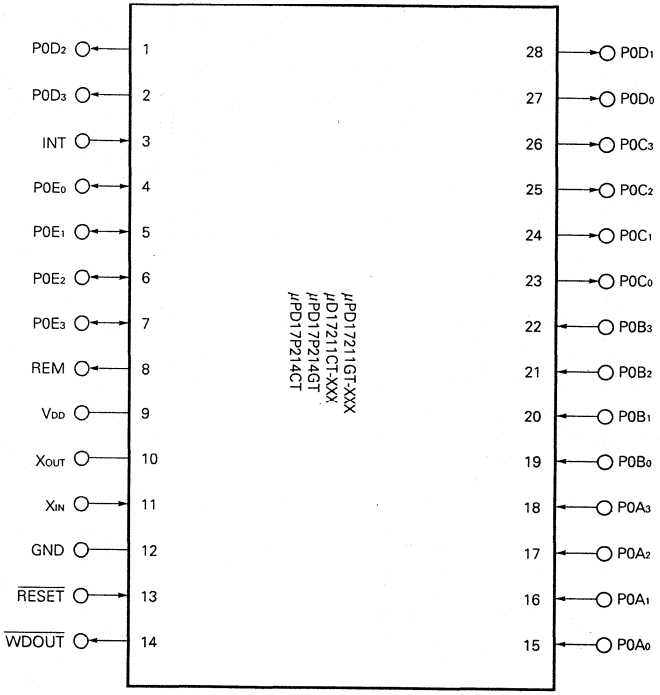


Remarks Values in this figure are for the μPD17211. The values for the μPD17P214 are enclosed in ( ) parentheses.

PACKAGE

- 28-pin plastic SOP (375 mil)
- 28-pin plastic shrink DIP (400 mil)

(Top View)



GND	: Ground
INT	: Interrupt input
P0A0-P0A3	: Port 0A (CMOS input)
P0B0-P0B3	: Port 0B (CMOS input)
P0C0-P0C3	: Port 0C (N-ch open-drain output)
P0D0-P0D3	: Port 0D (N-ch open-drain output)
P0E0-P0E3	: Port 0E (CMOS push-pull output)
REM	: Remote controller signal output (CMOS push-pull output)
$\overline{\text{RESET}}$	: Reset input
VDD	: Positive power
$\overline{\text{WDOUT}}$	: Watchdog output (N-ch open-drain output)
XIN, XOUT	: Oscillator connecting pins

DEVELOPMENT TOOLS

Hardware	IE-17K, IE-17K-ET*1	In-circuit emulator for common evaluation of 17K-series products	
	SE-17211*2	System evaluation board for μPD17211, μPD17P214	
	EP-17211GT*2 EP-17134CT	Emulation probe for SE-17211	
Software	AS17K	Common assembler for 17K series	• MS-DOS™ base (for PC-9801) • PC DOS™ base (for PC/AT™)
	AS17211*2	Device file for μPD17211, μPD17P214	
	SIMPLEHOST™	Man-machine interface software for MS-WINDOWS™	

*1 Low-price model: power supply excluded
*2 Under development

Instruction manual of the μPD17K-Family

Section 3 - Instruction manual of the μPD 17K-Family

CHAPTER 1 GENERAL

1.1 GENERAL DESCRIPTION

Each instruction of the μPD17000 series is composed of 16 bits per word. The instruction set contains 47 useful instructions having the following features:

(1) Permitting operation between memories in single step
(2) Permitting both binary and decimal calculation
(3) Permitting table reference on program memory (ROM)
(4) Permitting branching and subroutine call using the register value as address
(5) Well-arranged 47 types of instructions

This manual explains the instructions of the μPD17000 series. However, some instructions are inapplicable or limited in usage for certain products. Careful reference should be taken to the data sheet of the product you want to use before creating a program.

1.2 CONFIGURATION OF INSTRUCTION

The instruction codes of μPD17000 series are classified into the following three types:

(1) 0 operand instruction
Instructions 'INC AR', 'PUSH AR', 'RET', etc. These instructions have a unique or no operand.
(2) 1 operand instruction
Instructions 'RORC r', 'STOP s', etc. The address or immediate data is described in the operand.
(3) 2 operand instruction
Instructions 'ADD r, m', 'ADD m, #i', etc. Two addresses, or an address and immediate data are described in the operand.

CHAPTER 2 DATA MEMORY ADDRESSING

A data memory address is composed of a bank (four bits), row address (3 bits) and column address (four bits).

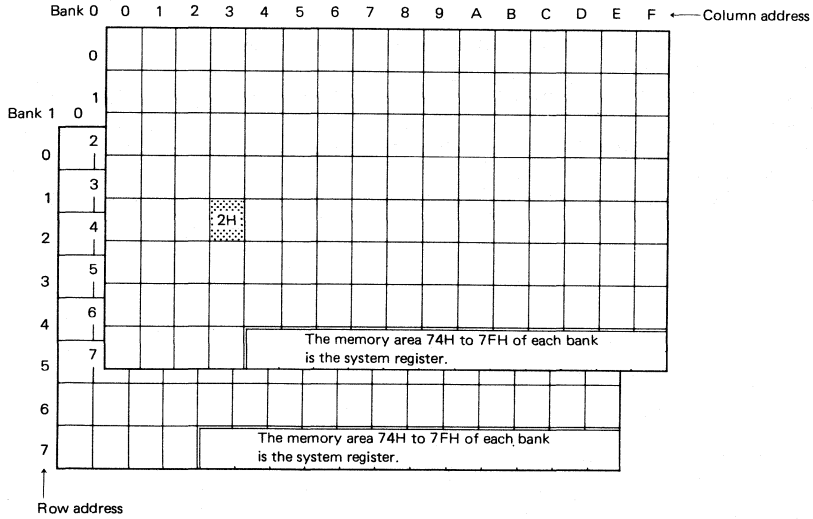
2.1 DIRECT ADDRESSING OF DATA MEMORY

When directly specifying data memory, the bank is specified by the BANK (bank register: 79H) of the system register, and the row address and column address are specified by the instruction operand m (seven bits).

[Example]

If BANK = 0,

```
MOV 43H, #2H
        |    |
        |    └── Immediate data
        └─── Address (Column address = 3, row address = 4)
```



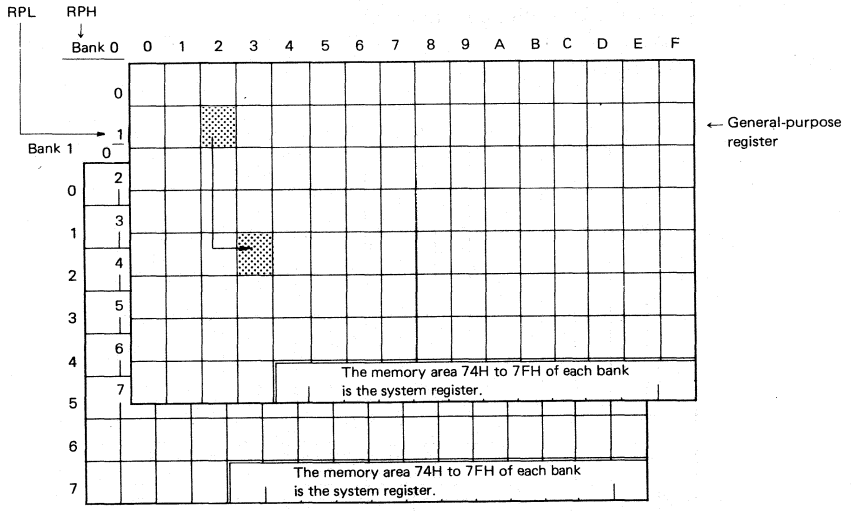
2.2 GENERAL-PURPOSE REGISTER ADDRESSING

When specifying a general-purpose register, the bank and row addresses are specified by RPH and RPL (register pointer: 7DH, 7EH) of the system register, and the column address is specified by the instruction operand r (four bits).

[Example]

When BANK = 0, RPH = 0, and RPL = 1;

```
ST 43H, 2H
   |    |
   |    └──General-purpose register column address
   └───Address
```



2.3 INDEX MODIFICATION ADDRESSING OF DATA MEMORY

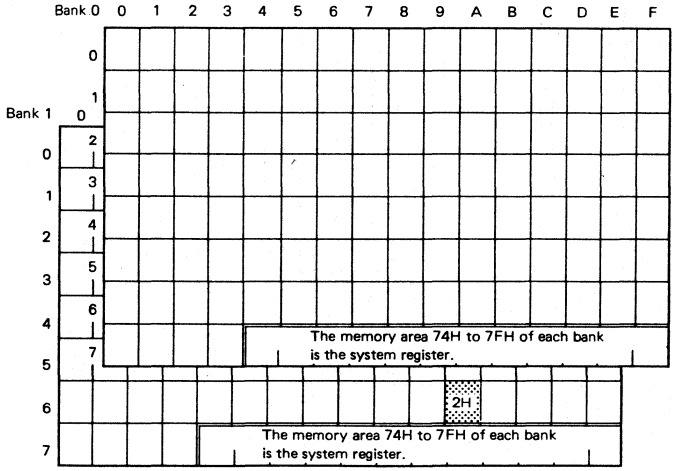
If IXE (index addressing enable flag: 7FH.0) of the system register is set '1', the data memory address is specified as the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of system register IXH, IXM, and IXL (index register: 7AH, 7BH, and 7CH).

[Example]

If BANK = 0, IXE = 1, IXH = 0, IXM = 0EH, and IXL = 8;

MOV 43H, #2H
- #2H: Immediate data
- 43H: Address

Data memory address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 1110 1000B]
= [0001 1101011B]
= 6BH of bank 1



2.4 GENERAL-PURPOSE REGISTER INDIRECT ADDRESSING OF DATA MEMORY

The data memory address specification method for executing the general-purpose register indirect transfer instruction 'MOV @r, m' and 'MOV m, @r' is explained below.

(1) When MPE = 0, IXE = 0

The bank for direct specification by operand m is specified by the system register BANK (bank register: 79H) and the row address and column address are specified by the instruction operand m (seven bits).

The bank for indirect specification by operand @r is specified by the system register BANK (bank register: 79H), and the row address is specified by the upper three bits of operand m. The column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system register RPH and RPL (register pointer: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

Accordingly, indirect transfer with MPE = 0 and IXE = 0 occurs within the same row address of the same bank.

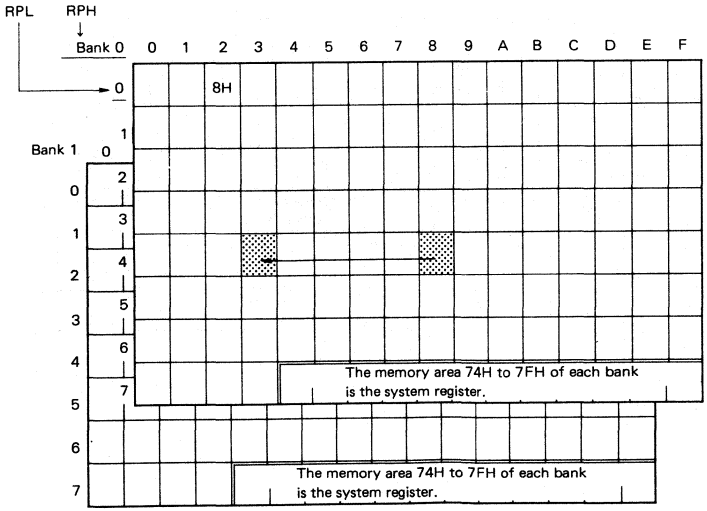
[Example]

When BANK = 0, RPH = 0, RPL = 0, and the value of address 0.02H is 8H;

MOV 43H, @2H
- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m]
= [0000 1000011B]
= 43H of bank 0

Indirect specification address = [BANK, $m_{6\text{-}4}$, (R)]
= [0000 100 1000B]
= 48H of bank 0



(2) When MPE = 1 and IXE = 0

The bank for direct specification by operand m is specified by the system register BANK (bank register: 79H), and the row address and column address are specified by the instruction operand m (seven bits).

The bank for indirect specification by operand @r and the row address are specified by the MPH and MPL (memory pointer: 7AH, 7BH) of the system register, and the column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the RPH and RPL (register pointer: 7DH, 7EH) of the system register, and the column address is specified by the instruction operand r (four bits).

Accordingly, when MPE = 1 and IXE = 0, indirect data transfer is allowed between any data memories.

[Example]

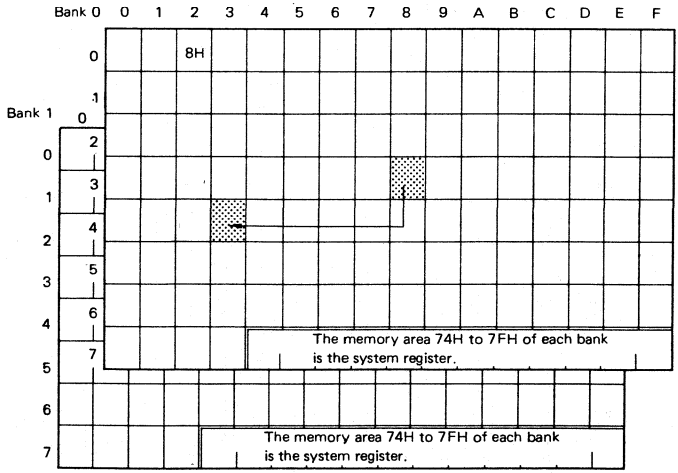
When BANK = 0, MPH = 0, MPL = 3, RPH = 0, RPL = 0, and the value of 0.02H address is 8H;

MOV 43H, @2H

- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m]
= [0000 1000011B]
= 43H of bank 0

Indirect specification address = [MPH, MPL, (R)]
= [000 0011 1000B]
= 38H of bank 0



(3) When MPE = 0 and IXE = 1

The bank, row address and column address for direct specification by operand m are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of system registers IXH, IXM and IXL (index registers: 7AH, 7BH, 7CH).

The bank and row address of the indirect specification by operand @r are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and the upper three bits of operand m and the contents of system registers IXH and IXM (index registers: 7AH, 7BH). The column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system registers RPH and RPL (register pointers: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

If MPE = 0 and IXE = 1, indirect transfer of data occurs within the same row address of the same bank.

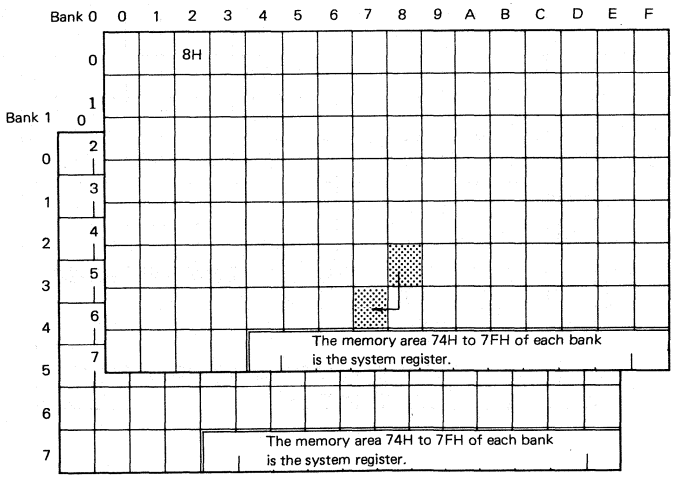
[Example]

When BANK = 0, IXH = 0, IXM = 2, IXL = 4, RPH = 0, RPL = 0, and the value of address 0.02H is 8H;

MOV 43H, @2H
- @2H: Indirect specification address
- 43H: Direct specification address

Direct specification address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 0010 0100B]
= [0000 1100111B]
= 67H of bank 0

Indirect specification address = [BANK, $m_{6\text{-}4}$, (R)] OR [IXH, IXM, 0]
= [0000 100 1000B] OR [000 0010 0000B]
= [0000 101 1000B]
= 58H of bank 0



(4) When MPE = 1, IXE = 1

The bank, row address, and column address by direct specification with operand m are specified by the ORed result of the address specified by the system register BANK (bank register: 79H) and instruction operand m (seven bits) and the contents of the system registers IXH, IXM, and IXL (index registers: 7AH, 7BH and 7CH). The bank and row address by indirect specification with operand @r is specified by the system registers MPH and MPL (memory pointers; 7AH, 7BH), and the column address is specified by the value of the general-purpose register. The bank and row address of the general-purpose register are specified by the system registers RPH and RPL (register pointers: 7DH, 7EH), and the column address is specified by the instruction operand r (four bits).

Accordingly, indirect data transfer with MPE = 1 and IXE = 1 is allowed between any data memories.

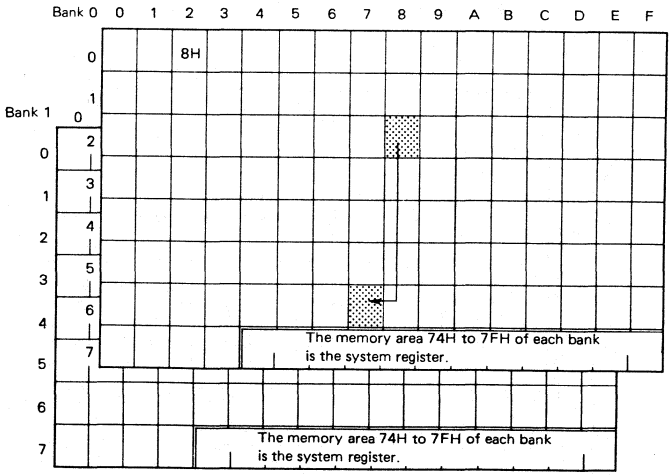
[Example]

When BANK = 0, IXH (MPH) = 0, IXM (MPL) = 2, IXL = 4, RPH = 0, RPL = 0, and value of address 0.02H is 8H;

MOV 43H, @2H
- 43H: Direct specification address
- @2H: Indirect specification address

Direct specification address = [BANK, m] OR [IXH, IXM, IXL]
= [0000 1000011B] OR [000 0010 0100B]
= [0000 1100111B]
= 67H of bank 0

Indirect specification address = [MPH, MPL, (R)]
= [000 0010 10000B]
= 28H of bank 0



CHAPTER 3 INSTRUCTION SET

This chapter explains the instruction set. The abbreviations used in the explanation of instruction set are shown below:

(X)	:	Value of data memory or register indicated by X (four bits)
[X, Y, Z]	:	Address consisting of upper 4 bits (X), medium 3 bits (Y) and lower 4 bits (Z) (Total 11 bits)
M	:	Data memory address If IXE = 0, then M = [(BANK), m_H, m_L] If IXE = 1, then M = [(BANK), m_H, m_L] OR (IX)
IXE	:	Index enable flag
(BANK)	:	Bank register value (4 bits)
m_H	:	Data memory row address (3 bits)
m_L	:	Data memory column address (4 bits)
(IX)	:	Index register value (11 bits)
R	:	General-purpose register address R = [(RP_H), (RP_L), r]
(RP_H)	:	General-purpose register bank (4 bits)
(RP_L)	:	General-purpose register row address (3 bits)
r	:	General-purpose register column address (4 bits)
i	:	Immediate data (4 bits)
addr	:	Address of branching destination
CY	:	Carry flag
SP	:	Stack pointer
STACK	:	Stack value indicated by stack pointer
AR	:	Address register
DBF	:	Data buffer
WR	:	Window register
rf	:	Register file address
rf_H	:	Upper 3 bits of register file address
rf_L	:	Lower 4 bits of register file address
p	:	Address of peripheral circuit
p_H	:	Upper 3 bits of peripheral circuit address
p_L	:	Lower 4 bits of peripheral circuit address

Note: Unless otherwise specified, the following conditions are used:

BANK = 0
RPH = 0, RPL = 0
IXE = 0

The data memory address is represented by direct address. When actually using an assembler, be sure to use the type MEM symbol. Any description of memory address directly into the operand will cause an error.

3.1 ADD r, m

Add data memory to general register

(1) Instruction code

00000	m_H	m_L	r

(2) Function

If CMP = 0, R ← (R) + (M)

The contents of the data memory addressed by M is added to the contents of the general-purpose register indicated by R, and the results are stored into the general-purpose register indicated by R.

If CMP = 1, then (R) + (M)

No results are stored. The flag only changes.

If a carry is made, set a carry flag (CY). If no carry is made, reset the carry flag (CY).

If the result of addition is other than zero, the zero flag (Z) is reset.

If the result of addition is zero, the zero flag (Z) will be set when the compare flag is in the reset status (CMP = 0). When the compare flag is in the set status (CMP = 1), the zero flag (Z) will not be changed if the result of addition is zero.

There are two types in addition: binary operation and BCD operation. The addition type is selected by the BCD flag (BCD) of PSW.

(3) **Example 1**

When the row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the result of addition of the contents of 0.2FH address is stored to the contents of 0.03H address.

```
0.03H ← (0.03H) + (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #00H  ;  General-purpose register bank to 0
MOV RPL, #00H  ;  General-purpose register row address to 0
ADD 03H, 2FH
```

Example 2

When row address 2 (1.20H to 1.2FH) of bank 1 is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 1.23H is added to the content of address 0.2FH, and the results are stored into address 1.23H.

```
1.23H ← (1.23H) + (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #01H  ;  General-purpose register bank 1
MOV RPL, #04H  ;  General-purpose register row address 2
ADD 03H, 2FH
```

Example 3

The result of addition of the contents of address 0.03H and address 0.6FH is stored into address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) + (0.6FH)
└── ORed result of index register content 0.40H and data memory address 0.2FH

```
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
MOV  IXH, #00H   ;  IX ← 00001000000B
MOV  IXM, #04H   ;
MOV  IXL, #00H   ;
SET1 IXE         ;  IXE flag ← 1
ADD  03H, 2FH    ;  IX                    00001000000B (0.40H)
                 ;  Bank operand OR    )  00000101111B (0.2FH)
                 ;  Specified address     00001101111B (0.6FH)
```

Example 4

The result of addition of the contents of address 0.03H and address 2.3FH is stored into address 0.03H. If IXE = 1, IXH = 1, IXM = 1, and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) + (2.3FH)
└── ORed result of the content of index register 2.10H and data memory address 0.2FH

```
MOV  BANK, #00H
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
MOV  IXH, #01H   ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H
MOV  IXL, #00H
SET1 IXE         ;  IXE flag ← 1
ADD  03H, 2FH    ;  IX                    00100010000B (2.10H)
                 ;  Bank operand OR    )  00000101111B (0.2FH)
                 ;  Specified address     00100111111B (2.3FH)
```

(4) **Note**

The 1st operand of 'ADD r, m' instruction is the column address of general-purpose register. If it is described as follows, the general-purpose register column address is taken as 03H. This will not cause any error in assembling.

```
ADD 13H, 2FH
    └── General-purpose register column address is meant.
        The lower 4 bits are significant.
```

If CMP flag = 1, no added result is stored.

If BCD flag = 1, the result of decimal operation is stored.

3.2 ADD m, #i

Add immediate data to data memory

(1) Instruction code

10000	m_H	m_L	i

(2) Function

If CMP = 0, then M ← (M) + i

The immediate data i is added to the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1, then (M) + i

No result is stored. Only the flag changes.

If any carry occurs as a result of addition, the carry flag (CY) is set. If no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, the zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is added to the content of address 0.2FH, and the result is stored to address 0.2FH.

```
0.2FH ← (0.2FH) + 5
ADD 2FH, #05H
```

Example 2

Value 5 is added to the content of address 0.6FH, and the result is stored to address 0.6FH. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

```
0.6FH ← (0.6FH) + 05H
          └── ORed result of the index register content 0.40H and data
              memory address 0.2FH
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  2FH, #05H  ;  IX                    00001000000B
                ;  Bank operand OR  )    00000101111B (0.2FH)
                ;  Specified address     00001101111B (0.6FH)
```

Example 3

Value 5 is added to the content of address 2.2FH, and the result is stored to address 2.2FH. If IXE = 1, IXH = 1, IXM = 0 and IXL = 0, that is, if IX = 2.00H, then the data memory 2.2FH can be specified by setting the data memory address at 2FH.

2.2FH ← (2.2FH) + 05H

└—ORed result of index register content 2.00H and data memory address 0.2FH

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #01H  ;  iX ← 00100000000B
MOV  IXM, #00H
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  2FH, #05H  ;  IX                  00100000000B (2.00H)
                ;  Bank operand OR  ) 00000101111B (0.2FH)
                ;  Specified address  00100101111B (2.2FH)
```

(4) **Note**

If CMP flag = 1, then no addition result is stored.

If BCD flag = 1, the result of decimal operation is indicated.

3.3 ADDC r, m

Add data memory to general register with carry flag

(1) Instruction code

00010	m_H	m_L	r

(2) Function

If CMP = 0, then R ← (R) + (M) + CY

The content of general-purpose register indicated by R, the content of data memory addressed by M and the value of carry flag (CY) are added, and the result is stored into the general-purpose register indicated by R.

If CMP = 1, then (R) + (M) + CY

The result of addition is not stored. Only the flag is changed.

Use of this 'ADDC' instruction permits addition to two words or more can be performed easily.

If a carry occurs as a result of addition, the carry flag (CY) is set; if no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

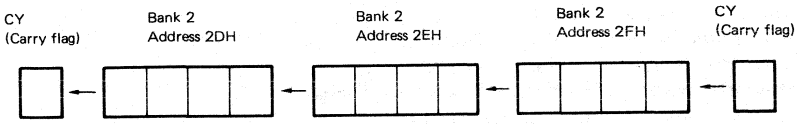
(3) **Example 1**

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as a general-purpose register, the 12-bit content of address 0.2DH-0.2FH is added to the 12-bit content of address 0.0DH-0.0FH, and then the result is stored into the 12-bit area of address 0.0DH-0.0FH.

```
0.0FH ← (0.0FH) + (0.2FH)
0.0EH ← (0.0EH) + (0.2EH) + CY
0.0DH ← (0.0DH) + (0.2DH) + CY
MOV  BANK, #00H  ;  Data memory bank 0
MOV  RPH, #00H   ;  General-purpose register bank 0
MOV  RPL, #00H   ;  General-purpose register row address 0
ADD  0FH, 2FH
ADDC 0EH, 2EH
ADDC 0DH, 2DH
```

Example 2

When row address 2 (1.20H to 1.2FH) of bank 1 is specified as a general-purpose register, the 12-bit content of address 1.2DH to 1.2FH is shifted to the left including a carry flag by one.




```
MOV  RPH, #01H   ;  General-purpose register bank 1
MOV  RPL, #04H   ;  General-purpose register row address 2
MOV  BANK, #01H  ;  Data memory bank 1
ADDC 0FH, 2FH
ADDC 0EH, 2EH
ADDC 0DH, 2DH
```

Example 3

The content of address 0.0FH and the contents of addresses 0.40H to 0.4FH are added, and then store the result into address 0.0FH.

0.0FH ← (0.0FH) + (0.40H) + (0.41H) + ... + (0.4FH)

```
        MOV  BANK, #00H  ;  Data memory bank 0
        MOV  RPH, #00H   ;  General-purpose register bank 0
        MOV  RPL, #00H   ;  General-purpose register row address 0
        MOV  IXH, #00H   ;  IX ← 00001000000B (0.40H)
        MOV  IXM, #04H
        MOV  IXL, #00H
LOOP1:
        SET1 IXE         ;  IXE flag ← 1
        ADD  0FH, 00H
        CLR1 IXE         ;  IXE flag ← 0
        INC  IX          ;  IX ← IX + 1
        SKE  IXL, #0
        JMP  LOOP1
```

Example 4

The 12-bit contents of addresses 1.40H to 1.42H are added to the 12-bit contents of addresses 0.0DH to 0.0FH, then the result is stored to the 12-bit area of addresses 0.0DH to 0.0FH.

0.0DH ← (0.0DH) + (1.40H)
0.0EH ← (0.0EH) + (1.41H) + CY
0.0FH ← (0.0FH) + (1.42H) + CY

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00011000000 (1.40H)
MOV  IXM, #0CH
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  0DH, 00H   ;  0.0DH ← (0.0DH) + (1.40H)
ADDC 0EH, 01H   ;  0.0EH ← (0.0EH) + (1.41H)
ADDC 0FH, 02H   ;  0.0FH ← (0.0FH) + (1.42H)
```

3.4 ADDC m, #i

Add immediate data to data memory with carry flag

(1) Instruction code

10010	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) + i + CY

The values of immediate data i and carry flag (CY) are added to the content of data memory addressed by M, and the result is stored to the data memory addressed by M.

If CMP = 1: (M) + i + CY

The result is not stored. Only the flag is changed.

If a carry occurs as a result of addition, the carry flag (CY) is set; if no carry occurs, the carry flag (CY) is reset.

If the result of addition is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of addition is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of addition turns zero.

There are two types of addition: binary operation and BCD operation. The addition type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

The value 5 is added to the 12-bit contents of addresses 0.0DH to 0.0FH, and then the result is stored to the addresses 0.0DH to 0.0FH.

```
0.0FH ← (0.0FH) + 05H
0.0EH ← (0.0EH) + CY
0.0DH ← (0.0DH) + CY
MOV BANK, #00H ; Data memory bank 0
ADD 0FH, #05H
ADDC 0EH, #00H
ADDC 0DH, #00H
```

Example 2

The value 5 is added to the 12-bit contents of addresses 0.4DH to 0.4FH, and the result is stored to the addresses 0.4DH to 0.4FH.

```
0.4FH ← (0.4FH) + 05H
0.4EH ← (0.4EH) + CY
0.4DH ← (0.4DH) + CY
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H
MOV  IXL, #00H
SET1 IXE        ;  IXE flag ← 1
ADD  0FH, #5       0.4FH ← (0.4FH) + 05H
ADDC 0EH, #0       0.4EH ← (0.4EH) + CY
ADDC 0DH, #0       0.4DH ← (0.4DH) + CY
```

3.5 SUB r, m

Subtract data memory from general register

(1) Instruction code

00001	m_H	m_L	r

(2) Function

If CMP = 0: R ← (R) – (M)

The content of data memory addressed by M is subtracted from the content of general-purpose register indicated by R, and the result is stored into the general-purpose register indicated by R.

If CMP = 1: (R) – (M)

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the content of address 0.2FH is subtracted from the content of address 0.03H, then the result is stored to the address 0.03H.

```
0.03H ← (0.03H) – (0.2FH)
SUB 03H, 2FH
```

Example 2

When bank 1 row address 2 (1.20H to 1.2FH) is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 0.2FH is subtracted from the content of address 1.23H, and the result is stored to the address 1.23H.

```
1.23H ← (1.23H) – (0.2FH)
MOV BANK, #00H ;  Data memory bank 0
MOV RPH, #01H  ;  General-purpose register bank 1
MOV RPL, #04H  ;  General-purpose register row address 2
SUB 03H, 2FH
```

Example 3

The content of address 0.6FH is subtracted from the content of address 0.03H, and the result is stored to the address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) – (0.6FH)

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  03H, 2FH   ;  IX                  00001000000B (0.40H)
                ;  Bank operand OR  ) 00000101111B (0.2FH)
                ;  Specified address  00001101111B (0.6FH)
```

Example 4

The content of address 2.3FH is subtracted from the content of address 0.03H, and the result is stored to the address 0.03H. If IXE = 1, IXH = 1, IXM = 1 and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

0.03H ← (0.03H) – (2.3FH)

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #01H  ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  03H, 2FH   ;  IX                  00100010000B (2.10H)
                ;  Bank operand OR  ) 00000101111B (0.2FH)
                ;  Specified address  00100111111B (2.3FH)
```

(4) **Note**

The 1st operand of the 'SUB r, m' instruction must be a general-purpose register address. The address 03H is specified as a register if described as follows. This will not cause an error in assembling.

```
SUB 13H, 2FH
    └── The general-purpose register address must fall within the range from 00H to 0FH
        (with register pointer set at other than row address 1).
```

If CMP flag = 1, the subtracted result is not stored.

If BCD flag = 1, the result of decimal operation is stored.

3.6 SUB m, #i

Subtract immediate data from data memory

(1) Instrctuion code

10001	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) − i

The immediate data i is subtracted from the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1: (M) − i

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is subtracted from the contents of address 0.2FH, and the result is stored to the address 0.2FH.

0.2FH ← (0.2FH) − 5

SUB 2FH, #05H

Example 2

The value 5 is subtracted from the content of address 0.6FH, and the result is stored to the address 0.6FH. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

0.6FH ← (0.6FH) − 5

└── ORed result of the content 0.40H of index register and the data memory address 0.2FH

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  2FH, #05H  ;  IX                  00001000000B (0.40H)
                ;  Bank operand OR  ) 00000101111B (0.2FH)
                ;  Specified address  00001101111B (0.6FH)
```

Example 3

The value 5 is subtracted from the content of address 2.2FH, and the result is stored to the address 2.2FH. If IXE = 1, IXH = 1, IXM = 0, and IXL = 0, that is, if IX = 2.00H, then the data memory 2.2FH can be specified by setting the data memory address at 2FH.

2.2FH ← (2.2FH) – 5
└── ORed result of the content 2.00H of index register and the data memory address 0.2FH

```
MOV BANK0, #00H;  Data memory bank 0
MOV IXH, #01H   ;  IX ← 00100000000B (2.00H)
MOV IXM, #00H   ;
MOV IXL, #00H   ;
SET1 IXE        ;  IXE flag ← 1
SUB 2FH, #05H   ;  IX                  00100000000B (2.00H)
                ;  Bank operand OR  )  00000101111B (0.2FH)
                ;  Specified address    00100101111B (2.2FH)
```

(4) **Note**

If CMP flag = 1, no subtract result is stored.

If BCD flag = 1, the result of decimal operation is stored.

3.7 SUBC r, m

Subtract data memory from general register with carry flag

(1) Instruction code

00011	m_H	m_L	r

(2) Function

If CMP = 0: R ← (R) − (M) − CY

The content of data memory indicated by address M and the value of carry flag (CY) are subtracted from the content of general-purpose register indicated by R, and the result is stored into the general-purpose register indicated by R. Use of this SUBC instruction permits subtraction of more than two words to be performed easily.

If CMP = 1: (R) − (M) − CY

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

When bank 0 row address 0 (0.00H to 0.0FH) is specified as general-purpose register, the 12-bit contents of addresses 0.2DH to 0.2FH are subtracted from the 12-bit content of addresses 0.0DH to 0.0FH, and then the result is stored into the 12-bit area of addresses 0.0DH to 0.0FH.

```
0.0FH ← (0.0FH) − (0.2FH)
0.0EH ← (0.0EH) − (0.2EH) − CY
0.0DH ← (0.0DH) − (0.2DH) − CY
SUB 0FH, 2FH
SUBC 0EH, 2EH
SUBC 0DH, 2DH
```

Example 2

The contents of 12 bits from addresses 1.40H to 1.42H are subtracted from the contents of 12 bits from addresses 0.0DH to 0.0FH, and then the result is stored to the 12 bits from 0.0DH to 0.0FH.

0.0DH ← (0.0DH) – (1.40H)
0.0EH ← (0.0EH) – (1.41H) – CY
0.0FH ← (0.0FH) – (1.42H) – CY

```
MOV  BANK, #00H ;  Data memory bank 0
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
MOV  IXH, #00H  ;  IX ← 00011000000B (1.40H)
MOV  IXM, #0CH  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  0DH, 00H   ;  0.0DH ← (0.0DH) – (1.40H)
SUBC 0EH, 01H   ;  0.0EH ← (0.0EH) – (1.41H)
SUBC 0FH, 02H   ;  0.0FH ← (0.0FH) – (1.42H)
```

Example 3

The contents of 12 bits from addresses 0.00H to 0.03H and the contents of 12 bits from addresses 0.0CH to 0.0FH are compared. If identical, jump is made to LAB1; if different, jump is made to LAB2.

```
        SET2 CMP, Z    ;  CMP flag ← 1, Z flag ← 1
        SUB  00H, 0CH  ;  The contents of addresses 0.00H-0.03H
        SUBC 01H, 0DH  ;  are not changed because the CMP flag is
        SUBC 02H, 0EH  ;  set.
        SUBC 03H, 0FH
        SKF1 Z         ;  If proven as identical by comparison, Z
        BR   LAB1      ;  flag = 1; if proven as different, Z
        BR   LAB2      ;  flag = 0.

LAB1:
LAB2:
```

3.8 SUBC m, #i

Subtract immediate data from data memory with carry flag

(1) Instruction code

10011	m_H	m_L	i

(2) Function

If CMP = 0: M ← (M) − i − CY

The immediate data i and the value of carry flag (CY) are subtracted from the content of data memory addressed by M, and the result is stored into the data memory addressed by M.

If CMP = 1: (M) − i − CY

The result is not stored. Only the flag is changed.

If a borrow occurs as a result of subtraction, the carry flag (CY) is set; if no borrow occurs, the carry flag (CY) is reset.

If the result of subtraction is other than zero, then zero flag (Z) is reset.

If the compare flag is reset (CMP = 0) when the result of subtraction is zero, the zero flag (Z) is set. If the compare flag is set (CMP = 1), the zero flag (Z) will not change when the result of subtraction turns zero.

There are two types of subtraction: binary operation and BCD operation. The subtraction type is specified by the BCD flag (BCD) of PSW.

(3) **Example 1**

Value 5 is subtracted from the contents of 12 bits of addresses 0.0DH to 0.0FH, and the result is stored to addresses 0.0DH to 0.0FH.

```
0.0FH ← (0.0FH) − 05H
0.0EH ← (0.0EH) − CY
0.0DH ← (0.0DH) − CY
SUB  0FH, #05H
SUBC 0EH, #00H
SUBC 0DH, 00H
```

Example 2

Value 5 is subtracted from the contents of 12 bits of addresses 0.4DH to 0.4FH, and the result is stored into addresses 0.4DH to 0.4FH.

```
0.4FH ← (0.4FH) − 05H
0.4EH ← (0.4EH) − CY
0.4DH ← (0.4DH) − CY
MOV  BANK, #00H ;  Data memory bank 0
MOV  IXH, #00H  ;  IX ← 00001000000B (0.40H)
MOV  IXM, #04H  ;
MOV  IXL, #00H  ;
SET1 IXE        ;  IXE flag ← 1
SUB  0FH, #5    ;  (0.4FH) (0.4FH) − 05H
SUBC 0EH, #0    ;  (0.4EH) (0.4EH) − CY
SUBC 0DH, #0    ;  (0.4DH) (0.4DH) − CY
```

Example 3

The contents of 12 bits of addresses 0.00H to 0.03H and 0A3FH of the immediate data are compared. If identical, jump is made to LAB1; if different, jump is made to LAB2.

```
        SET2 CMP, Z     ;  CMP flag ← 1, Z flag ← 1
        SUB 00H, #0H    ;  The contents of addresses 0.00H to 0.03H
        SUBC 01H, #AH ;  remain unchanged because the CMP flag is
        SUBC 02H, #3H ;  set.
        SUBC 03H, #FH
        SKF1  Z         ;  If identical in comparison, Z flag = 1;
        BR    LAB1      ;  if different, Z flag = 0
        BR    LAB2
            :
            :
LAB1:
            :
            :
LAB2:
            :
```

3.9 INC AR

Increment address register

(1) Instruction code

00111	000	1001	0000

(2) Function

AR ← (AR) + 1

Address register (AR) is incremented.

(3) **Example 1**

Value 1 is added to the contents of 16 bits of AR3 to AR0 (address register) in the system register, and the result is stored from AR3 to AR0.

```
AR0 ← AR0 + 1
AR1 ← AR1 + CY
AR2 ← AR2 + CY
AR3 ← AR3 + CY
```

INC AR

This instruction can be performed by using addition instruction as follows:

```
ADD  AR0, #01H
ADDC AR1, #00H
ADDC AR2, #00H
ADDC AR3, #00H
```

Example 2

The table data is transferred to DBF (data buffer) in units of 16 bits (one address). (For details, refer to 3.26 "MOVT Instruction".)

```
; Address          Table data
010H   DW          0F3FFH
011H   DW          0A123H
012H   DW          0FFF1H
013H   DW          0FFF5H
014H   DW          0FF11H
       :
       :
       MOV         AR3, #0H  ;  Table data address
       MOV         AR2, #0H  ;  0010H is set into address
       MOV         AR1, #1H  ;  register.
       MOV         AR0, #0H
LOOP:
       MOVT        @AR       ;  Table data is read into DBF.
       :
       :                     ;  Table data referencing
       :
       INC         AR        ;  Address register is incremented
       BR          LOOP         by 1.
```

(4) **Note**

The number of bits allowed for use with address registers (AR3, AR2, AR1, AR0) vary with the device types. When using, reference should be made to the appropriate manual of the device to be used.

3.10 INC IX

Increment index register

(1) Instruction code

00111	000	1000	0000

(2) Function

IX ← (IX) + 1

The index register (IX) is incremented.

(3) **Example 1**

Value 1 is added to the content of 12 bits of IXH to IXL (index register) in the system register, and the result is stored into the IXH to IXL.

```
IXL ← IXL + 1
IXM ← IXM + CY
IXH ← IXH + CY
INC IX
```

This operation can be performed by using the addition instruction as follows:

```
ADD  IXL, #01H
ADDC IXM, #00H
ADDC IXH, #00H
```

Example 2

The contents of data memory 0.00H to 0.73H are all turned '0' using the index register.

```
    MOV  IXH, #00H   ;  The contents of index register
    MOV  IXM, #00H   ;  are all set at 00H of bank 0.
    MOV  IXL, #00H   ;
RAM clear:
    SET1 IXE         ;  IXE flag ← 1
    MOV  00H, #00H   ;  0 is written into the data memory indicated by the index register.
    CLR1 IXE         ;  IXE flag ← 0
    INC  IX
    SET2 CMP, Z      ;  CMP flag ← 1, Z flag ← 1
    SUB  IXL, #03H   ;  Whether the content of index
    SUBC IXM, #07H   ;  register turned to 73H of bank 0
    SUBC IXH, #00H   ;  is checked.
    SKT1 Z           ;  Loop is repeated until the contents
    BR   RAM clear   ;  of index register turns to 73H of
                     ;  bank 0.
```

3.11 SKE m, #i

Skip if data memory equal to immediate data

(1) Instruction code

01001	m_H	m_L	i

(2) Function

If the content of the data memory addressed by M is equal to the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

0FH is transferred to address 24H if the content of address 24H is 0. If not 0, control jumps to OPE1.

```
    SKE 24H, #00H
    BR  OPE1
    MOV 24H, #0FH
OPE1 :
```

3.12 SKGE m, #i

Skip if data memory greater than or equal to immediate data

(1) Instruction code

11001	m_H	m_L	i

(2) Function

If the content of the data memory addressed by M is greater than the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the 8-bit data stored in address 1FH (upper) and address 2FH (lower) is greater than the immediate data '17H', then RET occurs; otherwise, RETSK occurs.

```
SKGE   1FH, #1
RETSK
SKNE   1FH, #1
SKLT   2FH, #8  ;  7 + 1
RET
RETSK
```

3.13 SKLT m, #i

Skip if data memory less than immediate data

(1) Instruction code

11011	m_H	m_L	i

(2) Function

If the content of data memory addressed by M is less than the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the content of address 10H is greater than the immediate data '6', then 01H is stored into address 0FH; if less than the immediate data '6', 02H is stored into address 0FH.

```
MOV   0FH, #02H
SKLT  10H, #06H
MOV   0FH, #01H
```

3.14 SKNE m, #i

Skip if data memory not equal to immediate data

(1) Instruction code

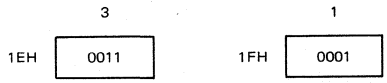
01011	m_H	m_L	i

(2) Function

If the content of data memory addressed by M is different from the value of immediate data i, then the instruction that follows is skipped.

(3) **Example**

If the content of address 1FH is 1 and the content of 1EH is 3, then control jumps to XYZ; if not, control jumps to ABC. Comparison of 8 bits can be performed by combining the instructions as shown below:




```
SKNE 1FH, #1
SKE 1EH, #3
BR  ABC
BR  XYZ
```

The same operation can be performed by using the compare flag and zero flag, as shown below.

```
SET2 CMP, Z      ;  CMP flag ← 1, Z flag ← 1
SUB 1FH, #1
SUBC 1EH, #3
SKT1 Z
BR  ABC
BR  XYZ
```

3.15 AND m, #i

AND between data memory and immediate data

(1) Instruction code

10100	m_H	m_L	i

(2) Function

M ← (M) AND i

The content of data memory addressed by M and the immediate data are ANDed, and the result is stored into the data memory addressed by M.

(3) **Example 1**

Bit 3 (MSB) of address 0.03H is reset.

0.03H ← (0.03H) and 0111B

Address 0.03H

0	x	x	x

x: Don't care

```
AND     03H, #0111B
```

Example 2

All the bits of address 0.03H are reset.

```
AND     03H, #0000B
```

or

```
MOV     03H, #00H
```

3.16 AND r, m

AND between general register and data memory

(1) Instruction code

00100	m_H	m_L	r

(2) Function

R ← (R) AND (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are ANDed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content (1010B) of address 0.03H and the content (0110B) of address 0.2FH are ANDed, and the result (0010B) is stored into address 0.03H.

0.03H ← (0.03H) and (0.2FH)

1	0	1	0	Address 03H
		and		
0	1	1	0	Address 2FH
↓				
0	0	1	0	Address 03H

```
MOV 03H, #1010B
MOV 2FH, #0110B
AND 03H, 2FH
```

3.17 OR m, #i

OR between data memory and immediate data

(1) Instruction code

10110	m_H	m_L	i

(2) Function

M ← (M) OR i

The content of data memory addressed by M and the immediate data i are ORed, and the result is stored into the data memory addressed by M.

(3) **Example 1**

Bit 3 (MSB) of address 0.03H is set.

0.03H ← (0.03H) or 1000B

Address 0.03H

1	x	x	x

x: Don't care

OR 03H, #1000B

Example 2

All the bits of address 0.03H are set.

OR 03H, #1111B

or

MOV 03H, #0FH

3.18 OR r, m

OR between general register and data memory

(1) Instruction code

00110	m_H	m_L	r

(2) Function

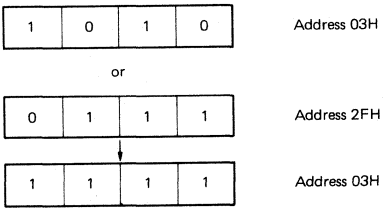
R ← (R) OR (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are ORed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content (1010B) of address 0.03H and the content (0111B) of address 0.2FH are ORed, and the result (1111B) is stored into address 0.03H.

0.03H ← (0.03H) or (0.2FH)




```
MOV   03H, #1010B
MOV   2FH, #0111B
OR    03H, 2FH
```

3.19 XOR m, #i

Exclusive OR between data memory and immediate data

(1) Instruction code

10101	m_H	m_L	i

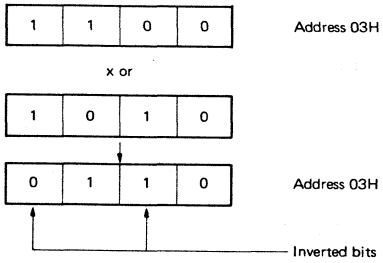
(2) Function

M ← (M) XOR i

The content of data memory addressed by M and the immediate data i are XORed, and the result is stored into the data memory addressed by M.

(3) **Example**

The bit 1 and bit 3 of address 0.03H are inverted, and the result is stored into address 03H.



XOR 03H, #1010B

3.20 XOR r, m

Exclusive OR between general register and data memory

(1) Instruction code

00101	m_H	m_L	r

(2) Function

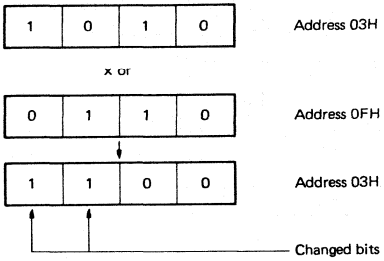
R ← (R) XOR (M)

The content of general-purpose register indicated by R and the content of data memory addressed by M are XORed, and the result is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content of address 0.03H and the content of address 0.0FH are compared, and the different bits are set and stored into address 0.03H. If all bits of 0.03H are reset (that is, the address 0.03H and address 0.0FH have the same content), then control jumps to LBL1; otherwise, jumps to LBL2.

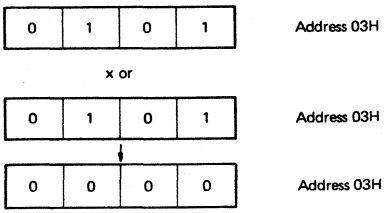
This operation occurs when the status of an alternate switch (content of address 0.03H) and internal status (content of address 0.0FH) are compared and branch is made to the processing of changed switch.




```
XOR   03H, 0FH
SKNE  03H, #00H
BR    LBL1
BR    LBL2
```

Example 2

The content of address 0.03H is cleared.




```
XOR   03H, 03H
```

3.21 LD r, m

Load data memory to general register

(1) Instruction code

01000	m_H	m_L	r

(2) Function

R ← (M)

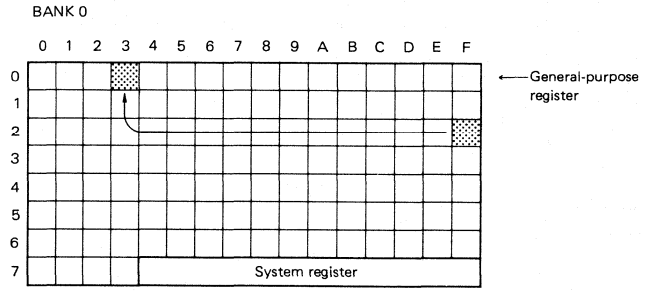
The content of data memory addressed by M is stored into the general-purpose register indicated by R.

(3) **Example 1**

The content of address 0.2FH is stored into address 0.03H.

0.03H ← (0.2FH)

```
LD      03H, 2FH
```

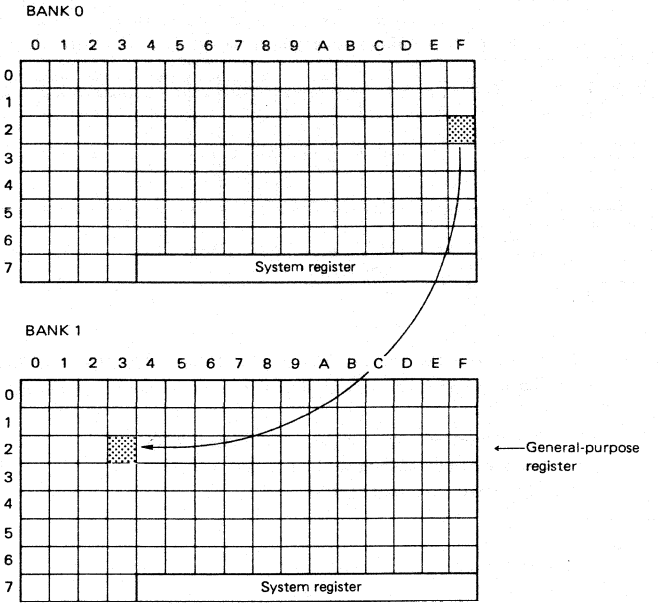


Example 2

When row address 2 of bank 1 (1.20H to 1.2FH) is specified as general-purpose register (RPH = 1, RPL = 4), the content of address 0.2FH is stored into address 1.23H.

1.23H ← (0.2FH)

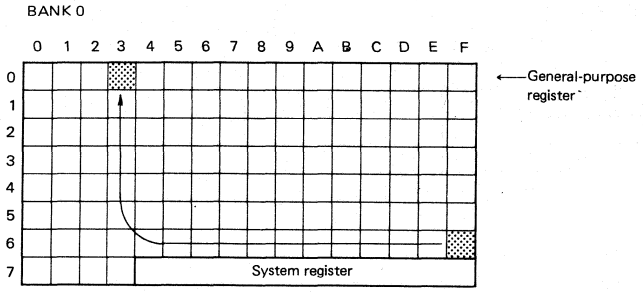
```
MOV  RPH, #01H   ;  Bank 1 is selected for general-purpose register.
MOV  RPL, #04H   ;  Row address 2 is selected for general-purpose register
LD   03H, 2FH
```



Example 3

The content of address 0.6FH is stored into address 0.03H. If IXE = 1, IXH = 0, IXM = 4, and IXL = 0, that is, if IX = 0.40H, then the data memory 0.6FH can be specified by setting the data memory address at 2FH.

```
IXH ← 00H
IXM ← 04H
IXL ← 00H
IXE flag ← 1
0.03H ← (0.6FH)
          └──Address obtained by computing OR of the content (0.40H) of
             index register and the content (0.2FH) of data memory.
MOV IXH, #00H    ;  IX ← 00001000000B (0.40H)
MOV IXM, #04H
MOV IXL, #00H
SET1 IXE         ;  IXE flag ← 1
LD 03H, 2FH
```

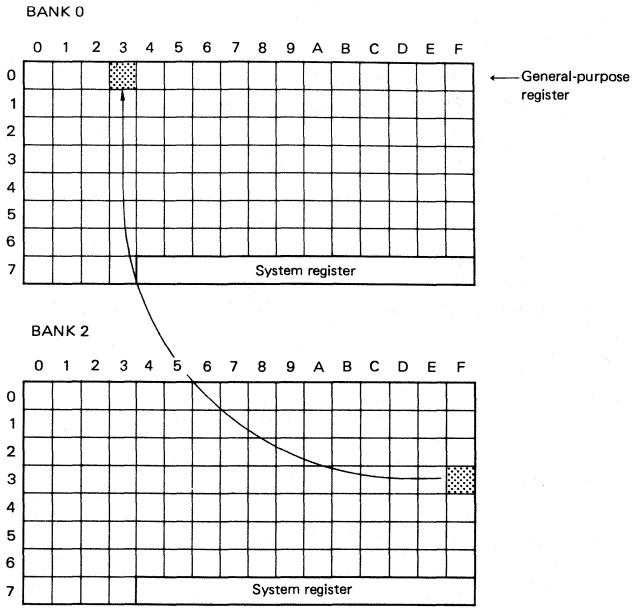


Example 4

The content of address 2.3FH is stored into address 0.03H. If IXE = 1, IXH = 1, IXM = 1, and IXL = 0, that is, if IX = 2.10H, then the data memory 2.3FH can be specified by setting the data memory address at 2FH.

0.03H ← (2.3FH)
└ Address obtained by computing OR of the content (2.10H) of index register and the content (0.2FH) of data memory

```
MOV  IXH, #01H    ;  IX ← 00100010000B (2.10H)
MOV  IXM, #01H
MOV  IXL, #00H
SET1 IXE          ;  IXE flag ← 1
LD   03H, 2FH
```



(4) **Note**

The 1st operand of the 'LD r, m' instruction is the column address of the general-purpose register. If described as shown below, the column address of the general-purpose register is set at 03H. This will cause no error in assembling.

```
LD   13H, 2FH
     └── Column address of general-purpose register is meant, and the lower four bits
         are significant. If row address 0 of bank 0 is specified as general-purpose
         register, the address 03H is specified.
```

3.22 ST m, r

Store general register to data memory

(1) Instruction code

11000	m_H	m_L	r

(2) Function

M ← (R)

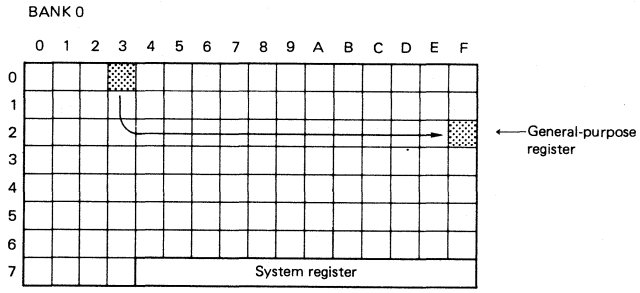
The content of general-purpose register indicated by R is stored into the data memory addressed by M.

(3) **Example 1**

The content of address 0.03H is stored into address 0.2FH.

(0.2FH) ← (0.03H)

```
ST   2FH, 03H      ;  The content of general-purpose register is transferred to data memory.
```

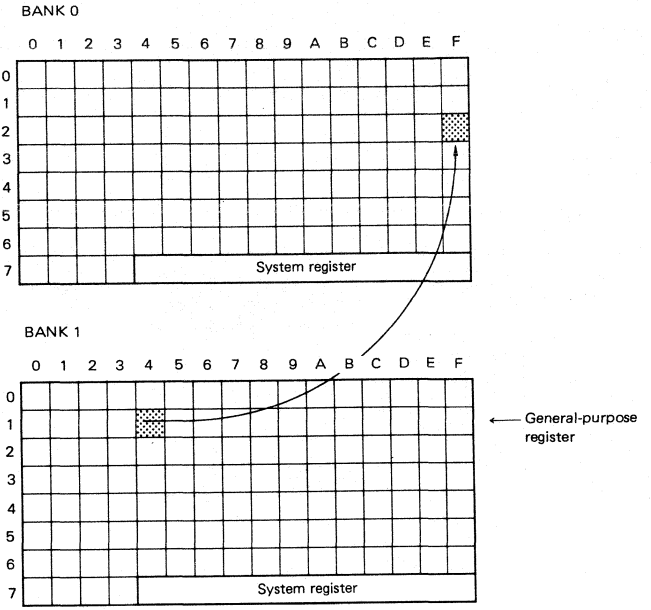


Example 2

The content of address 1.13H is stored into address 0.2FH. The general-purpose register is specified at row address 1 of bank 1 (1.10H to 1.1FH) by using register pointer.

(0.2FH) ← (1.13H)

```
MOV  RPH, #01H     ;  General-purpose register is set in bank 1
MOV  RPL, #02H     ;  General-purpose register is set at row address 1.
ST   2FH, 13H      ;  The content of general-purpose register is transferred to data memory.
```

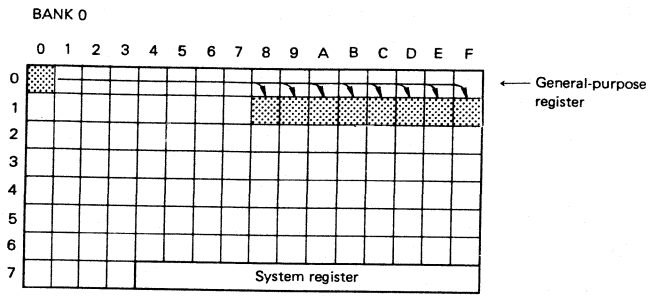


Example 3

The content of address 0.00H is stored into the addresses 0.18H to 0.1FH. The data memory (18H to 1FH) is specified by index register.

```
(0.18H) ← (0.00H)
(0.19H) ← (0.00H)
        :
        :
(0.1FH) ← (0.00H)
    MOV  IXH, #00H ;   IX ← 00000000000B (0.00H)
    MOV  IXM, #00H
    MOV  IXL, #00H ;   Address 0.00H is specified for data memory.
```

```
LOOP1:
    SET1  IXE        ;  IXE flag ← 1
    ST    18H, 00H   ;  (0.1XH) ← (0.00H)
    CLR1  IXE        ;  IXE flag ← 0
    INC   IX         ;  Index register + 1
    SKGE  IXL, #08H
    BR    LOOP1
```



3.23 MOV @r, m

Move data memory to destination indirect

(1) Instruction code

01010	m_H	m_L	r

(2) Function

If MPE = 1:

[(MP), (R)] ← (M)

If MPE = 0:

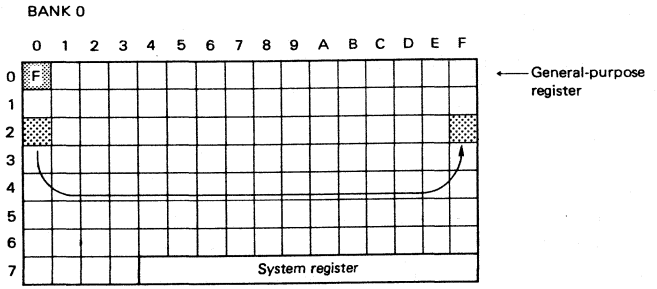
[m_H, (R)] ← (M)

The content of data memory addressed by M is stored into the data memory indicated by general-purpose register R. If MPE = 0, transfer occurs within the same row address of the same bank.

(3) **Example 1**

The content of address 0.20H is stored into address 0.2FH. The destination data memory is specified by the column address indicated by the general-purpose register (00H) and the row address of data memory (20H).

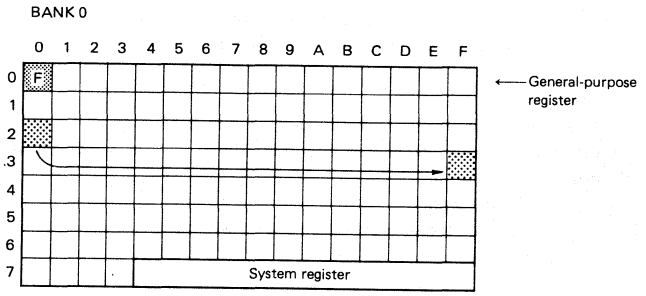
```
(0.2FH) ← (0.20H)
CLR1 MPE          ; MPE flag ← 0
MOV 00H, #0FH     ; Column address is set at general-purpose register
MOV @00H, 20H     ; Store.
```



Example 2

The content of address 0.20H is stored into address 0.3FH. The destination data memory is specified by the column address indicated by general-purpose register (00H) and the row address indicated by the memory pointer (MP).

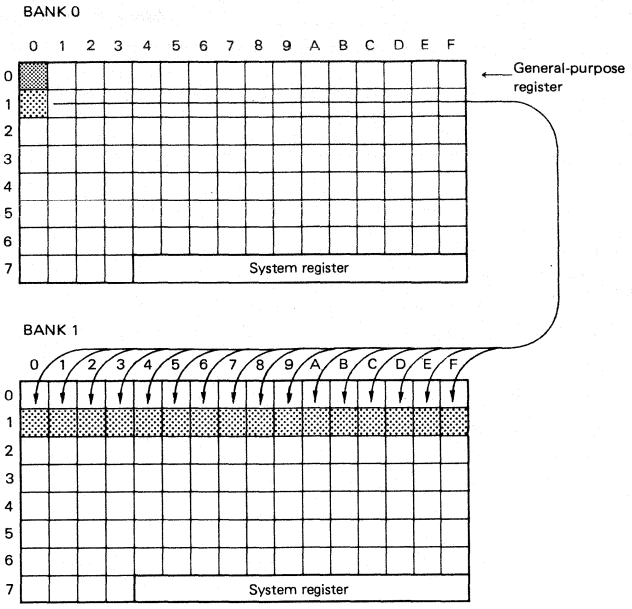
```
(0.3FH) ← (0.20H)
MOV  RPH, #00H   ;  General-purpose register is set on bank 0
MOV  RPL, #00H   ;  General-purpose register is set at row address 0
MOV  00H, #0FH   ;  Column address is set in general-purpose register
MOV  MPH, #00H   ;  Row address is set in memory pointer.
MOV  MPL, #03H
SET1 MPE         ;  MPE flag ← 1
MOV  @00H, 20H   ;  Store.
```



Example 3

The content of address 0.10H is stored into addresses 1.10H to 1.1FH.

```
(1.10H) ← (0.10H)
(1.11H) ← (0.10H)
        :
        :
(1.1FH) ← (0.10H)
MOV  RPH, #00H   ;  General-purpose register is set on bank 0.
MOV  RPL, #00H   ;  General-purpose register is set at row address 0.
MOV  00H, #00H   ;  Column address is set in general-purpose register.
MOV  MPH, #00H   ;  Bank 1 and row address 1 are set for memory pointer.
MOV  MPL, #09H
SET1 MPE         ;  MPE flag ← 1
LOOP 1:
MOV  @00H, 10H   ;  [(MP), (00H)] ← (10H)
ADD  00H, #01H   ;  Column address + 1
SKT1 CY          ;  Operation completed for address 1FH of bank 1?
BR   LOOP1
```


BANK 0
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register
General-purpose register
BANK 1
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register

3.24 MOV m, @r

Move data memory to destination indirect

(1) Instruction code

11010	m_H	m_L	r

(2) Function

If MPE = 1: (M) ← [(MP), (R)]

If MPE = 0: (M) ← [m_H, (R)]

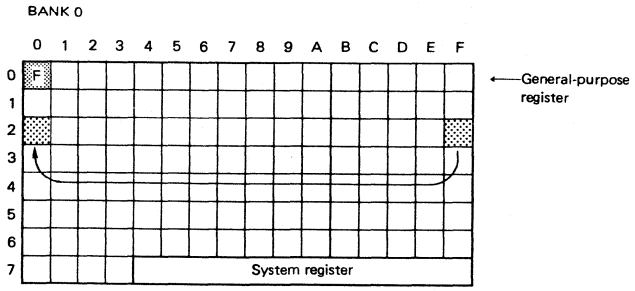
The content of data memory indicated by the general-purpose register R is stored into the data memory addressed by M. When MPE = 0, this movement occurs within the same row address on the same bank.

(3) **Example 1**

The content of address 0.2FH is stored into address 0.20H. The destination data memory is specified by the column address indicated by the general-purpose register (00H) and the row address of the data memory (20H).

(0.20H) ← (0.2FH)

```
CLR1 MPE        ; MPE flag ← 0
MOV 00H, #0FH   ; Column address is set at general-purpose register
MOV 20H, @00H   ; Store
```

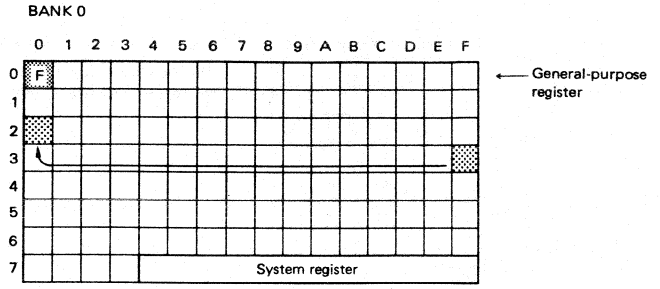


Example 2

The content of address 0.3FH is stored into address 0.20H. The destination data memory is specified by the column address indicated by general-purpose register (00H) and the row address indicated by memory pointer (MP).

(0.20H) ← (0.3FH)

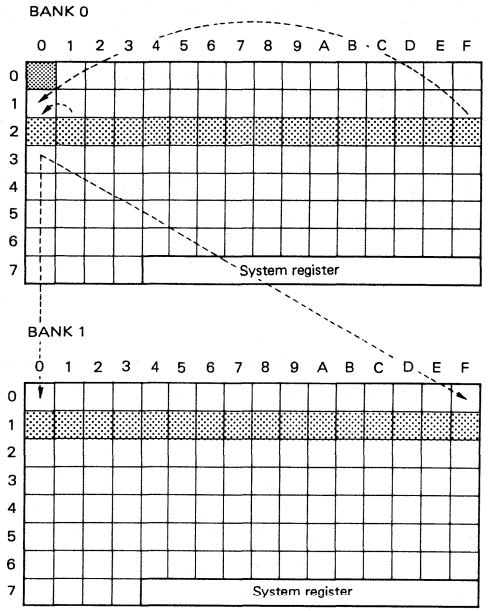
```
MOV 00H, #0FH   ; Column address is set at general-purpose register
MOV MPH, #00H   ; Row address is set at memory pointer.
MOV MPL, #03H   ;
SET1 MPE        ; MPE flag ← 1
MOV 20H, @00H   ; Store
```



Example 3

The contents of addresses 0.20H to 0.2FH are stored into addresses 1.10H to 1.1FH. The storing data memory is specified by the column address indicated by the general-purpose register (00H) and memory pointer (MP) or row address of data memory (20H).

```
(1.10H) ← (0.20H)
(1.11H) ← (0.21H)
(1.12H) ← (0.22H)
        :
        :
(1.1FH) ← (0.2FH)
    CLR1 MPE          ; MPE flag ← 0
    MOV 00H, #00H     ; Column address is set in the general-purpose register.
    MOV MPH, #00H     ; Memory pointer is set.
    MOV MPL, #09H     ; Bank 1, row address 1
LOOP1:
    MOV 20H, @00H     ; (20H) ← [2, (00H)]
    SET1 MPE          ; MPE flag ← 1
    MOV @00H, 20H     ; [(MP), (00H)] ← (20H)
    CLR1 MPE          ; MPE flag ← 0
    ADD 00H, #01H     ; Column address +1
    SKT1 CY           ; Up to 1FH of bank 1 terminated
    BR LOOP1
```


BANK 0
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register
General-purpose register
The data is transferred via 20H.
BANK 1
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
5
6
7
System register

3.25 MOV m, #i

Move immediate data to data memory

(1) Instruction code

11101	m_H	m_L	i

(2) Function

(M) ← i

The immediate data i is stored in the data memory addressed by M.

(3) **Example 1**

The immediate data 0AH is stored to address 0.50H used as data memory.

```
0.50H ← 0AH
MOV 50H, #0AH
```

Example 2

If IXH = 0, IXM = 3, IXL = 2 and IXE flag = 1 when address 0.00H is specified as data memory, then the immediate data 07H is stored into address 0.32H.

```
0.32H ← 07H
MOV IXH, #00H    ;  IX ← 00000110010B (0.32H)
MOV IXM, #03H
MOV IXL, #02H
SET1 IXE         ;  IXE flag ← 1
MOV 00H, #07H
```

3.26 MOVT DBF, @AR

Move program memory data specified by AR to DBF

(1) Instruction code

00111	000	0001	0000

(2) Function

SP ← SP − 1,
STACK ← PC,
DBF ← $(AR)_{rom}$,
PC ← STACK,
SP ← SP + 1

The content of program memory addressed by address register AR is stored into data buffer DBF.
Attention should be paid to the nesting such as subroutine and interruption, because this instruction temporarily uses one level of stack.

(3) **Example 1**

The 16-bit table data is transferred to the data buffers (DBF3, DBF2, DBF1, DBF0) according to the values of address registers (AR3, AR2, AR1, AR0) in the system register.

```
                ;*
                ;** Table data
                :*
Address         ORG 0010H
0010H           DW 0000000000000000B ; (0000H)
0011H           DW 1010101111001101B ; (0ABCDH)
                        :
                        :
                ;*
                ;** Table reference program
                ;*
                MOV AR3, #00H  ;  AR3 ← 00H  0011H is set in address register.
                MOV AR2, #00H  ;  AR2 ← 00H
                MOV AR1, #01H  ;  AR1 ← 01H
                MOV AR0, #01H  ;  AR0 ← 01H
                MOVT DBF, @AR  ;  Data of address 0011H is transferred to DBF.
```

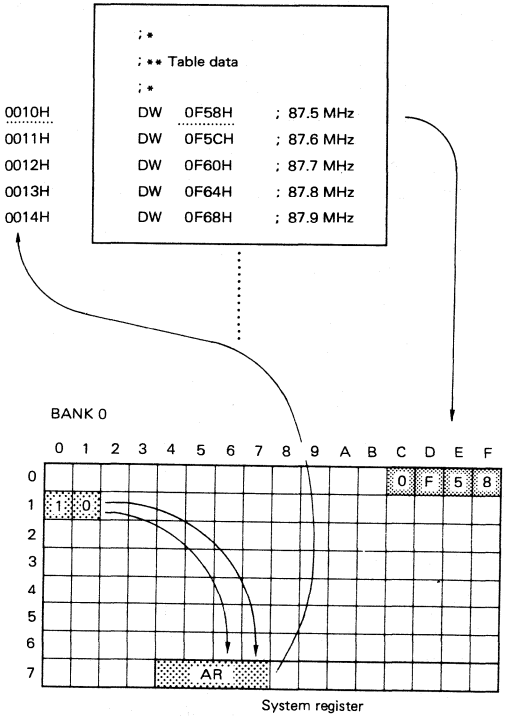
In this case, the data stored in DBF is shown below.

DBF3 = 0AH
DBF2 = 0BH
DBF1 = 0CH
DBF0 = 0DH

Example 2

The channel number is set at addresses 0.10H and 0.11H as data memory, and the divided value (N value) of PLL is obtained according to the content of the memory. The N value is then transferred to the PLL register.

```
                ;*
                ;** Table data for N value
                ;*
Address         ORG 0010H
0010H           DW 0F58H   ;  87.5 MHz (Lowest frequency 00 channel)
0011H           DW 0F5CH   ;  87.6 MHz
0012H           DW 0F60H   ;  87.7 MHz
0013H           DW 0F64H   ;  87.8 MHz
0014H           DW 0F68H   ;  87.9 MHz
0015H           DW 0F6CH   ;  88.0 MHz
0016H           DW 0F70H   ;  88.1 MHz
0017H           DW 0F74H   ;  88.2 MHz
                    .
                    .
                    .
                    .
                    .
                    .
                    .
                ;*
                ;** N value setting program
                ;*
                MOV  RPH, #00H   ;  RPH ← 00H  Row address 7 (0.70H
                MOV  RPL, #0EH   ;  RPL ← 0EH to 0.7FH) is set as
                MOV  AR3, #00H   ;  AR3 ← 0  general-purpose
                MOV  AR2, #00H   ;  AR2 ← 0  register.
                LD   AR1, 10H    ;  AR1 ← 10H  Channel data upper
                LD   AR0, 11H    ;  AR0 ← 11H  Channel data lower
                ADD  AR1, #01H   ;  0010H is added to the address
                ADDC AR2, #00H   ;  register since table data start
                ADDC AR3, #00H   ;  address starts at address 0010H.
                MOVT DBF, @AR    ;  Table data is stored to DBF.
                PUT  PLLR, DBF   ;  N value is transferred to PLL register (PLLR).
```



(4) **Notes**

1. The number of bits allowed for use with address registers (AR3, AR2, AR1, AR0) vary with the device types. When using, reference should be made to the appropriate manual of the device to be used.
2. When executing 'MOVT' instruction, one level of stack is used. Accordingly, sufficient care should be exercised to the stack level when using this instruction within a subroutine or interrupt processing routine.

3.27 PUSH AR

Push address register

(1) Instruction code

00111	000	1101	0000

(2) Function

SP ← SP – 1,

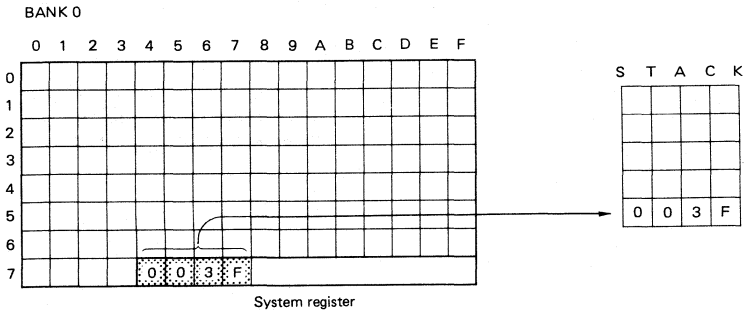
STACK ← AR

The value of address register AR is stored into STACK after decrement of the stack pointer SP.

(3) **Example 1**

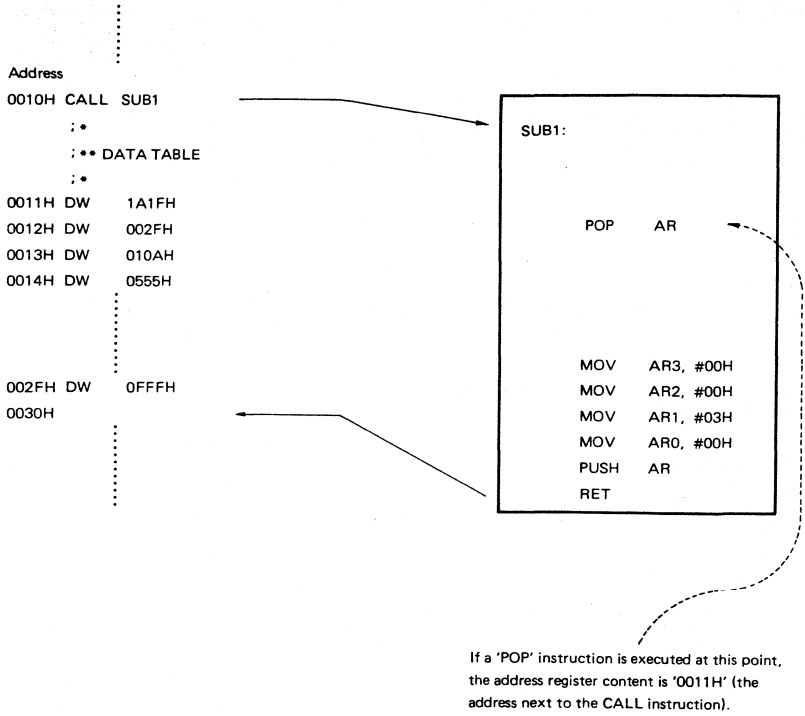
The address register is set at 003FH and stored into the stack.

```
MOV AR3, #00H
MOV AR2, #00H
MOV AR1, #03H
MOV AR0, #0FH
PUSH AR
```



Example 2

When the data table is placed behind a subroutine, the return address of the subroutine is set in the address register for returning.


Address
0010H CALL SUB1
;*
;** DATA TABLE
;*
0011H DW 1A1FH
0012H DW 002FH
0013H DW 010AH
0014H DW 0555H
002FH DW 0FFFH
0030H
SUB1:
POP AR
MOV AR3, #00H
MOV AR2, #00H
MOV AR1, #03H
MOV AR0, #00H
PUSH AR
RET
If a 'POP' instruction is executed at this point, the address register content is '0011H' (the address next to the CALL instruction).

3.28 POP AR

Pop address register

(1) Instruction code

00111	000	1100	0000

(2) Function

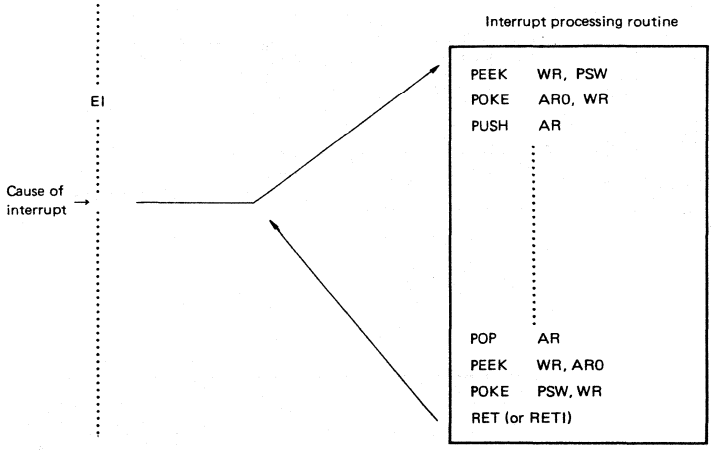
AR ← STACK,

SP ← SP + 1

The content of STACK is taken out to the address register, then the stack pointer SP is incremented.

(3) **Example**

When performing an interrupt processing, PSW may be changed within the interrupt processing routine. In such a case, the content of PSW is transferred to the address register via WR at the beginning of the interrupt processing, and then it is saved into the STACK by a 'PUSH' instruction. Before returning of the routine, the saved content is put into the address register by a 'POP' instruction, and then it is transferred to PSW via WR.



3.29 PEEK WR, rf

Peek register file to window register

(1) Instruction code

00111	rf_H	0011	rf_L

(2) Function

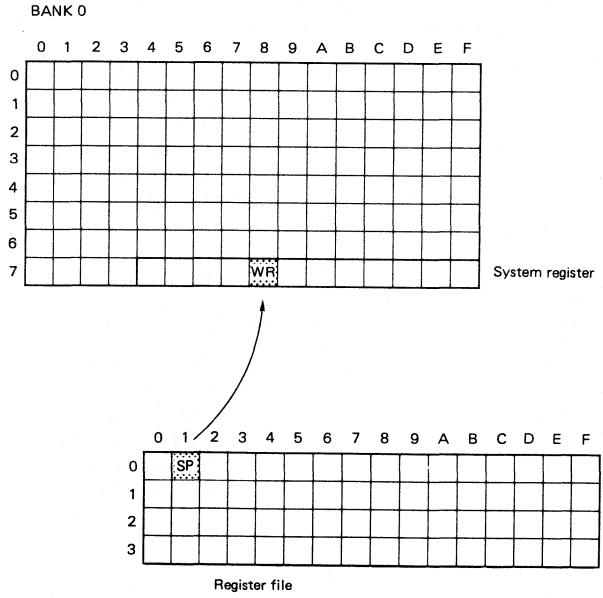
WR ← (rf)

The content of the register file addressed by rf is stored into the window register WR.

(3) **Example 1**

The content of the stack pointer SP of address 01H in the register file is stored into the window register.

```
PEEK   WR, SP
```



3.30 POKE rf, WR

Poke window register to register file

(1) Instruction code

00111	rf_H	0010	rf_L

(2) Function

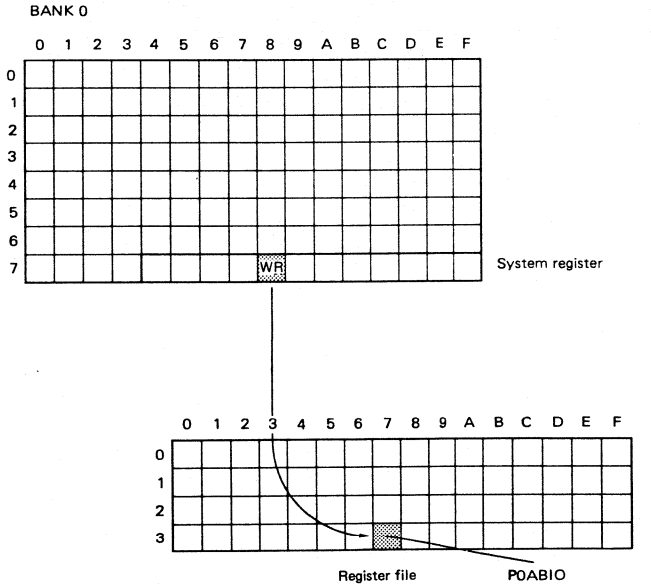
(rf) ← WR

The content of window register WR is stored into the register file addressed by rf.

(3) **Example 1**

The immediate data 0FH is stored into the register file POABIO via the window register.

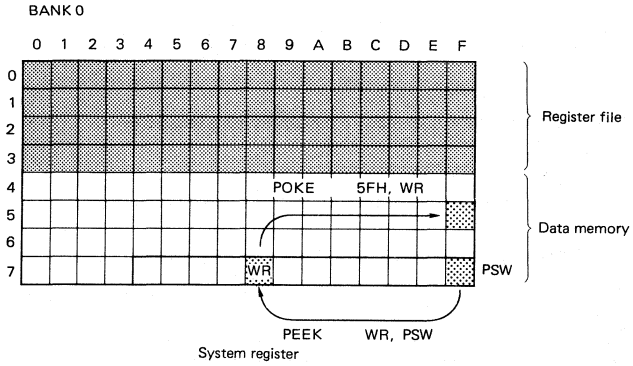
```
MOV   WR, #0FH
POKE  POABIO, WR ;  Each of POA0, POA1, POA2 and POA3 is set in the output mode.
```



(4) **Note**

The 'PEEK, POKE' instruction permits accessing of addresses 40H to 7FH in each bank of the data memory in addition to the register file. For example, this instruction can be used in the following way.

```
PEEK WR, PSW    ;  The content of PSW (7FH) in system register is stored into WR.
POKE 5FH, WR    ;  The content of WR is stored into address 5FH of data memory.
```



3.31 GET DBF, p

Get peripheral data to data buffer

(1) Instruction code

00111	P_H	1011	P_L

(2) Function

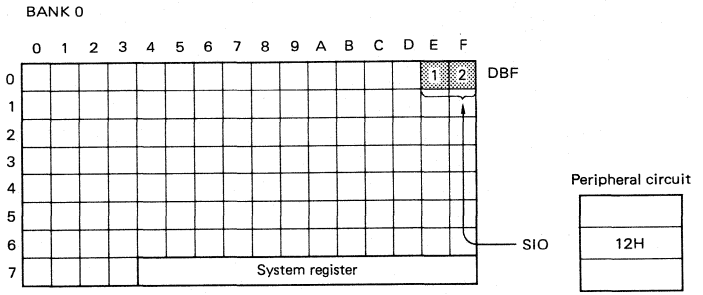
DBF ← (p)

The content of peripheral circuit addressed by p is stored into the data buffer DBF.

(3) **Example 1**

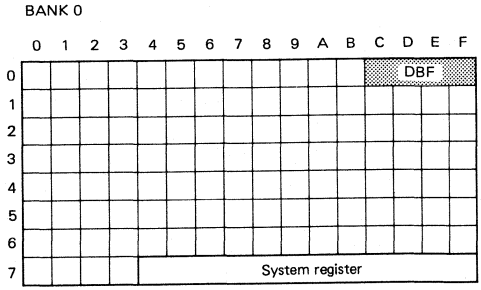
The content (8 bits) of the peripheral shift register (SIO) is stored into data buffers DBF0 and DBF1.

GET DBF, SIO



(4) **Notes**

1. The data buffer is allocated to 0CH, 0DH, 0EH, and 0FH in bank 0 of the data memory, irrespective of the value of the bank register.



2. The data buffer has a total of 16 bits. The number of bits to be used as the unit of input/output varies with the peripheral circuit accessed by 'GET' instruction. For example, if a 'GET' instruction is executed for a peripheral circuit whose input/output is done in units of 8 bits, data is stored to the lower 8 bits (DBF1, DBF0) of the data buffer DBF. Pay attention to the number of bits required as the unit of input/output because it varies with the peripheral circuits of each device.

3.32 PUT p, DBF

Put data buffer to peripheral

(1) Instruction code

00111	PH	1010	PL

(2) Function

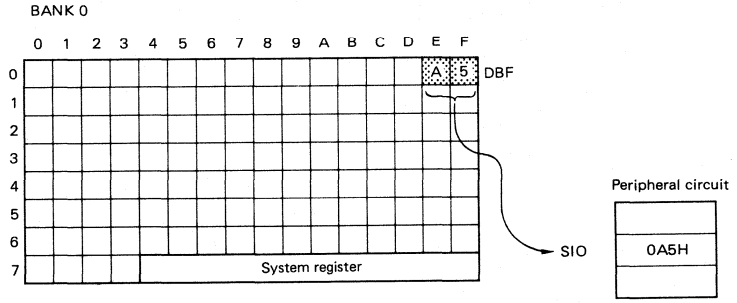
(p) ← DBF

The content of data buffer DBF is stored into the peripheral circuit addressed by p.

(3) **Example 1**

0AH and 05H are set into data buffers DBF1 and DBF0, respectively, and are then transferred to the shift register (SIO) of peripheral circuit.

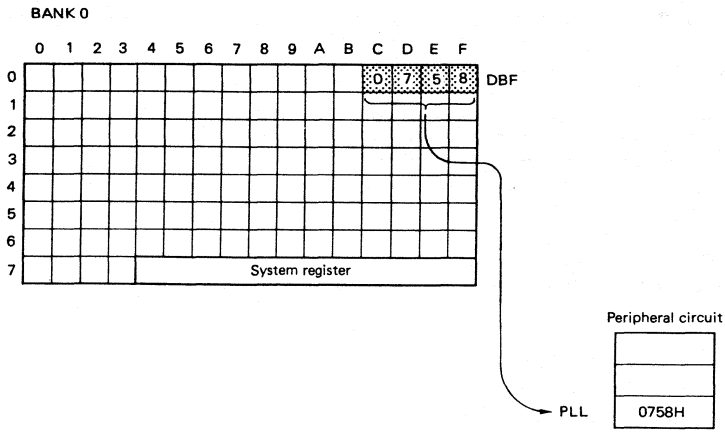
```
MOV  BANK, #00H ;  Data memory bank 0
MOV  DBF0, #05H
MOV  DBF1, #0AH
PUT  SIO
     DBF
```



Example 2

The data 0758H is set as PLL data in data buffers DBF0-DBF3, and then it is transferred to PLL register (PLL) of the peripheral circuit.

```
MOV  DBF3, #00H
MOV  DBF2, #07H
MOV  DBF1, #05H
MOV  DBF0, #08H
PUT  PLL, DBF
```



(4) **Note**

The data buffer size is 16 bits. The number of bits required as the unit of input/output varies with the peripheral circuit accessed by 'PUT' instruction. For example, the shift register SIO requires 8-bit input/output. When a 'PUT' instruction is executed, the contents of lower 8 bits (DBF1, DBF0) of data buffer DBF are transferred to the peripheral circuit. (The contents of DBF3 and DBF2 are not transferred.)

3.33 SKT m, #n

Skip next instruction if data memory bits are true

(1) Instruction code

11110	m_H	m_L	n

(2) Function

If the ANDed result of the content of data memory addressed by M and immediate data n is not 0, then the next one instruction is skipped.

(3) **Example 1**

If bit 0 of address 03H is '1', control jumps to AAA; if '0', it jumps to BBB.

```
SKT  03H, #0001B
BR   BBB
BR   AAA
```

Example 2

If bit 0 and bit 1 of address 03H are both '1', the next instruction is skipped.

```
SKT  03H, #0011B
```

		B_3	B_2	B_1	B_0	
Skip condition	03H	x	x	1	1	x: don't care

Example 3

The following two instructions provide the same execution result.

- SKT 13H, #1111B
- SKE 13H, #0FH

3.34 SKF m, #n

Skip next instruction if data memory bits are false

(1) Instruction code

11111	m_H	m_L	n

(2) Function

When the result of AND of the content of data memory addressed by M and the immediate data n is 0, the next one instruction is skipped.

(3) **Example 1**

If bit 2 of address 13H is '0', 00H of the immediate data is stored into address 0FH in the data memory; if '1', control jumps to ABC.

```
SKF  13H, #0100B
BR   ABC
MOV  0FH, #00H
```

Example 2

If bit 3 and bit 0 of address 29H are both '0', the next instruction is skipped.

```
SKF  29H, #1001B
```

		B_3	B_2	B_1	B_0	
Skip condition	29H	0	x	x	0	x: don't care

Example 3

The following two instructions provide the same execution result.

- SKF 34H, #1111B
- SKE 34H, #00H

3.35 BR addr

Branch to the address

(1) Instruction code

011	addr

(2) Function

PC ← addr

Control branches to the address indicated by addr.

The range of address to which direct branch by this instruction is allowed is 8K steps from address 0000H to address 1FFFH. When branching is required to address 2000H or after, use the following 'BR @AR' instruction.

(3) **Example**

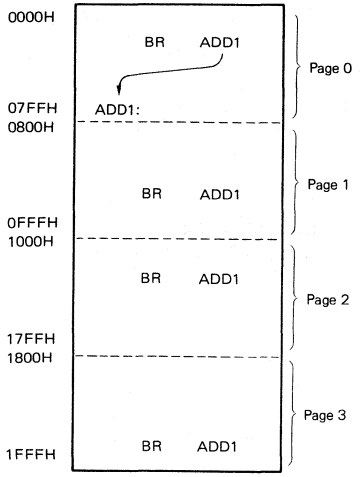
```
FLY   LAB   0FH   ;  FLY = 0FH is defined.
        :
        :
      BR    FLY   ;  Jumps to address 0F.
        :
        :
      BR    LOOP1;  Jumps to LOOP1.
        :
        :
      BR    $+2   ;  Jumps to the address which is lower by 2 than the current address.
        :
        :
      BR    $-3   ;  Jumps to the address which is higher by 3 than the current address.
        :
        :
LOOP1:
```

(4) **Note**

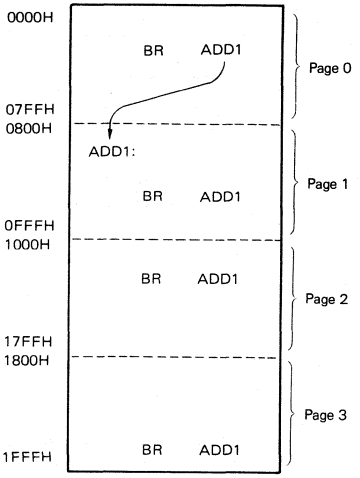
The BR instruction can be described in assembler without mentioning the page. The same description can be used between ROM addresses 0000H and 1FFFH. However, the BR instruction into page 0 (addresses 0000H to 07FFH), BR instruction into page 1 (addresses 07FFH to 0FFFH), BR instruction into page 2 (addresses 1000H to 17FFH), and BR instruction into page 3 (addresses 17FFH to 1FFFH) have respectively different operation codes.

The operation code in page 0 is '0C', in page 1, '0D', in page 2, '0E', and in page 3, '0F'. If the μPD17000 series assembler is used, these operation codes are automatically converted by the assembler by referencing the respective jump destinations.

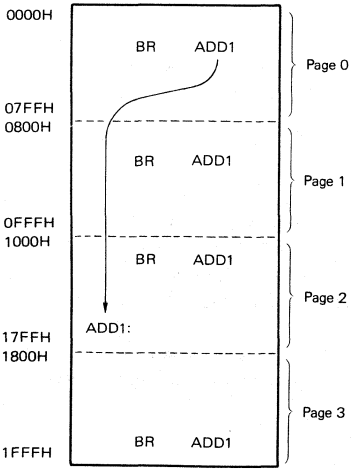
When operation code is '0C'
(The jumping destination address is in page 0)



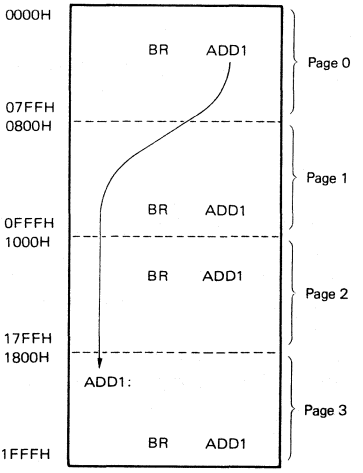
When operation code is '0D'
(The jumping destination address is in page 1)



When operation code is '0E'
(The jumping destination address is in page 2)

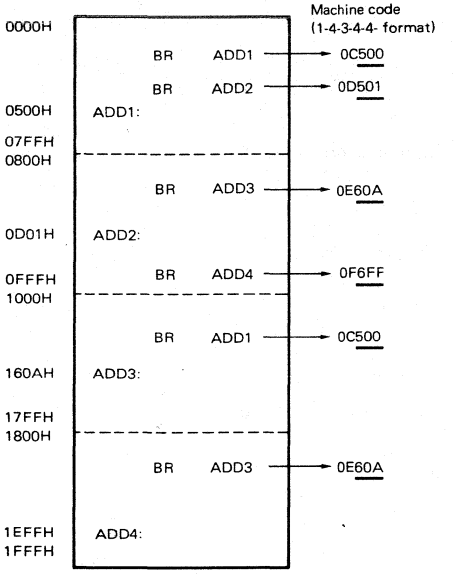


When operation code is '0F'
(The jumping destination address is in page 3)



When batch correction is required in debugging, the programmer is required to convert each of the operation codes '0C', '0D', '0E', and '0F' by himself.

Address must also be converted if the jump destination of BR instruction is in any of address 0000H to 07FFH, address 0800H to 0FFFH, address 1000H to 17FFH, and address 1800H to 1FFFH. In other words, each of address 0000H, address 0800H, address 1000H and address 1800H can be assumed as address 000H, which is incremented by 1, respectively.



Note: The number of pages varies from device to device of the μPD17000 series. Please refer to the manual of the device to be used.

3.36 BR @AR

Branch to the address specified by address register

(1) Instruction code

00111	000	0100	0000

(2) Function

PC ← AR

Control branches to the address indicated by the address register (AR).

(3) **Example 1**

003FH is set in the address register AR (AR0-AR3), and execution jumps to address 003FH by the 'BR @AR' instruction.

```
MOV   AR3, #00H  ;  AR3 ← 00H
MOV   AR2, #00H  ;  AR2 ← 00H
MOV   AR1, #03H  ;  AR1 ← 03H
MOV   AR0, #0FH  ;  AR0 ← 0FH
BR    @AR        ;  Jump to address 003FH
```

Example 2

The branching destination is changed as shown below depending on the content of address 0.10H of the data memory.

Content of 0.10H		Label of destination
00H	→	AAA
01H	→	BBB
02H	→	CCC
03H	→	DDD
04H	→	EEE
05H	→	FFF
06H	→	GGG
07H	→	HHH
08H-0FH	→	ZZZ

```
        ;*
        ;** Jump table
Address ;*
0010H   BR      AAA
0011H   BR      BBB
0012H   BR      CCC
0013H   BR      DDD
0014H   BR      EEE
0015H   BR      FFF
0016H   BR      GGG
0017H   BR      HHH
0018H   BR      ZZZ
          :
          :
```

```
MOV   RPH, #00H   ;  General-purpose register bank 0
MOV   RPL, #02H   ;  General-purpose register row address 1
MOV   AR3, #00H   ;  AR3 ← 00H AR is set to 001 x H.
MOV   AR2, #00H   ;  AR2 ← 00H
MOV   AR1, #01H   ;  AR1 ← 01H
ST    AR0, 10H    ;  AR0 ← 0.10H
SKF   AR0, #1000B;  If the content of AR0 is greater than
AND   AR0, #1000B;  08H, the content of AR0 is changed to
BR    @AR         ;  08H.
```

(4) **Note**

The number of bits of address registers (AR3, AR2, AR1, AR0) allowed for use varies with the device types. When using the address register, reference should be made to the manual of the appropriate device.

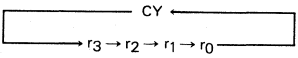
3.37 RORC r

Rotate right general register with carry flag

(1) Instruction code

00111	000	0111	r

(2) Function



The content of the general-purpose register indicated by R is shifted to the right by one bit, with carry flag included.

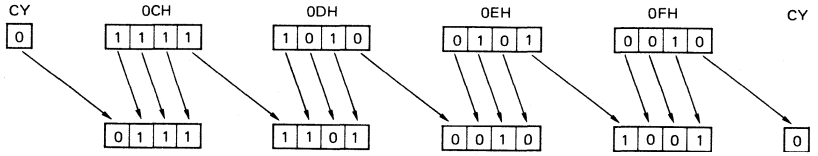
(3) **Example 1**

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the value of address 0.00H (1000B) is shifted to the right by one bit, and the value becomes 0100B.

```
0.00H ← (0.00H) ÷ 2
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
CLR1 CY         ;  Carry flag ← 0
RORC 00H
```

Example 2

When row address 0 (0.00H to 0.0FH) of bank 0 is specified as general-purpose register (RPH = 0, RPL = 0), the value 0FA52H of data buffer (DBF) is shifted to the right by one bit, and the content of DBF is changed to 7D29H.




```
MOV  RPH, #00H  ;  General-purpose register bank 0
MOV  RPL, #00H  ;  General-purpose register row address 0
CLR1 CY         ;  Carry flag ← 0
RORC 0CH
RORC 0DH
RORC 0EH
RORC 0FH
```

3.38 CALL addr

Call subroutine

(1) Instruction code

11100	addr

(2) Function

$SP \leftarrow SP - 1$,

$STACK \leftarrow PC + 1$,

$PC_{0\text{-}10} \leftarrow addr$,

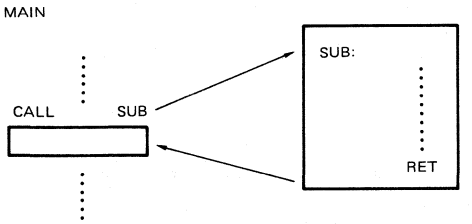
$PC_{11\text{-}15} \leftarrow 0$

The value of the program counter (PC) is incremented, and then it is stored into the stack. After this, execution branches to the subroutine indicated by addr.

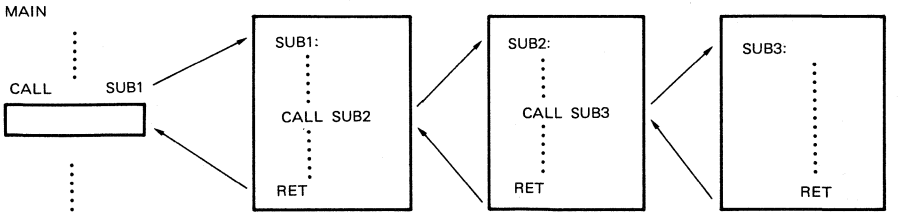
This instruction can be used to call subroutines contained within 2K steps from address 0000H to address 07FFH. It is therefore advisable to allocate frequently using subroutines in the range from address 0000H to 07FFH.

To call a subroutine allocated after address 0800H, use the 'CALL @AR' instruction to be mentioned in the next section.

(3) **Example 1**



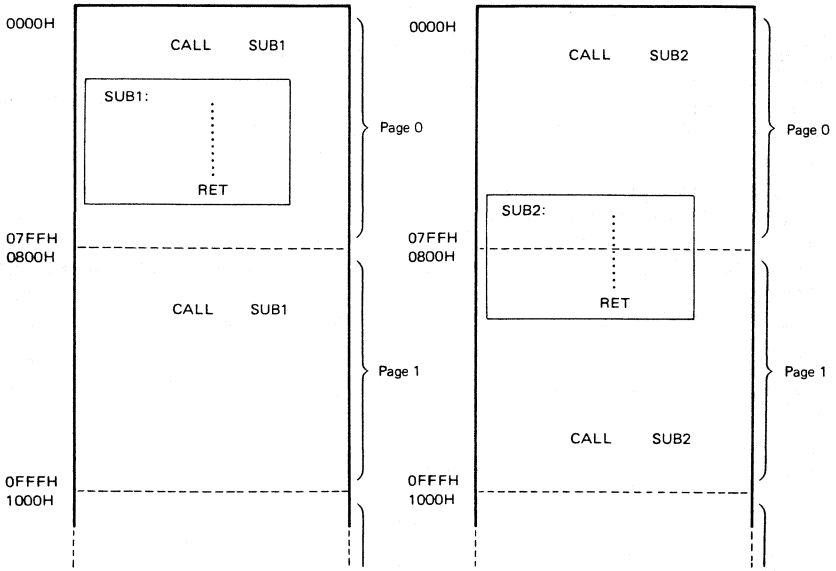
Example 2



(4) **Note**

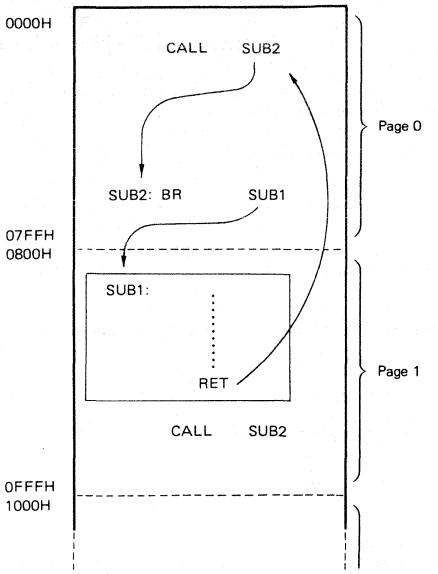
When using a 'CALL' instruction, the calling address, or the initial address of the subroutine to be called must be placed within page 0 (0000H to 07FFH). When calling a subroutine whose initial address is not positioned in page 0, use 'CALL @AR' instruction.

When initial address of subroutine is put in page 0



If the initial address of the subroutine is placed within page 0, the end address of the subroutine ('RET' or 'RETSK' instruction) may be placed outside of page 0.

The 'CALL' instruction can be used without considering page as far as the initial address of the subroutine to be called is placed within page 0. However, the following technique is useful when it is impracticable to place the initial address of a subroutine within page 0.



In this method, 'BR' instruction is set within page 0, and the actual subroutine is called by using this 'BR' instruction.

3.39 CALL @AR

Call subroutine specified by address register

(1) Instruction code

00111	000	0101	0000

(2) Function

SP ← SP − 1,

STACK ← PC + 1,

PC ← AR

The value of program counter (PC) is incremented, and stored into the stack, then execution branches to the subroutine indicated by address register (AR).

(3) **Example 1**

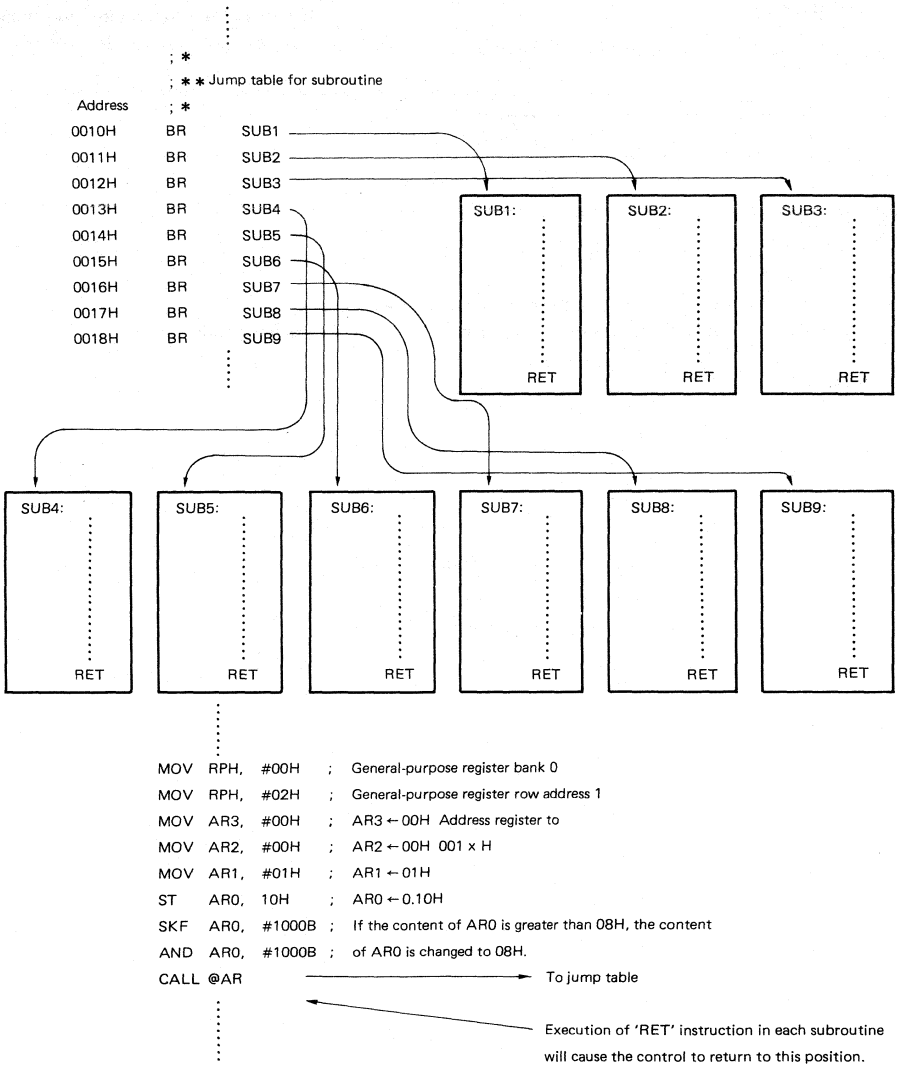
Value 0020H is set in the address register AR (AR0-AR3), and the subroutine of address 0020H is called by the 'CALL @AR' instruction.

```
MOV  AR3, #00H  ;  AR3 ← 00H
MOV  AR2, #00H  ;  AR2 ← 00H
MOV  AR1, #02H  ;  AR1 ← 02H
MOV  AR0, #00H  ;  AR0 ← 00H
CALL @AR        ;  Subroutine at address 0020H is called.
```

Example 2

The following subroutines are called depending on the contents of address 0.10H of the data memory.

Content of 0.10H		Subroutine name
00H	→	SUB1
01H	→	SUB2
02H	→	SUB3
03H	→	SUB4
04H	→	SUB5
05H	→	SUB6
06H	→	SUB7
07H	→	SUB8
08H-0FH	→	SUB9



(4) **Note**

The number of bits of address registers (AR3, AR2, AR1, AR0) allowed for use varies with the device types. When using the address register, reference should be made to the manual of the appropriate device.

3.40 RET

Return to the main program from subroutine

(1) Instruction code

00111	000	1110	0000

(2) Function

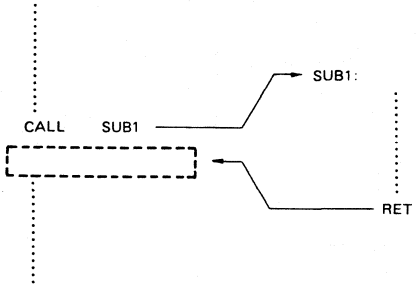
PC ← STACK,

SP ← SP + 1

This instruction is used to return to the main program from a subroutine.

The return address saved into the stack by CALL instruction is restored to the program counter.

(3) **Example**



3.41 RETSK

Return to the main program then skip next instruction

(1) Instruction code

00111	001	1110	0000

(2) Function

PC ← STACK,
SP ← SP + 1,
PC ← PC + 1

This instruction is used to return to the main program from a subroutine. The instruction following the 'CALL' instruction is skipped. That is, the return address saved to the stack by 'CALL' instruction is restored in the program counter (PC), then the program counter is incremented.

(3) **Example**

If the content of LSB (least significant bit) of address 25H of the data memory (RAM) is '0', the 'RET' instruction is executed, then control returns to the instruction next to the 'CALL' instruction. If the content is '1', 'RETSK' instruction is executed, and control returns to the instruction (in this example, ADD 03H, 16H) that follows the 'CALL' instruction.

```
   :                          :
   :                 SUB1:    :
   :                          :
CALL   SUB1                   :
BR     LOOP                 SKF     25H, #0001 B
ADD    03H, 16H             RETSK                ; LSB of 25H is '1'
   :                        RET                  ; LSB of 25H is '0'
   :
```

3.42 RETI

Return to the main program from interrupt service routine

(1) Instruction code

00111	100	1110	0000

(2) Function

PC ← STACK,

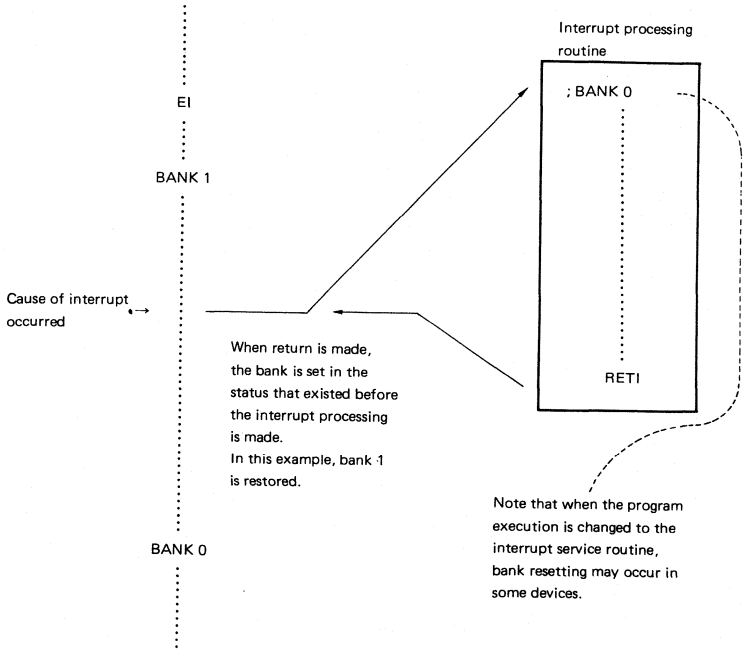
SP ← SP + 1

This instruction is used to return to the main program from an interrupt processing program. The return address which was saved into the stack by vector interrupt is restored in the program counter.

In some devices, a part of the system register is also returned to the status that existed before occurrence of vector interrupt.

(3) **Example**

A vector interrupt occurred when the data memory is placed in bank 1. Saving of data memory bank is needed since the data memory bank 0 is required for interrupt processing.



(4) **Notes**

1. The content of system register saved automatically by interrupt (this content can be restored by 'RETI' instruction) varies from device to device. Reference should be made to the manual of the device to be used.

2. If 'RETI' instruction is used in place of the 'RET' instruction in an ordinary subroutine, the bank and other data (saved by the interrupt) are restored when program execution returns to the return address. This may result in undefined status after returning. To avoid this, be sure to use the 'RET' (or 'RETSK') instruction when returning from a subroutine.

3.43 EI

Enable interrupt

(1) Instruction code

00111	000	1111	0000

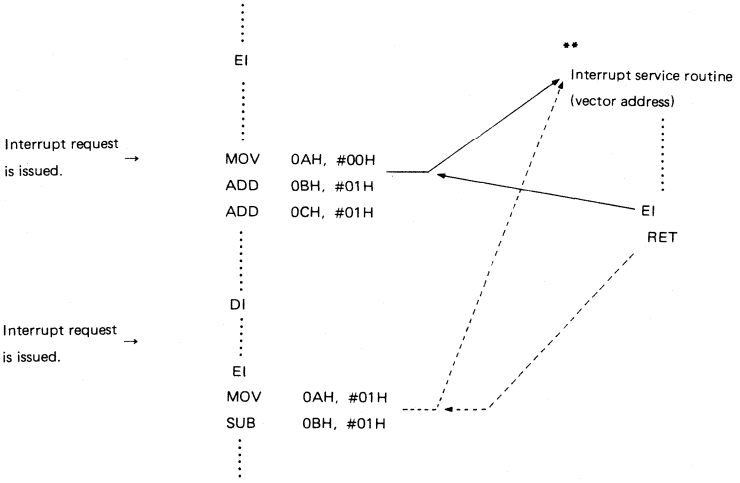
(2) Function

This instruction enables vector interrupt.

Vector interrupt is enabled after executing the instruction that follows the 'EI' instruction.

(3) **Example 1**

As shown in the following example, the interrupt request is actually accepted and program execution changes to the vector address after completing execution of the instruction (except program counter operating instruction) that follows this EI instruction.*

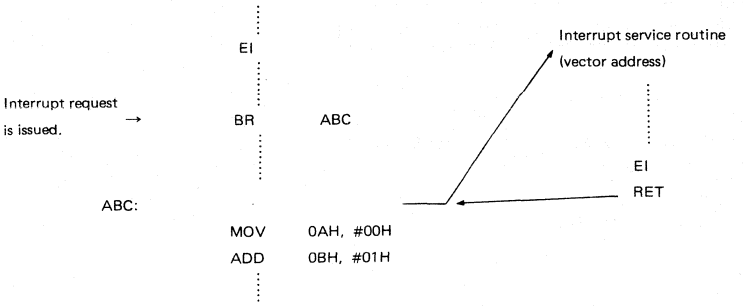


*: The vector address varies with the interrupt accepted. For details, refer to the manual of the device to be used.

**: Assume that the interrupt to be accepted here (Interrupt request is issued after execution of EI instruction and the flow of program execution changes to the interrupt service routine) is provided with the interrupt permission flag (IP) for that interrupt. No change will occur in the flow of program execution (that is, interrupt will not be accepted) if an interrupt request is issued after execution of the EI instruction, provided no interrupt permission flag is set for such interrupt. However, this causes the interrupt request flag (IREQ) to be set, hence the interrupt request will be accepted at the time when the interrupt permission flag is set. (For details, refer to the device manual.)

Example 2

Shown below is an example of interrupt caused by the interrupt request which is accepted during execution of an instruction for operating program counter (PC).



3.44 DI

Disable interrupt

(1) Instruction code

00111	001	1111	0000

(2) Function

This instruction is used to disable vector interrupt.

(3) **Example**

See Example 1 of Section 3.43.

3.45 STOP s

Stop CPU and release by condition s

(1) Instruction code

00111	010	1111	s

(2) Function

This instruction stops main clock, and turns the device to STOP mode.

The current consumption can be minimized by setting a device in the STOP mode.

The operand (s) specifies the condition by which the STOP mode is released and main clock oscillation re-started.

3.46 HALT h

Halt CPU and release by condition h

(1) Instruction code

00111	011	1111	h

(2) Function

This instruction turns the device into HALT mode.

The current consumption can be reduced by setting the device in HALT mode.

The operand (h) specifies the condition by which the HALT mode is released and main clock oscillation started.

3.47 NOP

No operation

(1) Instruction code

00111	100	1111	0000

(2) Function

This instruction causes one machine cycle to be consumed by executing nothing.

Development tools for μPD17K-Family

Section 4 - Development tools

Development tools

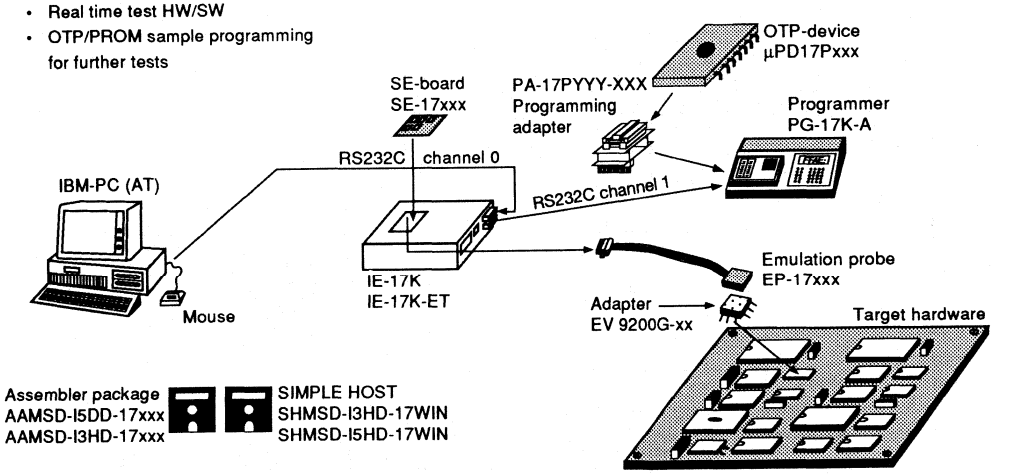
1. Development tools for the μPD17K-Family

This section gives a brief explanation of the development environment of the μPD17K-Family.

Hardware Tools:
- IE-17K
- IE-17K-ET
- SE-17xxx
- EP-17xxx
- EV-9200G-xx
- PG-17K-A
- PA-17PYYY-XXX

Software Tools:
- AAMSD-I5DD-170xx (Assembler for μPD170xx)
- AAMSD-I3HD-170xx (Assembler for μPD170xx)
- AAMSD-I5DD-171xx (Assembler for μPD171xx)
- AAMSD-I3HD-171xx (Assembler for μPD171xx)
- AAMSD-I5DD-172xx (Assembler for μPD171xx)
- AAMSD-I3HD-172xx (Assembler for μPD171xx)
- SHMSD-I5HD-17WIN (Source level debugger SIMPLEHOST)
- SHMSD-I3HD-17WIN (Source level debugger SIMPLEHOST)

- SW development
- HW/SW debugging
- Real time test HW/SW
- OTP/PROM sample programming for further tests



Development Enviroment

IE-17K

The IE-17K is a software development support tool applicable to every model of the μPD17K-Family. It consists of two boards:
a memory board and a supervisor board.

Features:

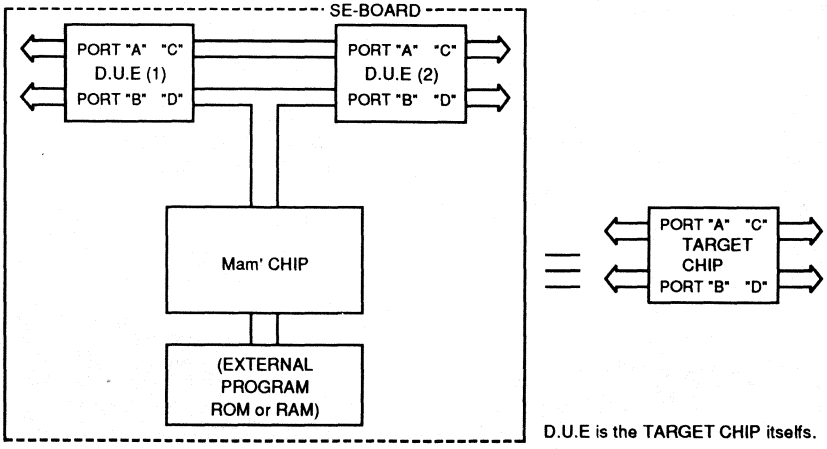
- Real-time emulation and one step emulation are available.
- Programmable break/trace function by which various break/trace conditions can be set hierarchically.
- Real-time trace function with a large-capacity trace memory (32K steps)
- Data memory coverage function which displays the state of writing in the data memory.
- Program memory coverage function which increments a counter every time an instruction which references to an address location is executed. The maximum count is 255.
- Incorporated programmable pattern generator (PPG) with 14 channels.

IE-17K-ET

IE-17K-ET has the same features like the IE-17K except for 3 differences:
- no internal power supply (external 5V power supply required)
- no Programmable Pulse Generator (PPG) available
- no logic analyzer port included

SE-17xxx

The SE-17xxx is the device-specific emulator board which completes the in-circuit-emulator. To ensure that the system evaluation (SE) board exhibits the same electrical behaviour as the original IC, a method known as „MAM chip" (implemented as an ASIC) device is applied. Two μPD17K devices and a MAM chip are mounted on the SE board as shown in the diagram. Half the I/O-lines of each 17K device are passed outside the board, so that they can be used to evaluate the I/O-lines of the real chip. Together with the MAM chip the other device form a bus system. All data sent out from the SE board or received by the SE board from outside are routed through the two μPD17K devices. Therefore an observer outside the SE board gets the impression that a real chip is being used. The external memory which is connected to the MAM chip stores the developed software in the case the SE board is used as a standalone system.



Emulation Chip Set Configuration

EP-17xxx

To connect the SE board with the printed circuit board a special cable is required. This device-specific emulation probe is called EP-17xxx.

EV-9200G-xx

The EV-9200G-xx is a special adapter socket to connect the emulation probe EP-17xxx with the target hardware in the case that the target device is mounted in a QFP package. This conversion socket is soldered onto the PCB.

PG-17K-A

The PG-17K-A is an OTP programmer which can be used for all 17K OTP devices. It is similar to the well known PROMAC2A.

PA-17PYYY-XXX

These are th appropiate programming adapters which have to be used in conjunction with PG-17K-A.

AAMSD-INXD-17Zxx
N = 3,5
X = D, H
Z = 0, 1, 2

These are absolute macro assembler packages used for all devices of the 170xx, 171xx and the 172xx device group. They all comprise two parts. One part is the main unit used for all devices of the corresponding device group, the other is a device file for the particular μPD17K device. The device file includes device-specific information, like ROM and RAM size, reserved words and addresses of the on-chip hardware functions. The assembler has a unique feature which supports software assembly of the code configured in modules. The assembler handles up to 99 modules. This feature, however, belongs to a relocatable assembler. The assembler is not able to assemble each module separately. Nevertheless, after the software is assembled for the first time, the assembler can be directed to assemble only those parts of the user program which were changed. Therefore the software development is speeded up.
The assembler also performs linkage operations to produce an executable code. In addition, this assembler supports powerful macro functions to end up in a versatile development tool for execution in a MS-DOS environment.

SIMPLEHOST

SIMPLEHOST is a full-screen debugger which improves the interface between the in-circuit-emulator and the operator. SIMPLEHOST runs under Microsoft Windows, which means that all emulator commands can be selected and activated with a mouse. The contents of the ROM and RAM size of the emulator are shown on the screen together with the source program.

Overview of development environment

Product	Assembler	Debugger	Evaluation Board SE-Board	In circuit emulator	Probe	Socket adapter	Package	Programmer	Programming adapters for OTP
17001	AAMSD-I5DD-170XX or AAMSD-I3HD-170XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17001	IE-17K-ET or IE-17K				PG-17K-A	PA-17P48G/0
					EP-17001GH	EV-9200GH-48	48QFP		
17003A/005	AAMSD-I5DD-170XX or AAMSD-I3HD-170XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17010	IE-17K-ET or IE-17K				PG-17K-A	PA-17P80G/0
					EP-17003GF	EV-9200G-80	80QFP		
17006	AAMSD-I5DD-170XX or AAMSD-I5HD-170XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17006	IE-17K-ET or IE-17K				PG-17K-A	PA-17P80G/2
					EP-17201GF	EV-9200G-80	80QFP		
17010	AAMSD-I5DD-170XX or AAMSD-I3HD-170XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17010	IE-17K-ET or IE-17K				PG-17K-A	PA-17P80G/0
					EP-17003GF	EV-9200G-80	80QFP		
17102	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17102	IE-17K-ET or IE-17K					NO OTP
					EP-17102G	EV-9200G-52	52QFP		
17103/103L	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17103L	IE-17K-ET or IE-17K	EP-17103CX		16DIP	PG-17K-A	PA-17P16CG22C24G
							16SOP		
17104/104L	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17104L	IE-17K-ET or IE-17K	EP-17104CS		22SDIP	PG-17K-A	PA-17P16CG22C24G
							24QFP		
17107/107L	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17107	IE-17K-ET or IE-17K	EP-17103CX		16DIP	PG-17K-A	PA-17P16CG22C24G
							16SOP		
17108/108L	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17108	IE-17K-ET or IE-17K	EP-17104CS		22SDIP	PG-17K-A	PA-17P16CG22C24G
							24QFP		
17120/121 17132/133	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17120	IE-17K-ET or IE-17K	EP-17120CS		24SDIP	PG-17K-A	PA-17P24CG28CG/0
							24SOP		
17134A/135A 17136/137A	AAMSD-I5DD-171XX or AAMSD-I3HD-171XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17134	IE-17K-ET or IE-17K	EP-17K28CT		28SDIP	PG-17K-A	PA-17P24CG28CG/0
					EP-17K28GT	TBD	28SOP		
17201A/207	AAMSD-I5DD-172XX or AAMSD-I3HD-172XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17207	IE-17K-ET or IE-17K				PG-17K-A	PA-17P80G/1
					EP-17201GF	EV-9200G-80	80QFP		
17202A	AAMSD-I5DD-172XX or AAMSD-I3HD-172XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17202	IE-17K-ET or IE-17K				PG-17K-A	PA-17P52G/64G/0
					EP-17202GF	EV-9200G-64	64QFP		
17203A	AAMSD-I5DD-172XX or AAMSD-I3HD-172XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17202	IE-17K-ET or IE-17K				PG-17K-A	PA-17P52G/64G/0
					EP-17202GC	EV-9200G-52	52QFP		
17204	AAMSD-I5DD-172XX or AAMSD-I3HD-172XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17204	IE-17K-ET or IE-17K				PG-17K-A	PA-17P52G/64G/0
					EP-17203GC	EV-9200G-52	52QFP		
17211	AAMSD-I5DD-172XX or AAMSD-I3HD-172XX	SHMSD-I5HD-17WIN or SHMSD-I3HD-17WIN	SE-17211	IE-17K-ET or IE-17K	EP-17K28CT			PG-17K-A	PA-17P24CG28CG/0
					EP-17K28GT	TBD	28SOP		

For further and more detailed information about the development tools of the μPD17K-Family please refer to the special user's manual „Development tools".

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Keeping our customers informed

Our offices throughout Europe are always at your service for comprehensive support. Here are some of the technical services we provide:

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- Seminars
- Update service
- Mailing list
- University programme

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